MICRO NETWORKS

MN5909

6-Bit, 100MHz CMOS
FLASH A/D CONVERTER

FEATURES

- 6-Bit Resolution Plus Overflow Bit
- 100MHz Typical Conversion Rate
- Single +5V Operation
- Low Input Capacitance
- Low Power (200mW, Typical)
- Externally-Strobed, Auto-Zeroed Comparators
- Small 20-Pin Ceramic or Plastic DIP
- 3-State Outputs
- Optional Environmental Stress Screening

DESCRIPTION

The MN5909 is a high-speed, low-power, monolithic CMOS Flash A/D converter. The MN5909 converts analog input signals into six-bit digital words at an impressive 100MHz (typ) rate. The device's transparent flash architecture contains 64 externally-strobed, auto-zeroed comparators, reference resistor ladder, decode logic and output 3-state buffers. An intermediate tap is provided for user adjustments of integral linearity.

The converter provides six TTL-compatible output bits plus an overflow flag signal. Overflow can be used in conjunction with 3-state output controls to stack multiple MN5909's for higher resolution applications.

The MN5909 is available for commercial/industrial applications in both ceramic side-brazed and plastic DIP packages. The MN5909H/B is also available with Environmental Stress Screening for application in military/aerospace systems.

Model	Package	Temp. Range	Mil
MN5909PD	Plastic DIP	0°C to +70°C	No
MN5909CD	Ceramic DIP	0°C to +70°C	No
MN5909PDE	Plastic DIP	−25°C to +85°C	No
MN5909CDE	Ceramic DIP	−25°C to +85°C	No
MN5909CDH	Ceramic DIP	−55°C to +125°C	No
MN5909CDH/B	Ceramic DIP	−55°C to +125°C	Yes

APPLICATIONS

Video

RADAR Systems

Pulse Measurement Systems

Infrared Imaging

Communications

High-Speed Digitizers

EW and ECM Systems

This data sheet contains preliminary information regarding the MN5909. Please contact the factory for up-to-date performance and product information.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN5909 6-Bit, 100MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN5909PD, CD	0°C to +70°C
MN5909PDE, CDE	−25°C to +85°C
MN5909CDH, CDH/B	−55°C to +125°C
Storage Temperature Range	
MN5909PD, PDE	−65°C to +100°C
MN5906CD, CDE, CDH, CDH/B	−65°C to +150°C
$+V_{DD}$ Supply (Pins 5, 6, 7)	−0.5 to +7.0 Volts
Digital Inputs (Pins 3, 4, 19, 20)	−0.5 to $+V_{DD}$ +0.5 Volts
Analog Input (Pin 9)	−0.5 to $+V_{DD}$ +0.5 Volts

ORDERING INFORMATION

PART NUMBER — MN5909 CD H/B

Select suffix "PD" for plastic DIP or "CD" for ceramic DIP.

Standard "PD" and "CD" are specified for 0°C to +70°C operation.

Add "E" suffix to either "PD" or "CD" models for specified −25°C to +85°C operation.

Add "H" suffix to "CD" models for specified −55°C to +125°C operation.

Add "/B" suffix to "CDH" models for Environmental Stress Screening.

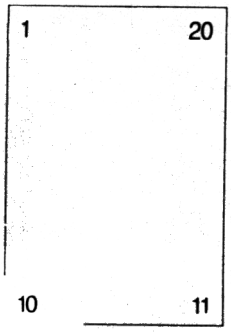
SPECIFICATIONS (T_A = +25°C, $+V_{DD}$ = +5V, V_{REF+} = +2.75V, V_{REF-} = 0.0V, f_{CLK} = 100 MHz unless otherwise indicated)

	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT				
Input Voltage Range		0 to $+V_{REF}$		Volts
Input Capacitance		12		pF
Full Power Bandwidth		100		MHz
REFERENCE INPUTS				
Reference Voltage (V_{REF+},)		+2.75		Volts
Reference Ladder Resistance		90		Ω
Reference Ladder Tempco		0.3		Ω/°C
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
			+5	μA
			−5	μA
	+4.5			Volts
			+0.4	Volts
Integral Linearity Error		± ¾	± 1	LSB
Differential Linearity Error		± ¼	± ¾	LSB
No Missing Codes		Guaranteed		
DYNAMIC PERFORMANCE				
Conversion Rate		100		MHz
Aperture Delay		5		nsec
Output Propagation Delay	10	14	20	nsec
AC LINERITY				
Signal-to-(Noise and Distortion)				
f_{AIN} = 1MHz	34			dB
f_{AIN} = 10MHz	33			dB
Spurious Free Dynamic Range:				
f_{AIN} = 1MHz	43			dB
f_{AIN} = 10MHz	37			dB
POWER SUPPLY				
Power Supply ($+V_{DD}$ Supply)	+4.75	+5	+5.25	Volts
Power Supply Drain ($+V_{DD}$ Supply)		+40		mA

SPECIFICATION NOTES:

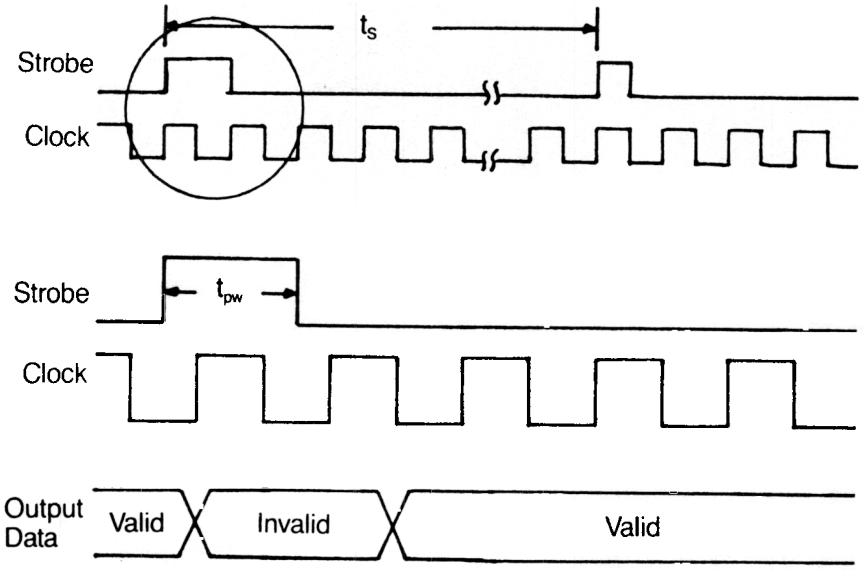
1. Measured while operating at specified conversion rate with an auto-zero pulse repitition rate of 40kHz.
2. Integral Linearity Error is specified using transfer function endpoints.
3. Differential Linearity Error measurements are based on code transitions.

PIN DESIGNATIONS



1	V_{REF-}	20	Conversion Clock
2	V_{REF+}	19	Auto-zero Strobe
3	3-State Control (CS2)	18	Ground
4	3-State Control ($\overline{CS1}$)	17	Overflow
5	$+V_{DD}$ Supply	16	Bit 1 (MSB)
6	$+V_{DD}$ Supply	15	Bit 2
7	$+V_{DD}$ Supply	14	Bit 3
8	Ground	13	Bit 4
9	Analog Input	12	Bit 5
10	R_{MID}	11	Bit 6 (LSB)

PACKAGE OUTLINE

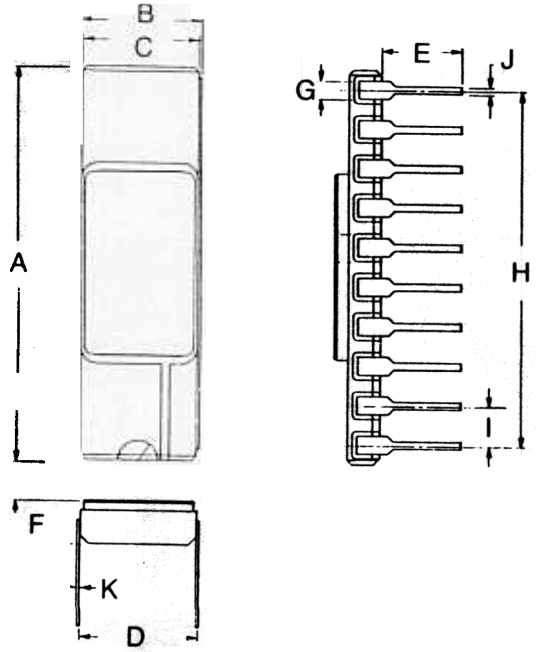


TIMING NOTES:

1. t_{pw} must be high for one full clock cycle. Strobe may be asynchronous with Clock.
2. t_s = Strobe repetition rate = 40kHz.
3. Output data is indeterminate when strobe = "1" Output data returns valid upon falling edge of clock after strobe returns to "0".

MN5909

PIN DESCRIPTIONS



	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	1.010	0.990	25.65	25.15
B	0.300	0.320	7.62	8.13
C	0.285	0.305	7.24	7.75
D	0.295	0.305	7.49	7.75
E	0.125	0.200	3.18	5.08
F	—	0.123	—	3.12
G	0.048	0.052	1.22	1.32
H	0.900 BASIC		22.86 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.016	0.020	0.41	0.51
K	0.005	0.015	0.13	0.38

Package shown is for MN5909CD, CDE, CDH and CDH/B. Please contact factory for information regarding dimensions and availability of "PD" and "PDE" models.

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN5909 6-Bit, 100MHz CMOS Flash A/D converter, operates in a transparent fashion with an externally supplied asynchronous, auto-zero pluse. Typical CMOS Flash A/D converters auto-zero the sampling comparators during each clock cycle. The MN5909's unique architecture utilizes an externally-applied asynchronous pulse to auto-zero the sampling comparators every 40,000 conversions (typically).

The auto-zero pulse must be high during a low-to-high transition of the applied conversion clock and must remain high for a minimum of one clock cycle. It is recommended that a 40kHz repetition rate of the auto-zero pulse be utilized.

Output data present during the auto-zero phase should be considered invalid.

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5909 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. The pinout of the MN5909 has been carefully chosen to maintain as much separation of digital and analog signals as possible. The use of ground and power planes and signal shielding is highly recommended. It is recommended that bypass capacitors of 0.01 and 0.001 μF should used and located as close to the device as possible.

It is also recommended that circuits interfacing with the MN5909 (such as data latches, etc.) be located within 2 inches of the device to avoid transmission line effects (rise and fall times of the MN5909 output drivers are 2nsec or less implying frequency components in the hundreds of MHz).

PIN DESCRIPTIONS

PIN	NAME	SYMBOL	DESCRIPTION
1, 2	Reference Inputs	$-V_{REF}$, $+V_{REF}$	Bottom and top of the reference resistor string. $-V_{REF}$ normally tied to GND, $+V_{REF}$ normally tied to +2.75 Volts.
3	3-State Control (Overflow Bit)	CS2	Overflow bit valid when CS2 = Logic "1". Output bits and overflow bit in high-impedance state when CS2 = Logic "0". See Truth Table.
4	3-State Control (Data Bits)	$\overline{CS1}$	Data bits valid when $\overline{CS1}$ = Logic "0". Data bits in high-impedance state when $\overline{CS1}$ = Logic "1". $\overline{CS1}$ is a "don't care" (X) when CS2 is a Logic "0". See Truth Table.
5, 6, 7	Power Supply	$+V_{DD}$	Connected to +5V Supply for normal operation.
8	Ground	GND	Connected to System Analog Ground plane.
9	Analog Input	A_{IN}	Connect analog input signal to be digitized. Nominally 0V to $+V_{REF}$.
10	Reference Resistor Midpoint	R_{MID}	Midpoint tap to resistor ladder.
11,12,13 14,15,16	Data Output Bits	B6-B1	Digital Output Bits.
17	Overflow Bit	OF	Set to a Logic "1" when analog input exceeds $+V_{REF}$ -½LSB.
18	Ground	GND	Connected to System Analog Ground plane.
19	Strobe	STB	Externally-applied auto-zero strobe pulse.
20	Clock	CLK	Clock Input.

DIGITAL OUTPUT CODING

ANALOG INPUT	OF	MSB					LSB
$+V_{REF}$	1	1	1	1	1	1	
$+V_{REF}$ – ½LSB	ϕ	1	1	1	1	1	
$+V_{REF}$ – 1LSB	0	1	1	1	1	1	1
$+V_{REF}$ – 3/2LSB	0	1	1	1	1	1	ϕ
$+½V_{REF}$ + ½LSB	0	1	0	0	0	0	ϕ
$+½V_{REF}$ – ½LSB	0	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
$+½V_{REF}$ – 3/2LSB	0	0	1	1	1	1	ϕ
+½LSB	0	0	0	0	0	0	ϕ
0	0	0	0	0	0	0	0

Analog inputs indicated are the theoretical values for the transitions of codes indicated above. With the converter continuously converting, the output bit indicated as ϕ will change from Logic "0" to Logic "1" or vise versa as the input voltage passes through the indicated level.

TRUTH TABLE

$\overline{CS1}$	CS2	B1 - B6	OF
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	High-Z