

M81016P/FP/KP

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

DESCRIPTION

M81016 is octal D-type flip-flop driver by 20-pin package. It has 8 same circuit units which is composed of D-type flip-flop logic circuit and high voltage NchMOS output transistor. M81016 has a common direct clear input and a common clock input.

FEATURES

- Lineup with three packages
- High breakdown voltage ($BV_{DSX} \geq 40V$)
- Drain output current ($I_{DS(max)} = 200mA$)
- With input protection diodes
- Pin assignment of input-output flow through
- Wide operating temperature range ($T_a = -40$ to $+85^\circ C$)

APPLICATION

LED drive

FUNCTION

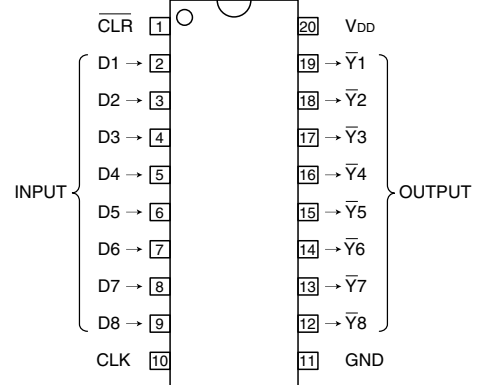
The common direct clear input and common clock input are connected to every circuit unit by the same way. Signal at the D inputs is transferred to $\bar{Y}$ outputs by D-type flip-flops on the positive-going edge of the clock pulse.

If $\overline{CLR}$ is set to "L", outputs $\bar{Y}1$ - $\bar{Y}8$ will be altogether set to "H" regardless of D1-D8 and CLK.

The maximum drain current of an output is 200mA. The maximum between drain-source is 40V.

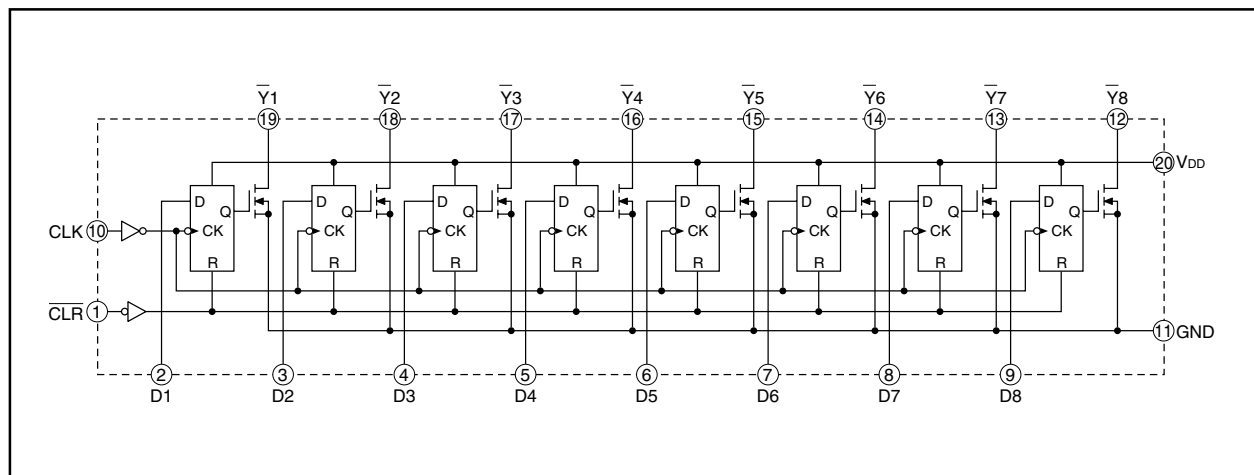
Moreover, M81016FP/KP can save space with mini-flat package.

PIN CONFIGURATION (TOP VIEW)



Package type 20P4B(P)
20P2N-A(FP)
20P2E-A(KP)

LOGIC DIAGRAM (POSITIVE LOGIC)



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FUNCTION TABLE (EACH CHANNEL)

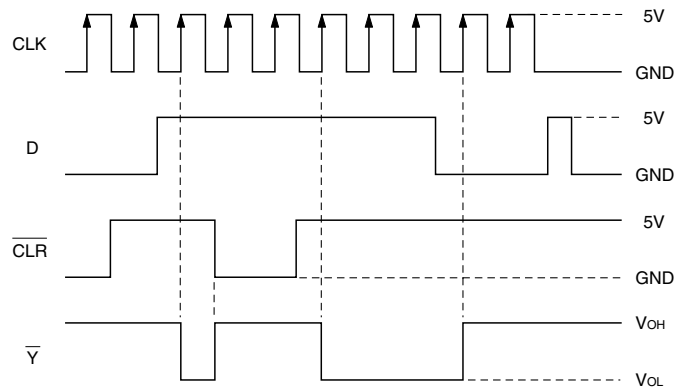
INPUT			OUTPUT : $\bar{Y}$
$\overline{\text{CLR}}$	CLK	D	
L	X	X	H
H	$\uparrow$	L	H
H	$\uparrow$	H	L
H	L	X	Latched
H	$\downarrow$	X	Latched

H : High level

L : Low level

X : Irrelevant

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Conditions		Ratings	Unit
VDD	Supply voltage			7	V
VDS	Drain-to-source voltage	Output, H		−0.5 ~ +40	V
VI	Input voltage			−0.5 ~ VDD	V
IDS	Drain output current	Current per circuit output, L		200	mA
Pd	Power dissipation	Ta = 25°C, when mounted on board	M81016P	1.47	W
			M81016FP	1.10	
			M81016KP	0.68	
Topr	Operating temperature			−40 ~ +85	°C
Tstg	Storage temperature			−55 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, $T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Conditions	Limits			Unit
			min	typ	max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{DS}	Drain-to-source voltage		0	—	40	V
V_{IH}	"H" input voltage		$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	"L" input voltage		0	—	$0.3V_{DD}$	V
I_{DS}	Drain output current (Current per 1 circuit when 8 circuits are coming on simultaneously)	P	Duty Cycle no more than 45%	0	200	mA
			Duty Cycle no more than 100%	0	135	
		FP	Duty Cycle no more than 34%	0	200	
			Duty Cycle no more than 100%	0	120	
		KP	Duty Cycle no more than 18%	0	200	
			Duty Cycle no more than 100%	0	95	
V_{IN}	Input voltage		0	—	V_{DD}	V
t_r, t_f	Rise time, Fall time, drain output	$V_{DD} = 4.5\text{V}$	0	—	500	ns
t_{su}	Setup time before CLK $\uparrow$	$V_{DD} = 4.5\text{V}$	20	—	—	ns
t_h	Hold time, data after CLK $\uparrow$	$V_{DD} = 4.5\text{V}$	5	—	—	ns
t_w	Pulse duration	$V_{DD} = 4.5\text{V}$	40	—	—	ns
f	Clock frequency	$V_{DD} = 4.5\text{V}$	—	—	20	MHz

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V_{DD} = 5V$, $T_a = 25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
$V_{(BR)DSX}$	Drain-source breakdown voltage	$I_{DS} = 1mA$	40	—	—	V
I_{DSX}	Drain-source leakage current	$V_{DS} = 40V$	—	0.002	5	μA
I_{IH}	"H" input current	$V_{DD} = 5.5V$, $V_I = 5.5V$	—	0.005	1	μA
I_{IL}	"L" input current	$V_{DD} = 5.5V$, $V_I = 0V$	—	0.005	-1	μA
I_{CC}	Supply current	$V_{DD} = 5.5V$ $V_I = 5.5V$ or $0V$	All outputs off	—	0.005	5
			All outputs on	—	0.005	5
V_{DS}	"L" output voltage	$I_{DS} = 100mA$, $V_{DD} = 4.5V$	—	0.25	0.38	V
		$I_{DS} = 200mA$, $V_{DD} = 4.5V$	—	0.51	0.77	
$R_{DS(on)}$	Drain-source on-state resistance	$I_{DS} = 100mA$, $V_{DD} = 4.5V$	—	2.5	3.8	Ω

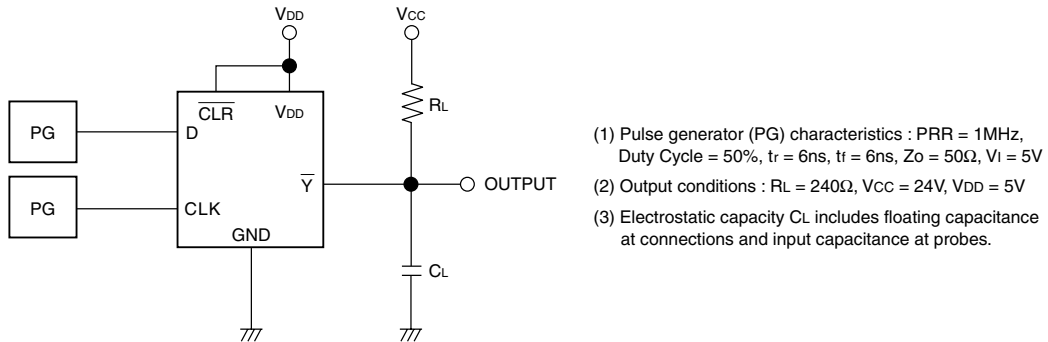
SWITCHING CHARACTERISTICS ($V_{DD} = 5V$, $T_a = 25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
tTLH	Low-level to high-level and high-level to low-level output transition time	CL = 30pF (Note 1)	—	10	—	ns
tTHL			—	3	—	ns
tPLH	Low-level to high-level and high-level to low-level output propagation time (CLK)		—	35	—	ns
tPHL			—	30	—	ns
tPLH(R)	Low-level to high-level output propagation time (CLR)		—	35	—	ns

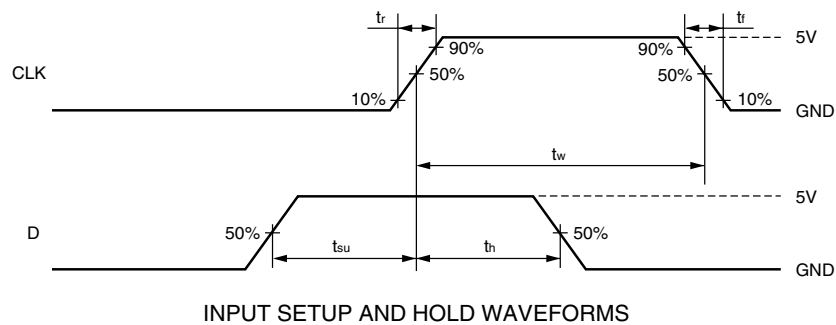
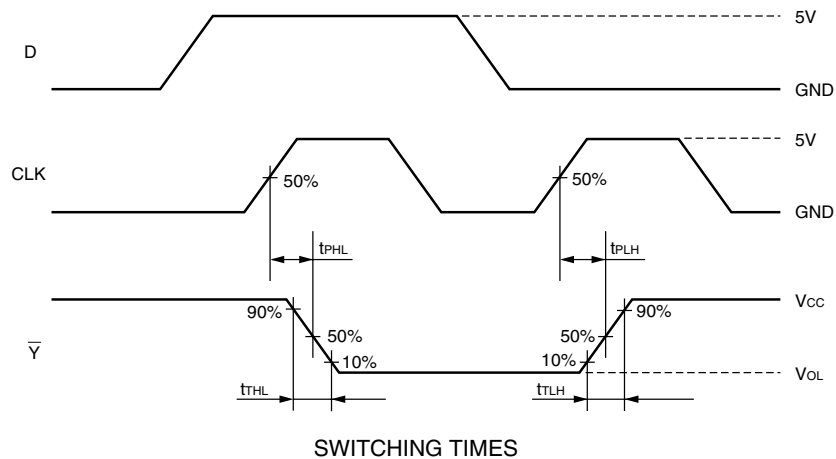
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NOTE 1 TEST CIRCUIT



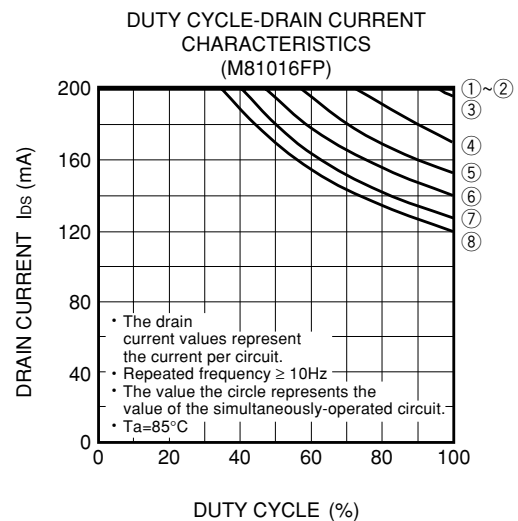
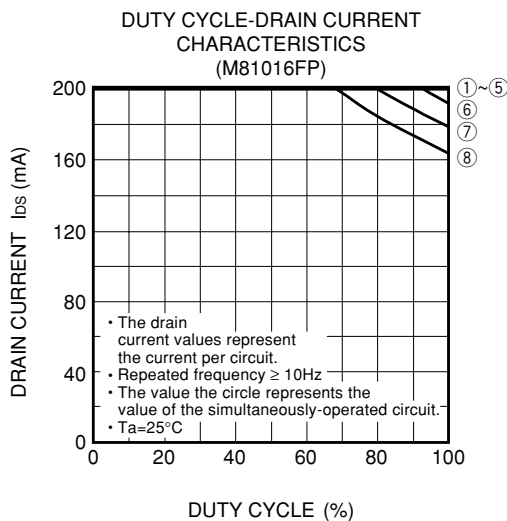
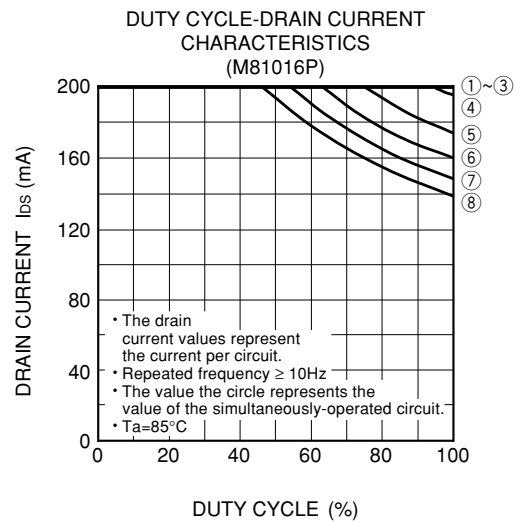
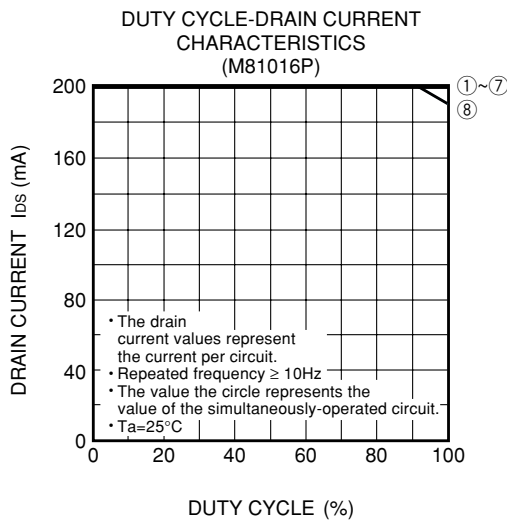
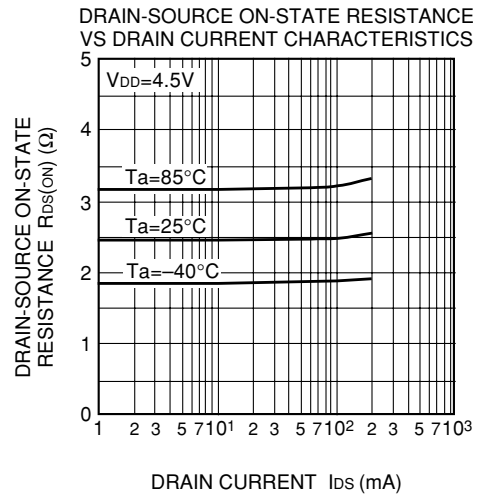
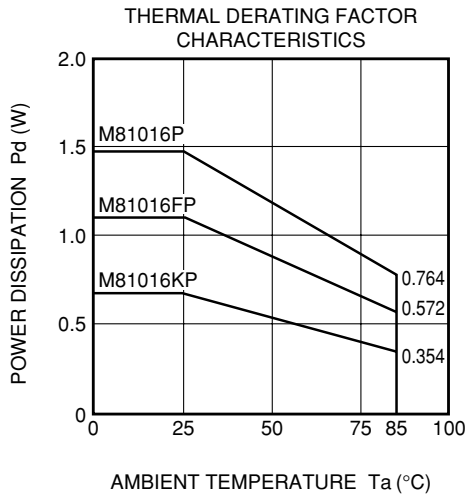
TIMING DIAGRAM



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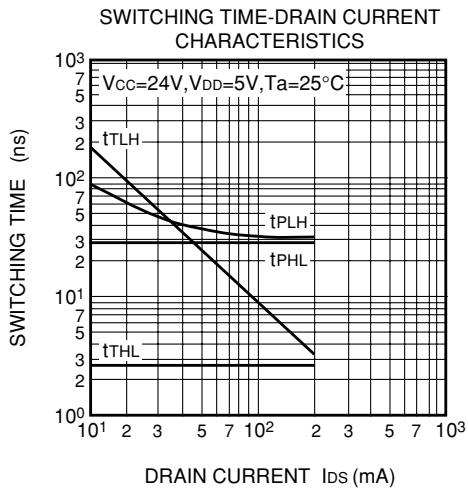
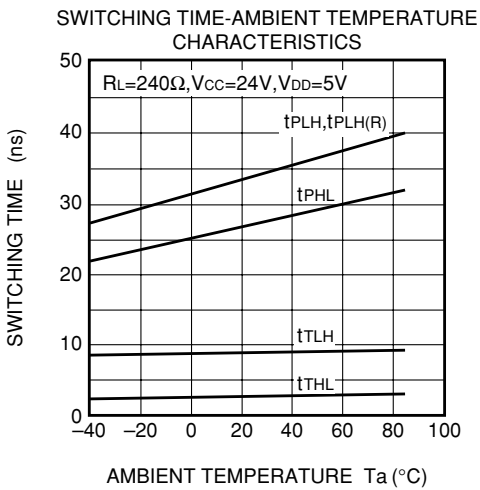
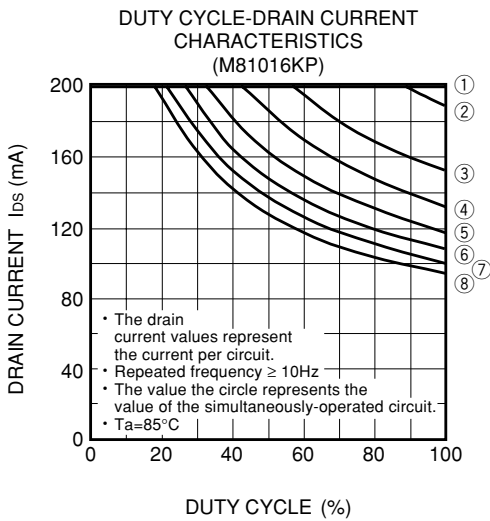
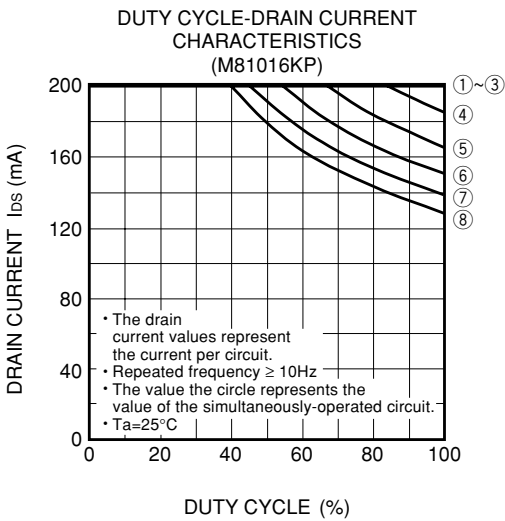
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TYPICAL CHARACTERISTICS



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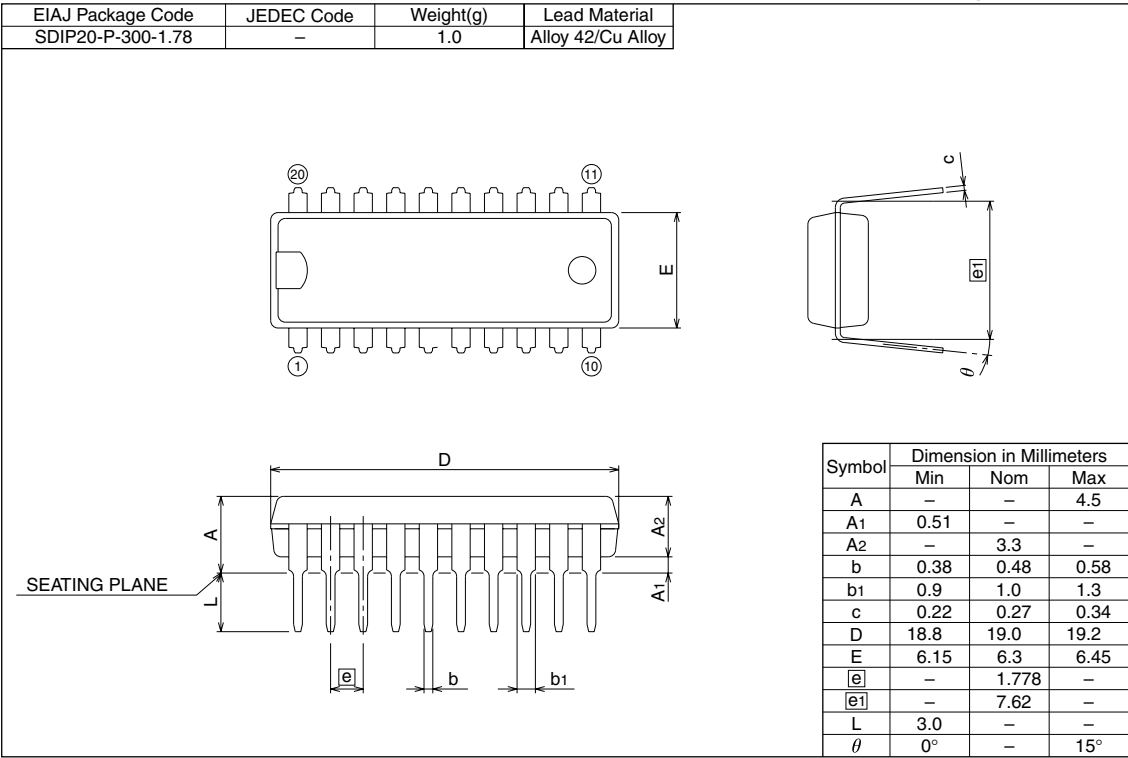


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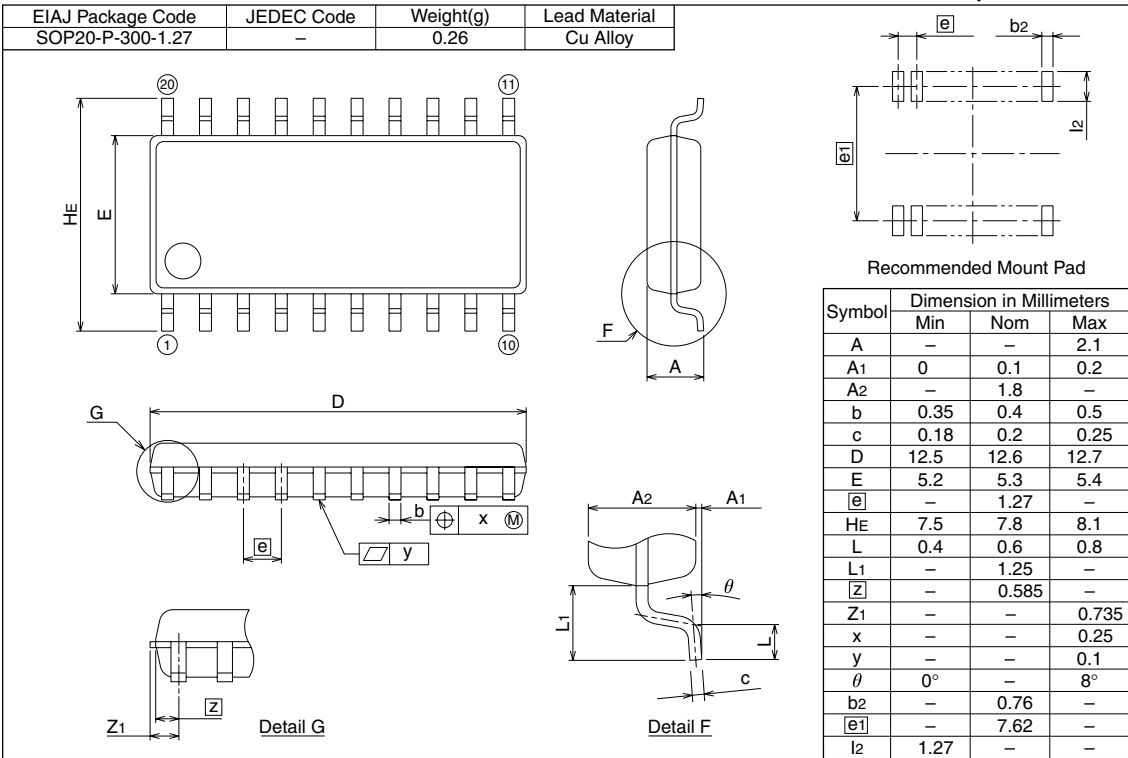
20P4B

Plastic 20pin 300mil SDIP



20P2N-A

Plastic 20pin 300mil SOP



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20P2E-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP20-P-225-0.65	—	0.08	Alloy 42

Plastic 20pin 225mil SSOP

