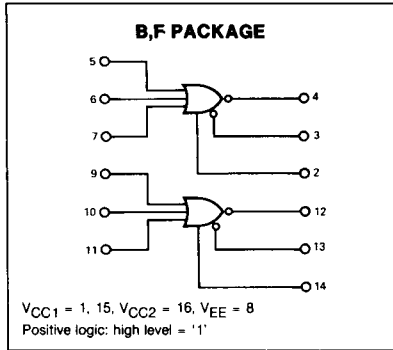


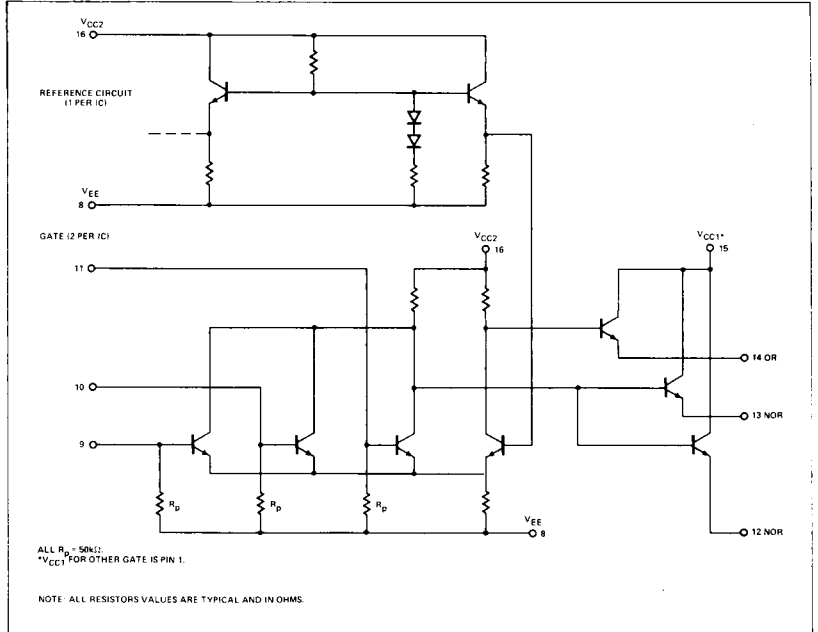
LOGIC DIAGRAM



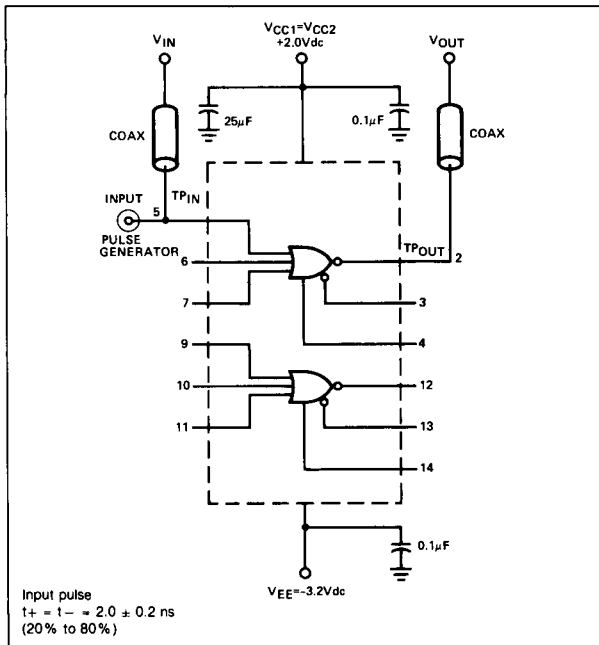
FEATURES

- Fast propagation delay = 2.4 ns TYP (all outputs loaded)
- Power dissipation = 150 mW/package TYP (no load)
- Very high fanout capability — can drive six 50 Ω lines
- High Z inputs — internal 50k Ω pulldowns
- High immunity from power supply variations: $V_{EE} = -5.2 V \pm 5\%$ recommended
- Open emitters for bussing and logic capability

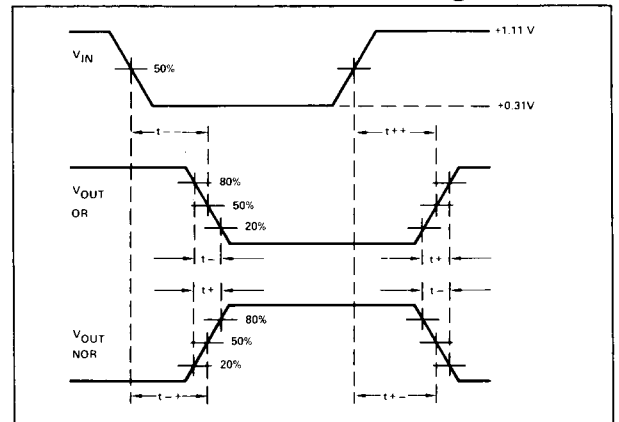
CIRCUIT SCHEMATIC



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25° C



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $< \frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. Pin 1 = Pin 15 = Pin 16 = $V_{CC} = 0$ V, Pin 8 = $V_{EE} = -5.2$ V.
6. Pin 1 = Pin 15 = Pin 16 = $V_{CC} = +2.0$ V, Pin 8 = $V_{EE} = -3.2$ V.