

MB89413

OUTLINE FONT GENERATOR 2 (OFGII)

DESCRIPTION

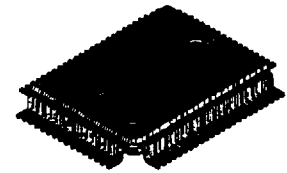
The OFGII is a large-scale integrated circuit (LSI) that draws an outline defined by lines and curves (cubic Bezier curve and cubic B-spline curve) and rasterizes an internally-filled image, which is generated in internal font expansion memory.

The OFGII can generate high-quality characters at high speed with equipment using outline fonts, such as a word processor or a page printer.

FEATURES

- **Upper Compatibility with MB89412 (OFG)**
Software and hardware for the OFG are available for the OFGII. The OFGII is distinguishable from the OFG by software.
- **Supports Cubic B-spline Curve, Cubic Bezier Curve and Straight Line**
A cubic B-spline curve, cubic Bezier curve, and straight line can be used as elements of an outline. The cubic B-spline curve supports three shapes.
- **Specifying Flatness Parameter and Minimum Dividing Number of Segment**
Flatness parameter that define the curve smoothness can be freely specified from 0 to 15. Also, the minimum dividing number of one curve segment can be selected from two, four, or eight. These two parameters control the quality of a curve and the processing speed.
- **Contains Font Expansion Memory**
The 128 x 128-dot (2048-byte) font expansion memory means that no external work area is required. If an image is larger than the font expansion memory, it can be generated by dividing it into several parts.
The font expansion memory can also serve as an 80 x 80 x 2 plane. In this case, the plane-to-plane logic operation function enables pattern filling.
- **Mapping onto Arbitrary Coordinates**
The font expansion memory can be mapped onto arbitrary coordinates over the range of -32767 to 32767. Clipping is performed for inputting outline data beyond the font expansion memory area to enable high-speed processing.
- **Selecting Format for Inputting Coordinates**
Coordinates are input in 16-bit fixed-point format. The integer part can be selected from 16, 14, 12, or 8 bits.
- **Filling According to EVEN/ODD Rule**
Filling is performed according to the EVEN/ODD rule.
- **Selecting Characteristics of Digital Differential Analyzer (DDA)**
The DDA (linear interpolation) characteristics can be selected.
- **Input by Token Format**
All input (commands, parameters and coordinate data) is by the token format.
- **Twin-bus Configuration**
There are two 16-bit buses: the system bus for input the token, and the image bus for reading the generated image.
- **Two Read Methods**
There are two methods for reading from the font expansion memory: 'random access mode' by addressing, and 'sequential read mode' in which the address is incremented automatically.
The output area can be specified for sequential read mode.

80-LEAD PLASTIC QFP
(FPT-80P-M06)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

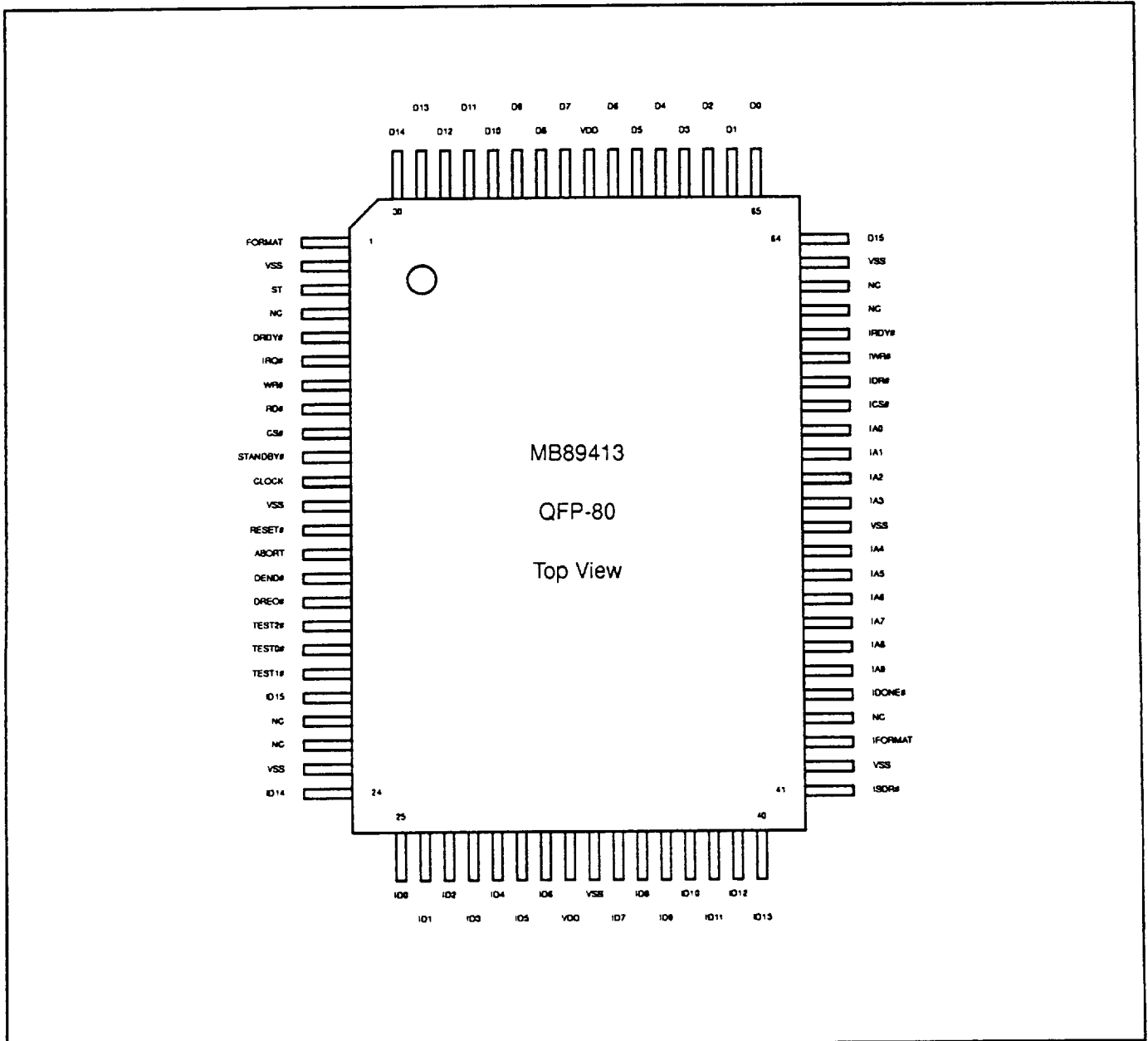
FEATURES

- Read-with-Fill and Read-with-Clear
'Read-with-Fill' reads an image with filling, and 'read-with-clear' automatically clears the read word to 0. These functions can be selected in sequential read mode.
- Straight-line Coordinates Output
Outline coordinates composed of straight-line segments can be output.
- Interrupt Function
Interrupt request signal can be output by various interrupt sources.
- Standby Function
Power can be saved by the standby pin.
- Performance (at 20 MHz)
 - 3000 to 5000 characters/s (Alphanumeric characters: 64 x 64)
 - 1500 to 3000 characters/s (Kanji: 64 x 64)

Note: Depends on character design and data form.

PIN ASSIGNMENT

- MB89413 Pin Assignment

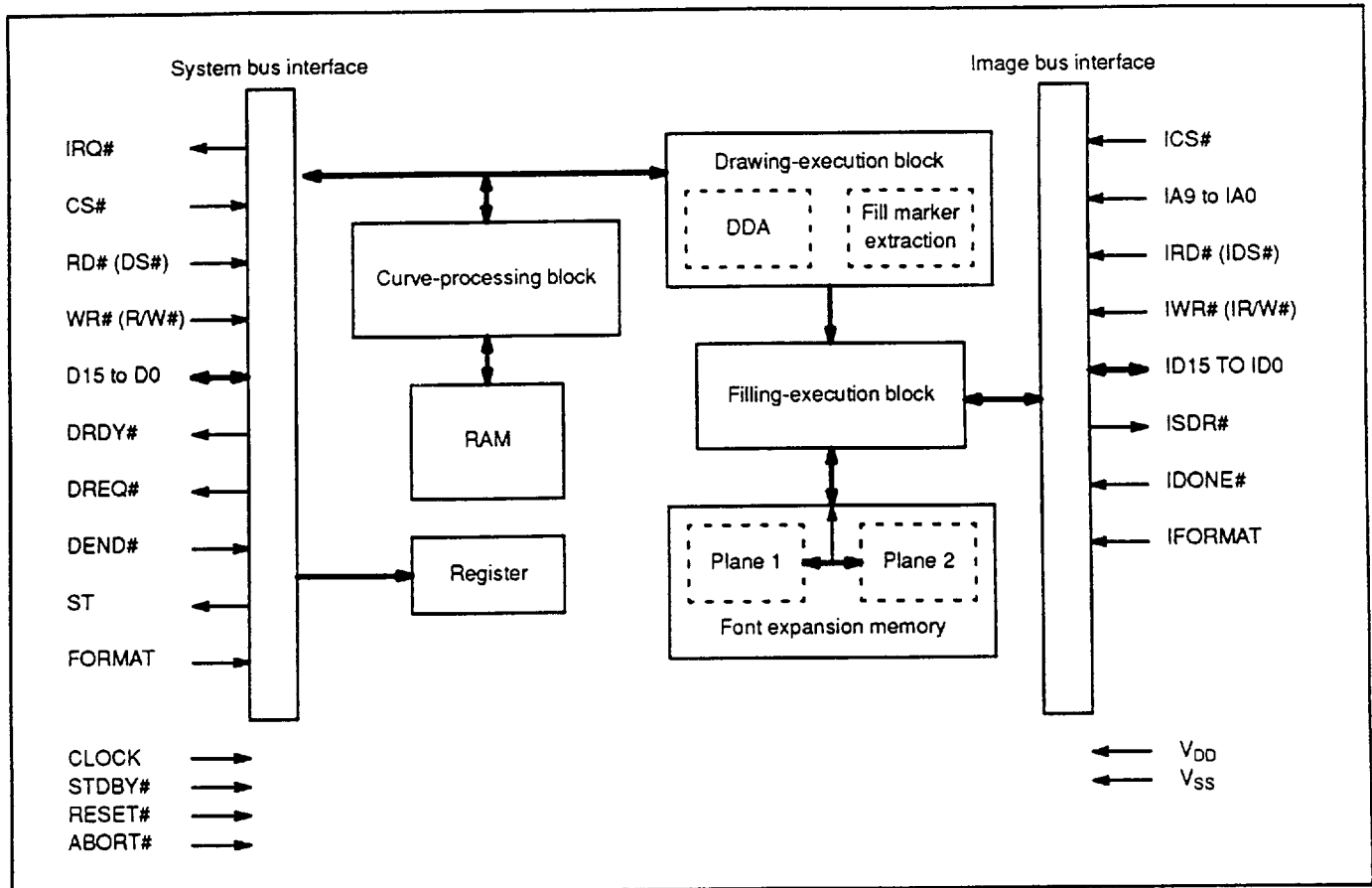


MB89413

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	FORMAT	21	NC	41	ISDR#	61	NC
2	V _{SS}	22	NC	42	V _{SS}	62	NC
3	ST	23	V _{SS}	43	IFORMAT	63	V _{SS}
4	NC	24	ID14	44	NC	64	D15
5	DRDY#	25	ID13	45	IDONE#	65	D14
6	IRQ#	26	ID12	46	IA9	66	D13
7	WR#(R/W#)	27	ID11	47	IA8	67	D12
8	RD#(DS#)	28	ID10	48	IA7	68	D11
9	CS#	29	ID9	49	IA6	69	D10
10	STDBY#	30	ID8	50	IA5	70	D9
11	CLOCK	31	ID7	51	IA4	71	D8
12	V _{SS}	32	V _{SS}	52	V _{SS}	72	D7
13	RESET#	33	V _{DD}	53	IA3	73	V _{DD}
14	ABORT#	34	ID6	54	IA2	74	D6
15	DEND#	35	ID5	55	IA1	75	D5
16	DREQ#	36	ID4	56	IA0	76	D4
17	TEST2#	37	ID3	57	ICS#	77	D3
18	TEST0#	38	ID2	58	IRD#(IDS#)	78	D2
19	TEST1#	39	ID1	59	IWR#(IRW#)	79	D1
20	ID15	40	ID0	60	IRDY#	80	D0

- Pins marked with NC are open.
- Pins marked with V_{DD} or V_{SS} are connected to the power supply or ground, respectively.
- Pins marked with TEST0#, TEST1# and TEST2# are open or pull-up.

BLOCK DIAGRAM



- **System bus interface**

System bus interface analyzes input tokens, and controls the chip. The internal 5-word token buffer stores input tokens.

- **Register**

This register is where various parameters are stored.

- **Curve-processing block**

This block approximates the curve shape to straight-line segments when a cubic Bezier curve or cubic B-spline curve is input.

- **Drawing-execution block**

This block performs the linear interpolation (DDA) and extract the fill markers required for filling.

- **Filling-execution block**

This block draws the fill markers extracted by drawing-execution block, fills the inside of the drawn fill markers, and controls the font expansion memory.

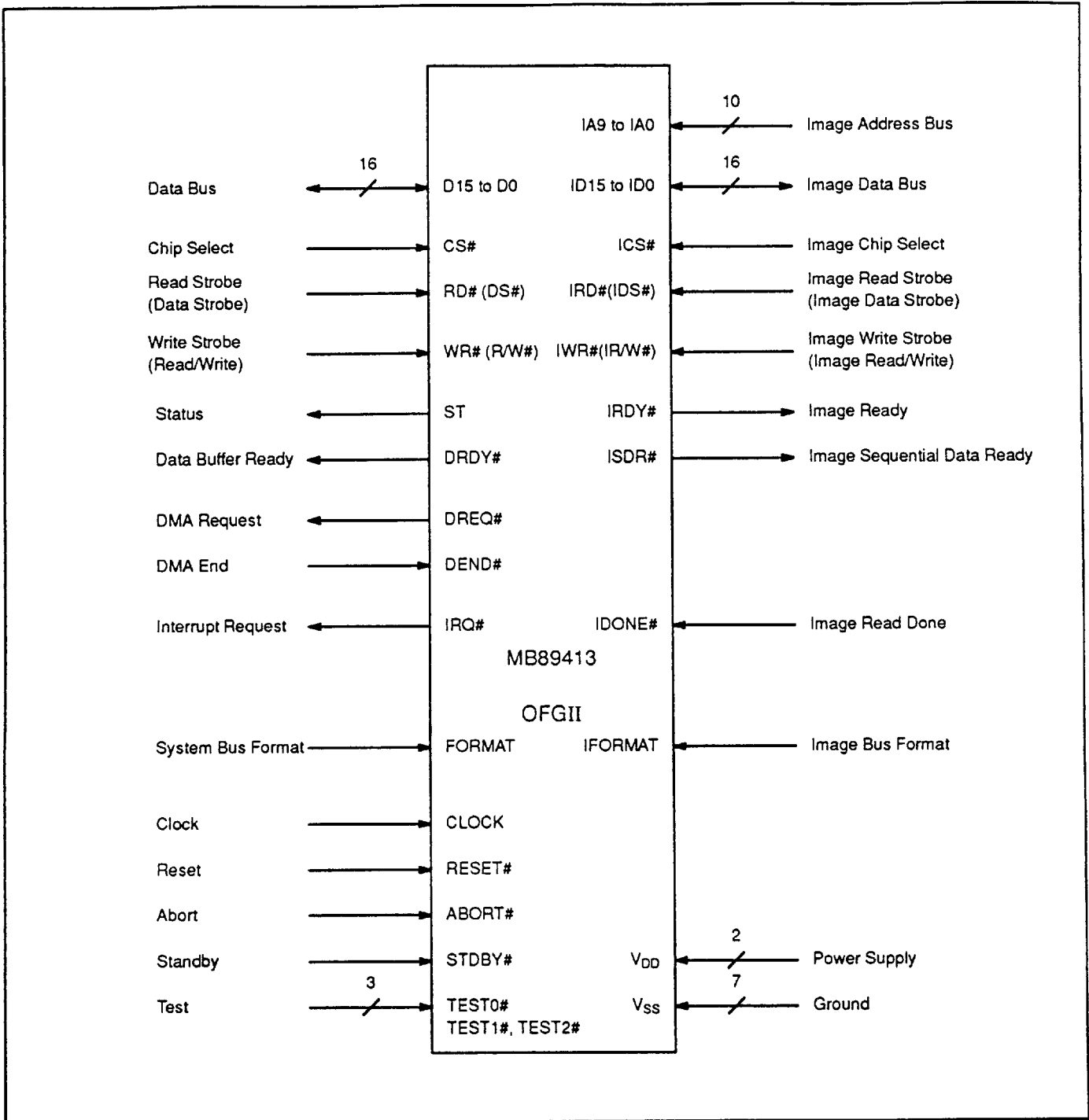
- **Font expansion memory**

This memory (RAM) is the area where the image is generated. A 128 x 128 x 1 plane or 80 x 80 x 2 plane can be selected.

- **Image bus interface**

Image bus interface is used when reads the image generated in the font expansion memory.

SIGNAL LINES



PIN DESCRIPTION

Pin No.	Pin Name	Signal Name	I/O	Function
11	CLOCK	Clock	I	This is used to input the Clock signal.
13	RESET#	Reset	I	This is used to input the Reset signal. Input of the Reset signal resets the internal state (set parameters are reset).
14	ABORT#	Abort	I	This is used to input the Abort signal. Input of the Abort signal resets the internal state (set parameters are stored).
3	ST	Status	O	This pin goes High during the operating or when the font expansion memory is connected to the image bus.
64 to 72, 74 to 80	D15 to D0	Data Bus	I/O 3state	These are used to input/output data to/from the system bus.
9	CS#	Chip Select	I	This is used to input the Select signal to access the system bus.
8	RD#	Read Strobe	I	This is used to input the Read Strobe signal to the system bus (when FORMAT pin is Low).
	DS#	Data Strobe	I	This is used to input the Data Strobe signal to the system bus (when FORMAT pin is High).
7	WR#	Write Strobe	I	This is used to input the Write Strobe signal to the system bus (when FORMAT pin is Low).
	R/W#	Read/Write	I	This is used to input the Read/Write signal to the system bus (when FORMAT pin is High).
5	DRDY#	Data Buffer Ready	O	This is used to output signal indicating that data can be written to the system bus.
16	DREQ#	DMA Request	O	This pin function as the same as the DRDY# pin when the DMA request function is set.
15	DEND#	DMA End	I Pull-up	This is used to input signal canceling the DMA request function.
6	IRQ#	Interrupt Request	O	This is used to output the Interrupt Request signals according to the various interrupt sources.
1	FORMAT	System Bus Format	I	This is used to set the access signal functions (RD# or DS# and WR# or R/W#) at the system bus.

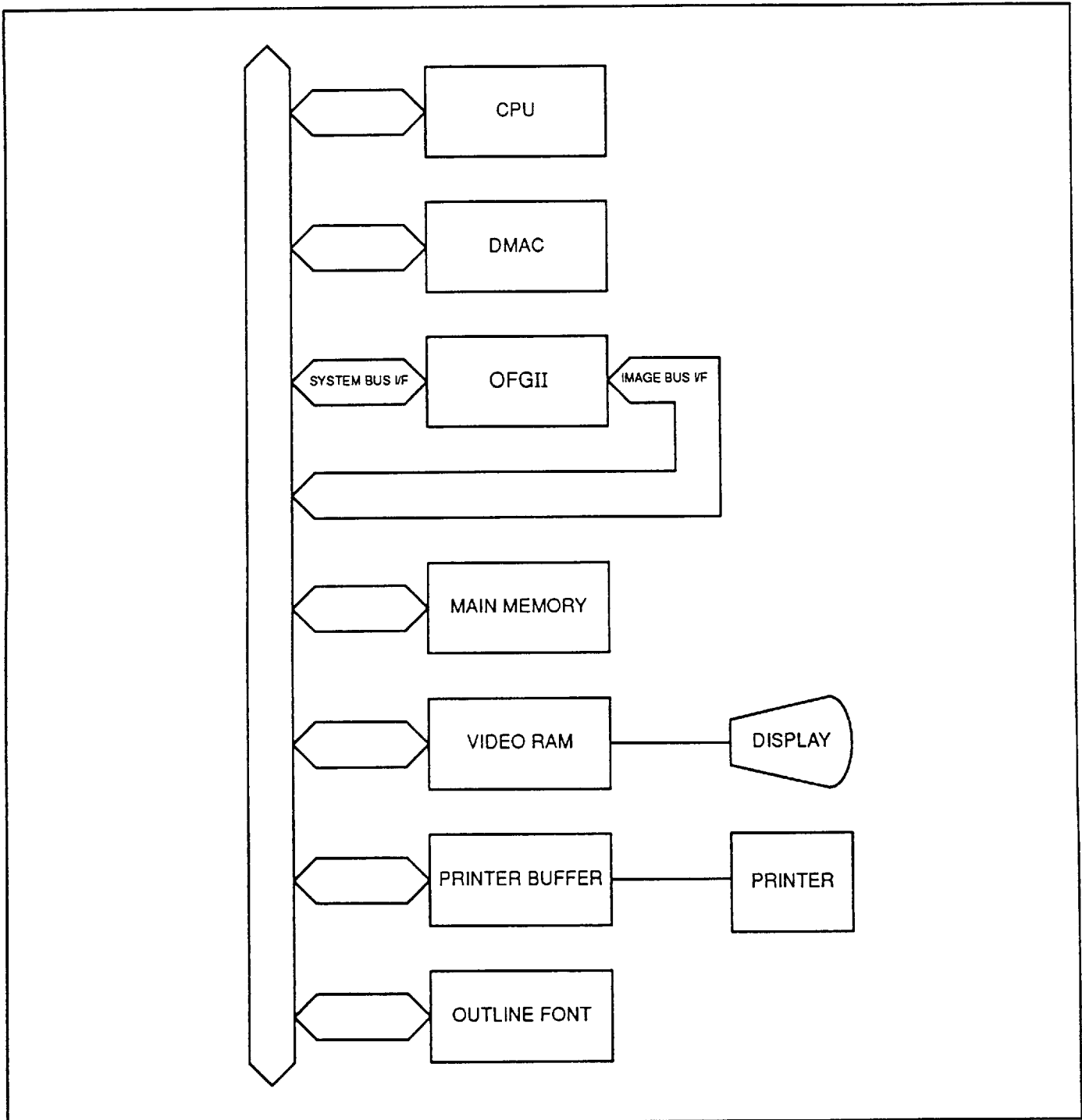
MB89413

Pin No.	Pin Name	Signal Name	I/O	Function
46 to 51, 53 to 56	IA9 to IA0	Image Address Bus	I Pull-up	These are used to input font expansion memory addresses.
20, 24 to 31, 34 to 40	ID15 to ID0	Image Data Bus	I/O 3state	These are used to input/output data to/from the image data bus.
57	ICS#	Image Chip Select	I	This is used to input the Select signal for accessing the font expansion memory.
58	IRD#	Image Read Strobe	I	This is used to input the Read Strobe signal to the image bus (when IFORMAT pin is Low).
	IDS#	Image Data Strobe	I	This is used to input the Data Strobe signal to the image bus (when IFORMAT pin is High).
59	IWR#	Image Write Strobe	I	This is used to input the Write Strobe signal to the image bus (when IFORMAT pin is Low).
	IR/W#	Image Read/Write	I	This is used to input the Read/Write signal to the image bus (when IFORMAT pin is High).
60	IRDY#	Image Ready	O	This is used to output signal indicating that the font expansion memory can be accessed.
41	ISDR#	Image Sequential Data Ready	O	This is used to output signal indicating that the next data in sequential reading of the font expansion memory is ready.
45	IDONE#	Image Read Done	I Pull-up	This is used to input signal terminating the font expansion memory access.
43	IFORMAT	Image Bus Format	I	This is used to set the access signal functions (IRD# or IDS# and IWR# or IR/W#) at the image bus.
10	STDBY#	Standby	I	This pin is asserted to enter the Standby (Power Save) mode.*
17 to 19	TEST0,1,2#	Test	I Pull-up	These are test pins (open or fixed High).
33,73	V _{DD}	Power Supply	—	
2, 12, 23, 32, 42, 52, 63	V _{SS}	Ground	—	
4, 21, 22, 44, 61, 62	NC	Open	—	

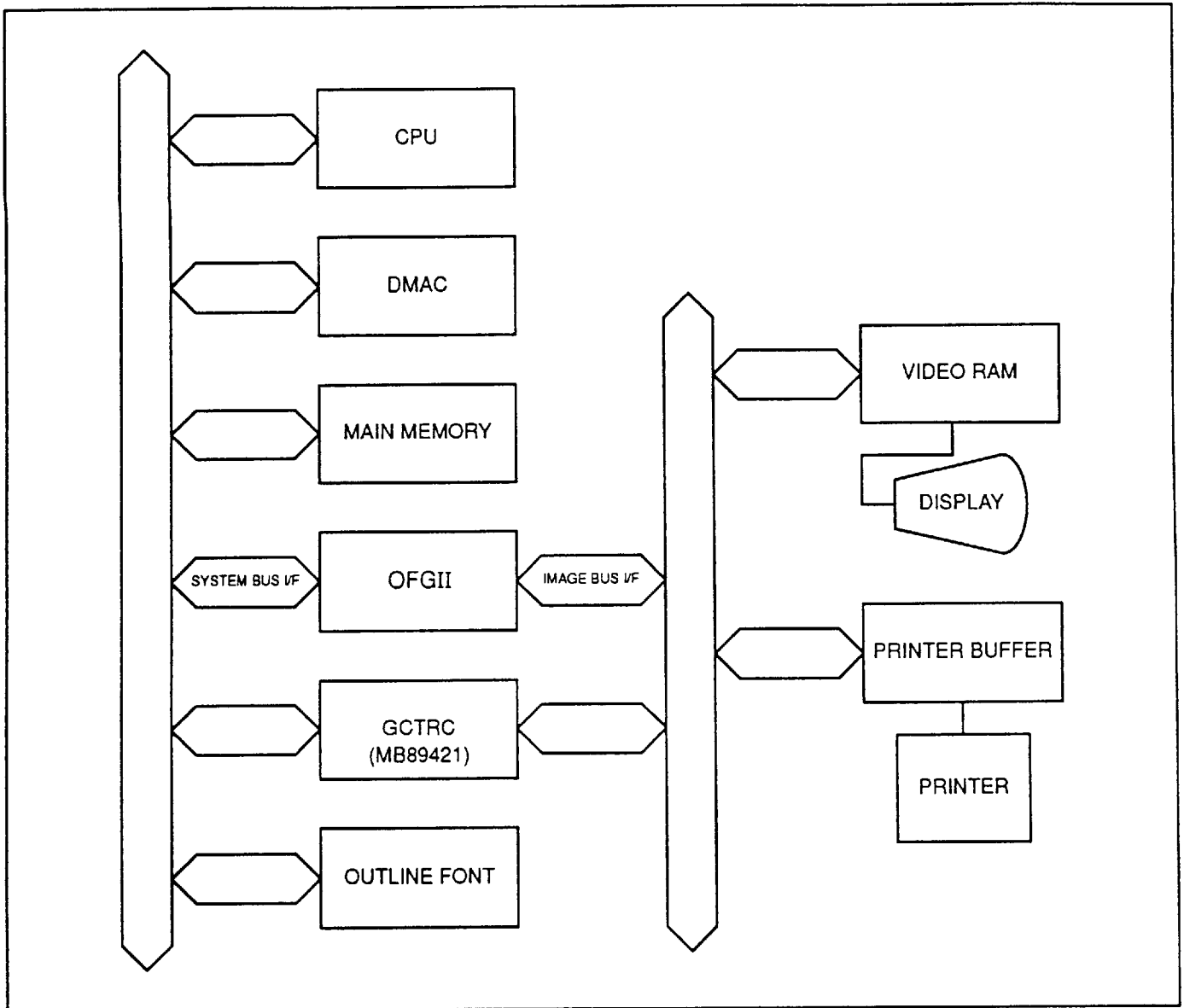
* The conditions (set values of various parameters and content of font expansion memory) are not assured after canceling Standby; be sure to reset.

SYSTEM CONFIGURATION

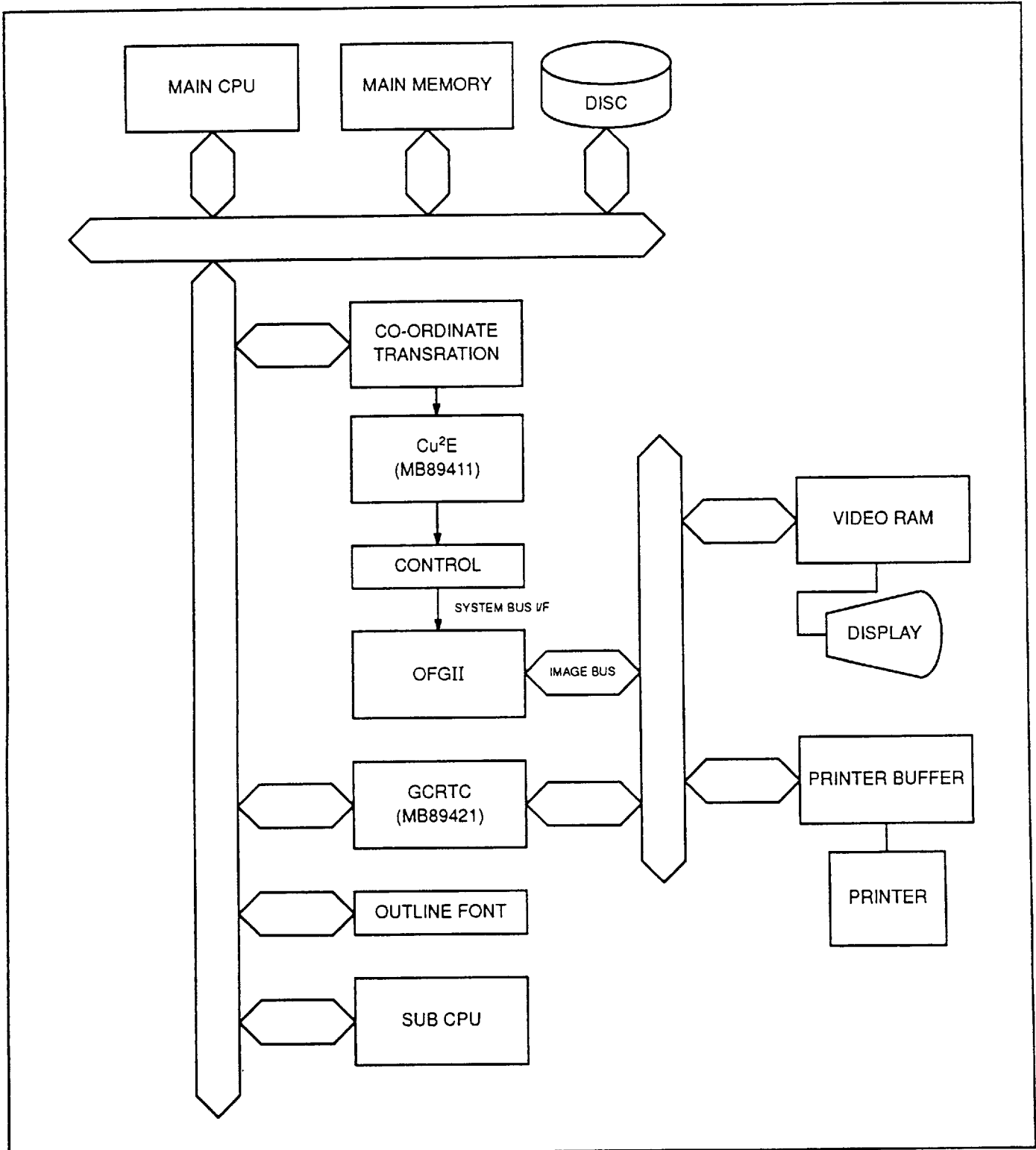
1. SMALL-SCALE SYSTEM



2. MEDIUM-SCALE SYSTEM



3. LARGE-SCALE SYSTEM



ELECTRICAL CHARACTERISTICS

1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	$V_{SS}^{*1} - 0.3$ to $+6.0$	V
Input voltage	V_I	$V_{SS}^{*1} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage	V_O	$V_{SS}^{*1} - 0.3$ to $V_{DD} + 0.3$	V
Total output current of system bus (D0 to D15)	ΣI_{OHS}	Max. -25	mA
	ΣI_{OLS}	Max. 40	mA
Total output current of image bus (ID0 to ID15)	ΣI_{OHI}	Max. -25	mA
	ΣI_{OLI}	Max. 40	mA
Operating temperature	T_{OP}	0 to $+70$	$^{\circ}C$
Storage temperature	T_{STG}	-40 to $+125$	$^{\circ}C$

*1: $V_{SS} = 0$ V

2. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings			Unit
		Min.	Typical	Max.	
Current voltage	V_{DD}	4.75	5.0	5.25	V
Ambient temperature	T_A	0	25	70	$^{\circ}C$

3. DC CHARACTERISTICS

Parameter	Symbol	Condition	Ratings			Unit
			Min.	Typical	Max.	
Input voltage	V_{IH1}	Input pins except RESET#, ABORT#, and STDBY# pins	2.4	—	V_{DD}	V
	T_{IL1}		V_{SS}	—	0.8	V
	V_{IH2}	RESET#, ABORT#, and STDBY# pins	3.0	—	V_{DD}	V
	T_{IL2}		V_{SS}	—	0.8	V
Output voltage	V_{OH}	$I_{OH} = -2 \text{ mA}$	4.0	—	V_{DD}	V
	T_{OL}	$I_{OL} = 3.2 \text{ mA}$	V_{SS}	—	0.4	V
Input leakage current	I_{LIN1}	$V_1 = V_{SS}$ to V_{DD} Pull-up resistor attached Input pins excluded	-10	—	10	μA
	I_{LIN2}	$V_1 = V_{SS}$ to V_{DD} Pull-up resistor attached Input pins	-300	—	10	μA
Input/output leakage current	I_{LIO}	$V_1 = V_{SS}$ to V_{DD}	-10	—	10	μA
Supply current	I_{DD}	Output pins: Open CLOCK: Input RESET# pin fixed to V_{SS} and others fixed to V_{DD} or V_{SS} . Pull-up resistor attached input pins: Open	—	—	50	mA
	I_{DDS}	Output pins: Open CLOCK: Input RESET# pin fixed to V_{SS} , STDBY# pin fixed to V_{SS} , and others fixed to V_{DD} or V_{SS} . Pull-up resistor attached input pins: Open	—	—	300	μA

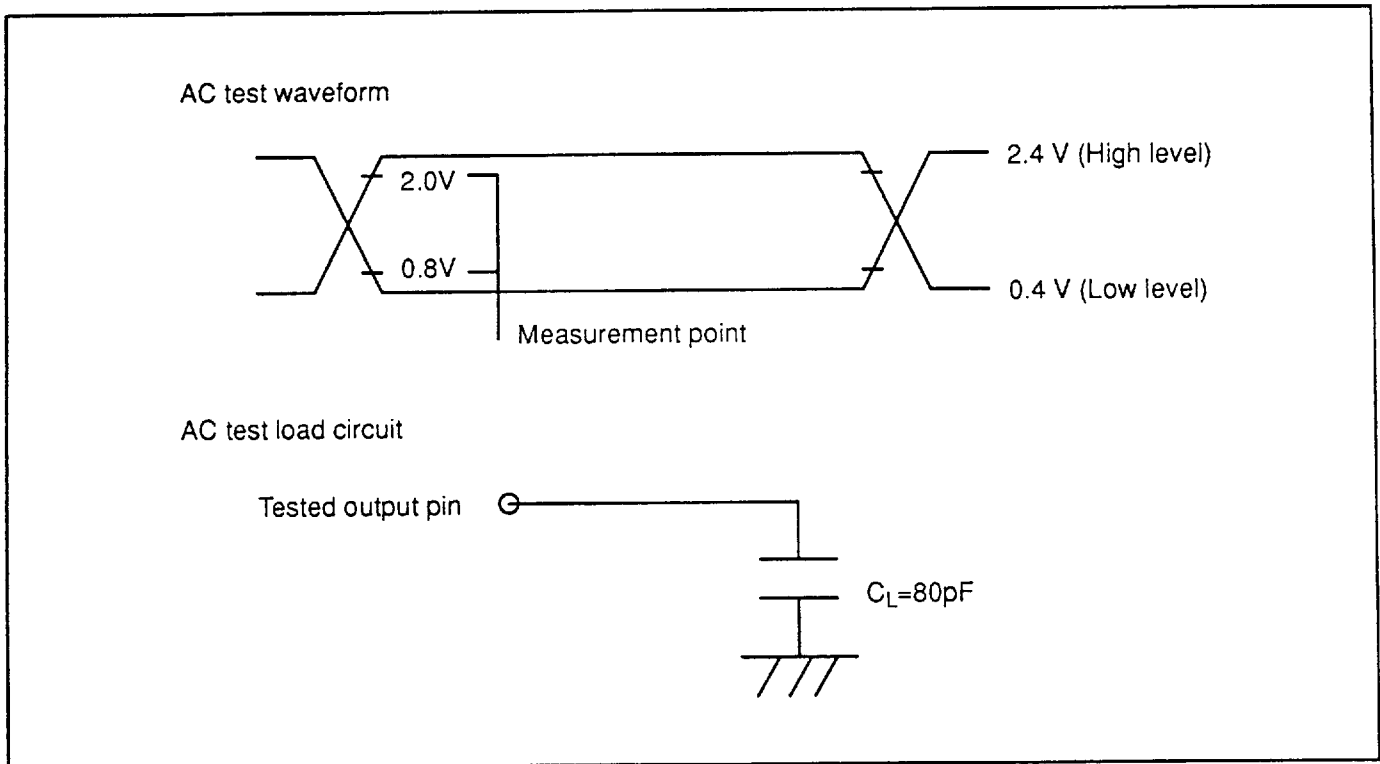
(V_{DD} = 5 V±5%, V_{SS} = 0V, T_A = 0 to 70 °C)

4. I/O PIN CAPACITANCE

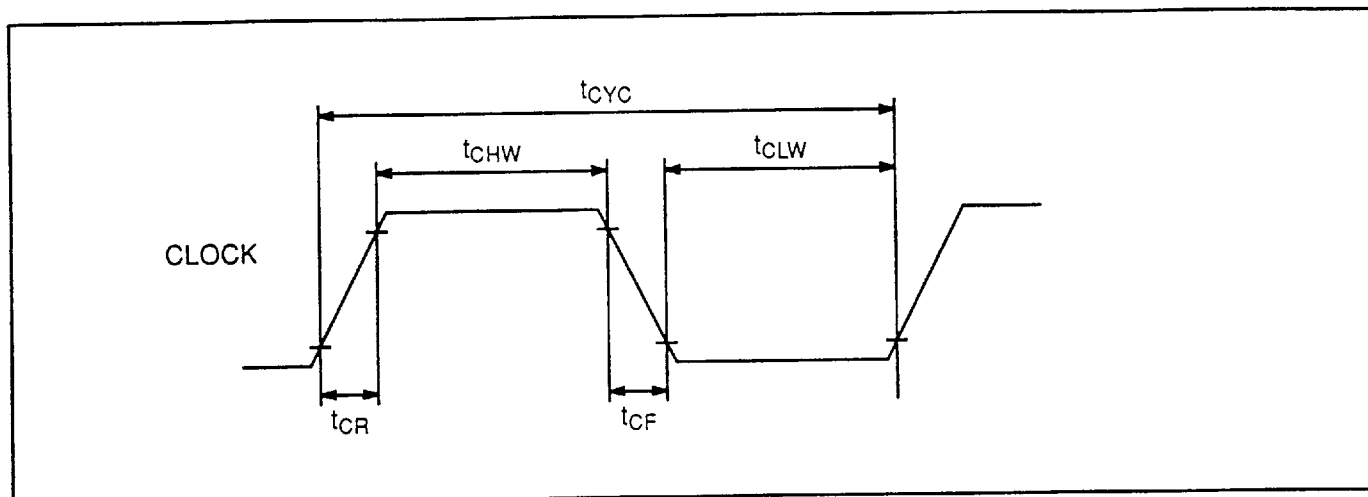
Parameter	Symbol	Measurement condition	Rating	Unit
Input pin	C_{IN}	$V_I = 0V$ $V_{DD} = 0V$ $f = 1MHz$	16 (max)	pF
Output pin	C_{OUT}		16 (max)	pF
I/O pin	C_{IO}		16 (max)	pF

5. AC CHARACTERISRICS

(1) I/O Level and Measurement Conditions

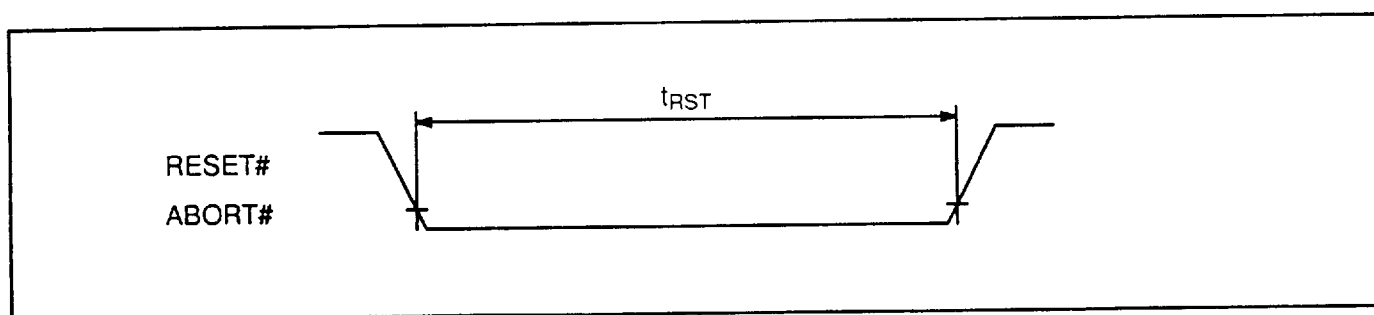


(2) Clock Input Waveform



Parameter	Symbol	Min. value (ns)	Max. value (ns)
CLOCK Cycle time	t_{cyc}	50	250
CLOCK Low level width	t_{clw}	20	—
CLOCK High level width	t_{chw}	20	—
CLOCK Rise time	t_{cr}	—	10
CLOCK Fall time	t_{cf}	—	10

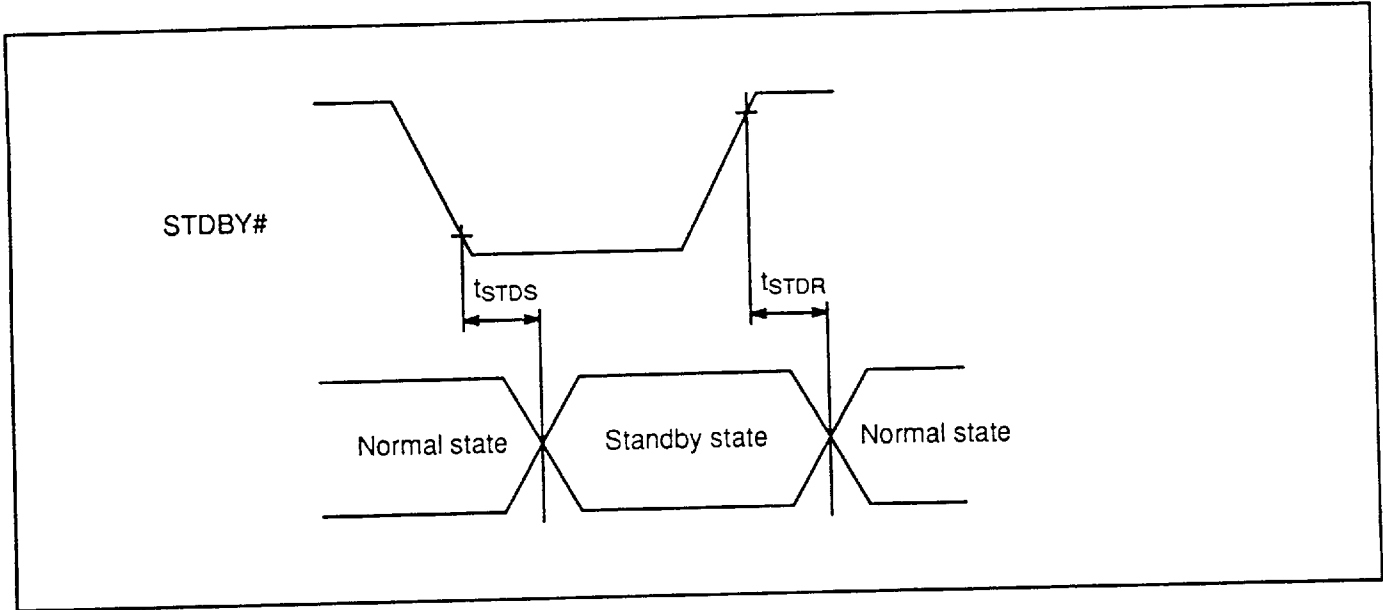
(3) RESET#/ABORT# Signal



Parameter	Symbol	Min. value (ns)	Max. value (ns)
RESET#/ABORT# Low level width	t_{rst}	$3t_{cyc}$	—

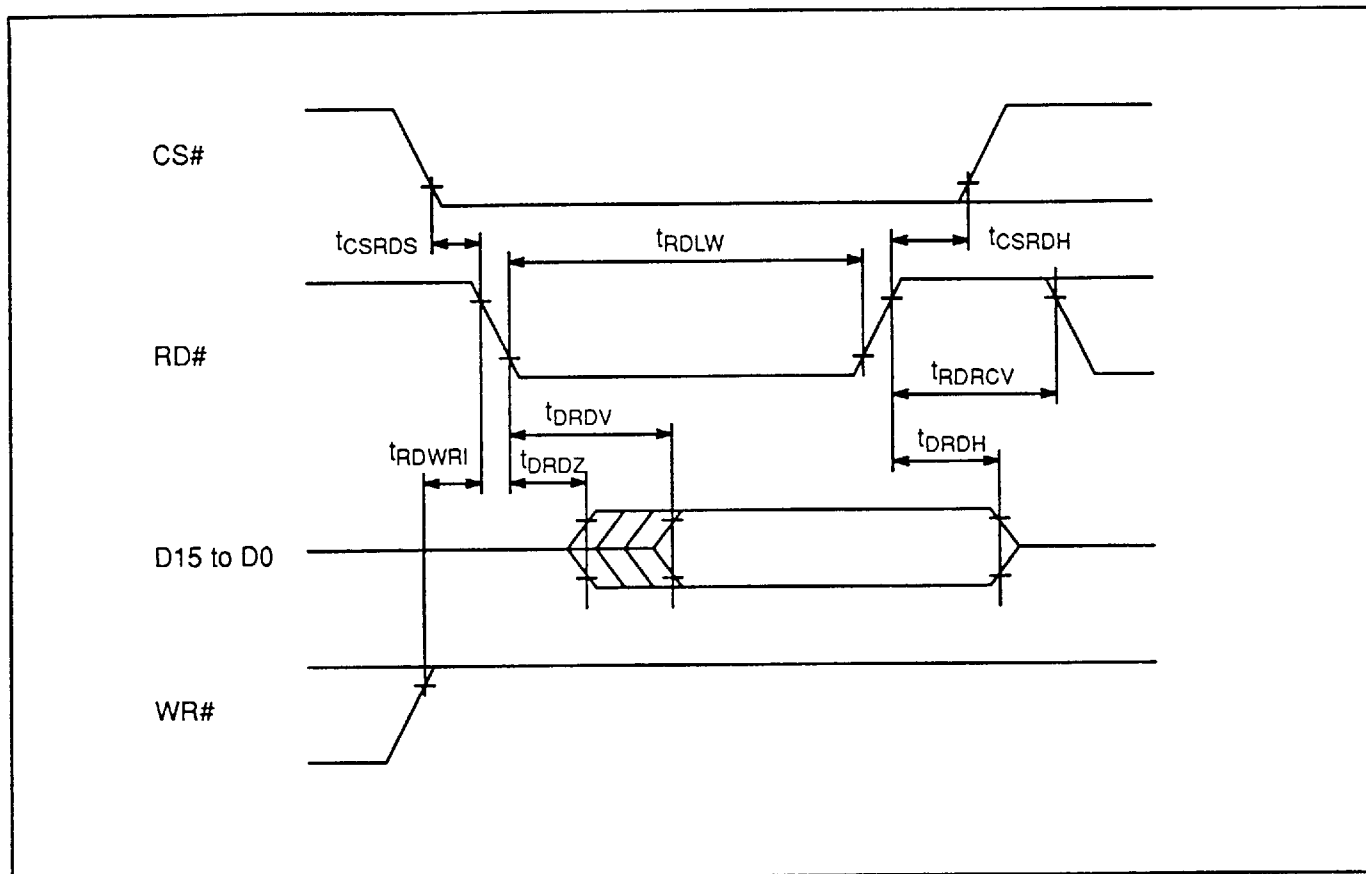
* The STDBY# pin is set High during input of the RESET#/ABORT# signal.

(4) STDBY# Pin Switching



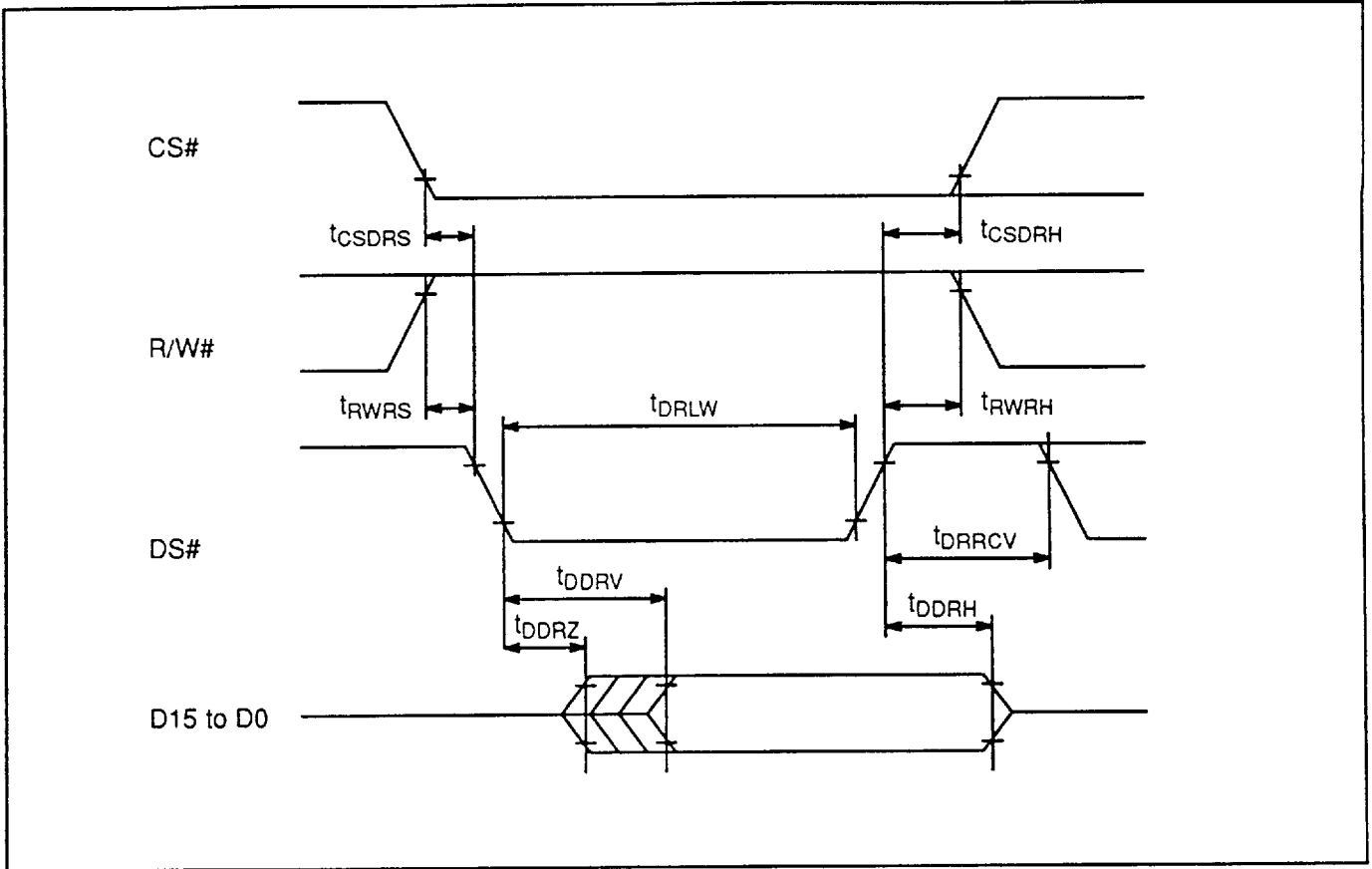
Parameter	Symbol	Min. value (ns)	Max. value (ns)
STDBY# Low to standby state	t_{STDS}	—	$2t_{cyc}$
STDBY# High to normal state	t_{STDR}	—	$2t_{cyc}$

(5) System Bus Read Cycle (FORMAT = L)



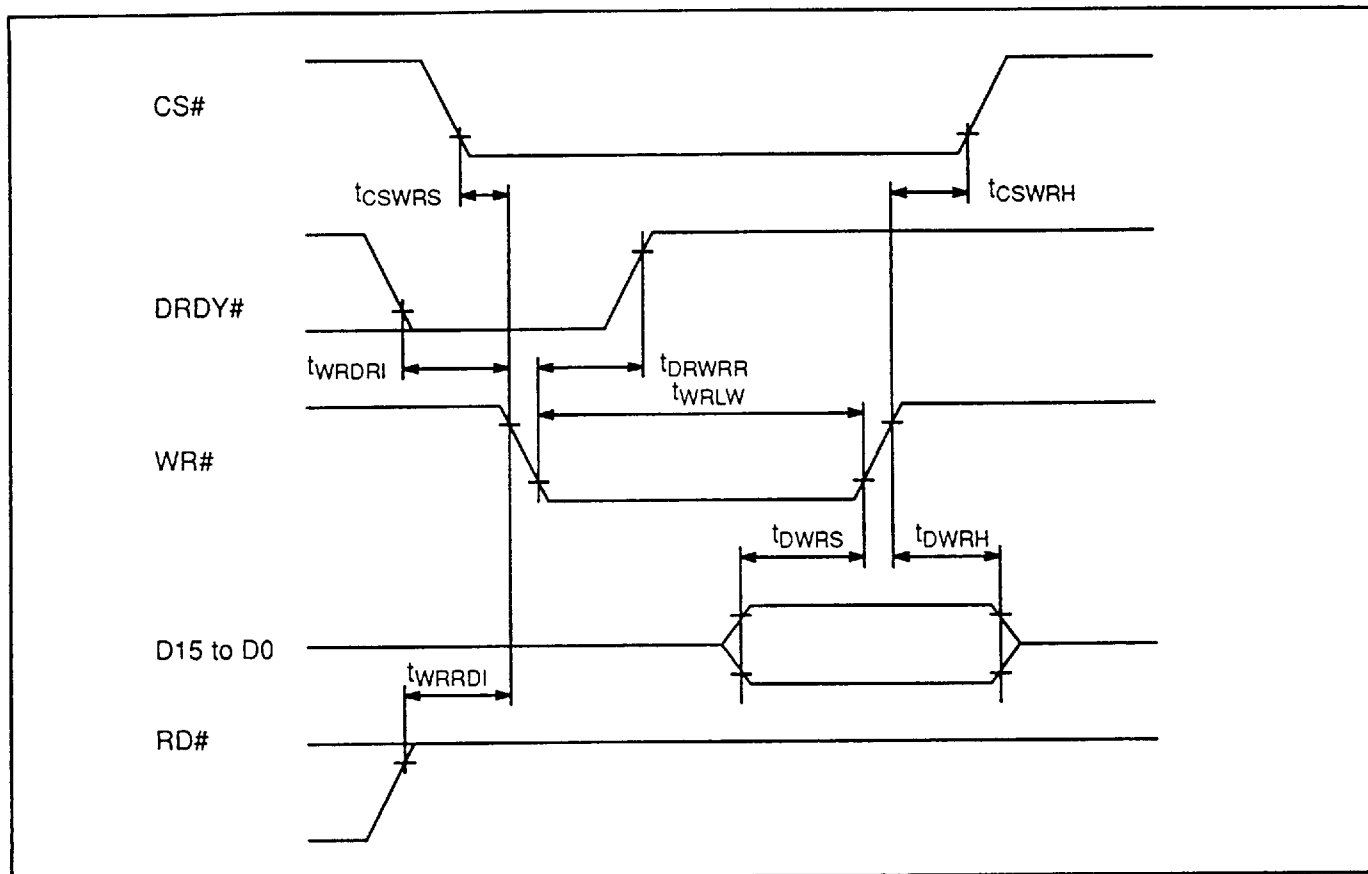
Parameter	Symbol	Min. value (ns)	Max. value (ns)
RD#↓ inhibit time from WR#↑	t _{RDWRI}	70	—
CS# Low setup time for RD#↓	t _{CSRDS}	15	—
CS# Low hold time for RD#↑	t _{CSRDH}	0	—
RD# Low pulse width	t _{RDLW}	60	—
RD# recovery time	t _{RDRCV}	70	—
D15 – D0 drive delay time from RD#↓	t _{DRDZ}	0	—
D15 – D0 valid delay time from RD#↓	t _{DRDV}	—	50
D15 – D0 hold time for RD#↑	t _{DRDH}	10	60

(6) System Bus Read Cycle (FORMAT = H)



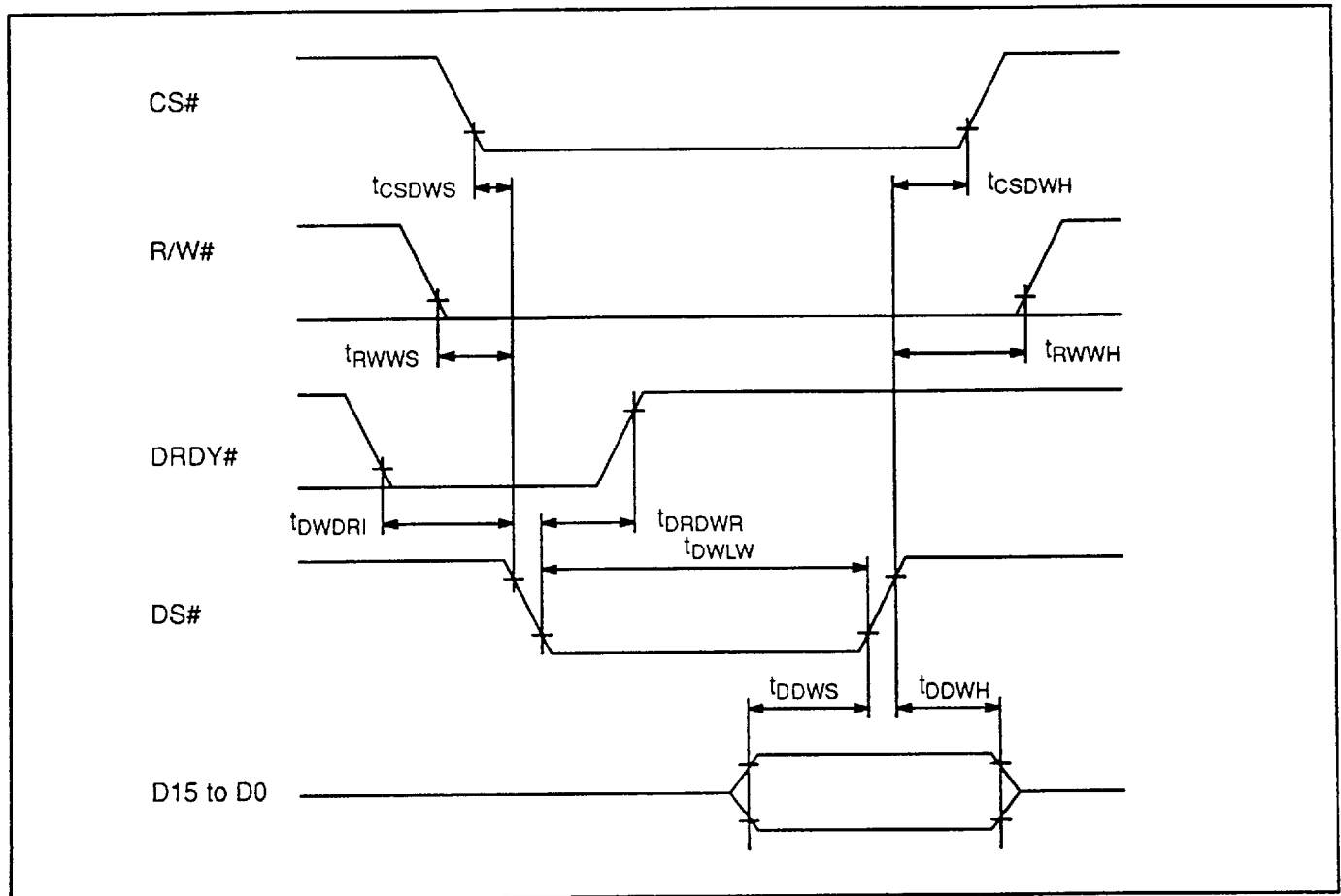
Parameter	Symbol	Min. value (ns)	Max. value (ns)
CS# Low setup time for DS#↓	t_{CSDRS}	15	—
R/W# High setup time for DS#↓	t_{RWRS}	15	—
CS# Low hold time for DS#↑	t_{CSDRH}	0	—
R/W# hold time for DS#↑	t_{RWRH}	15	—
DS# Low pulse width	t_{DRLW}	60	—
DS# recovery time	t_{DRRCV}	70	—
D15 – D0 drive delay time from DS#↓	t_{DDRZ}	0	—
D15 – D0 valid delay time from DS#↓	t_{DDRV}	—	50
D15 – D0 hold time for DS#↑	t_{DDRH}	10	60

(7) System Bus Write Cycle (FORMAT = L)



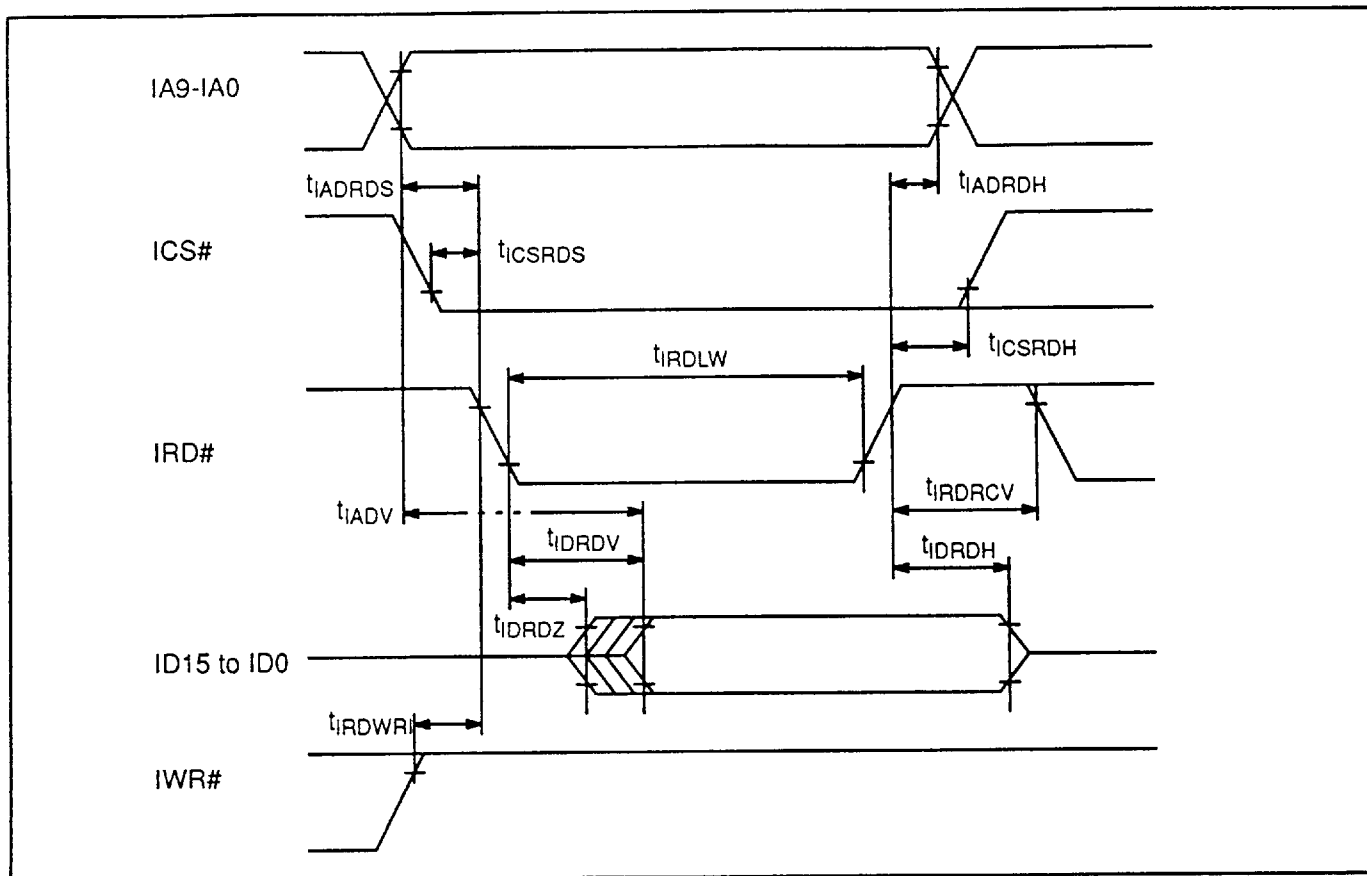
Parameter	Symbol	Min. value (ns)	Max. value (ns)
WR#↓ inhibit time from RD#↑	tWRRDI	70	—
CS# Low setup time for WR#↓	tCSWRS	15	—
CS# Low hold time for WR#↑	tCSWRH	0	—
WR#↓ inhibit time from DRDY#↓	tWRDRI	0	—
WR# Low pulse width	tWRLW	30	—
DRDY#↑ release time from WR#↓	tDRWRR	—	45
D15 – D0 setup time for WR#↑	tDWRS	40	—
D15 – D0 hold time for WR#↑	tDWRH	0	—

(8) System Bus Write Cycle (FORMAT = H)



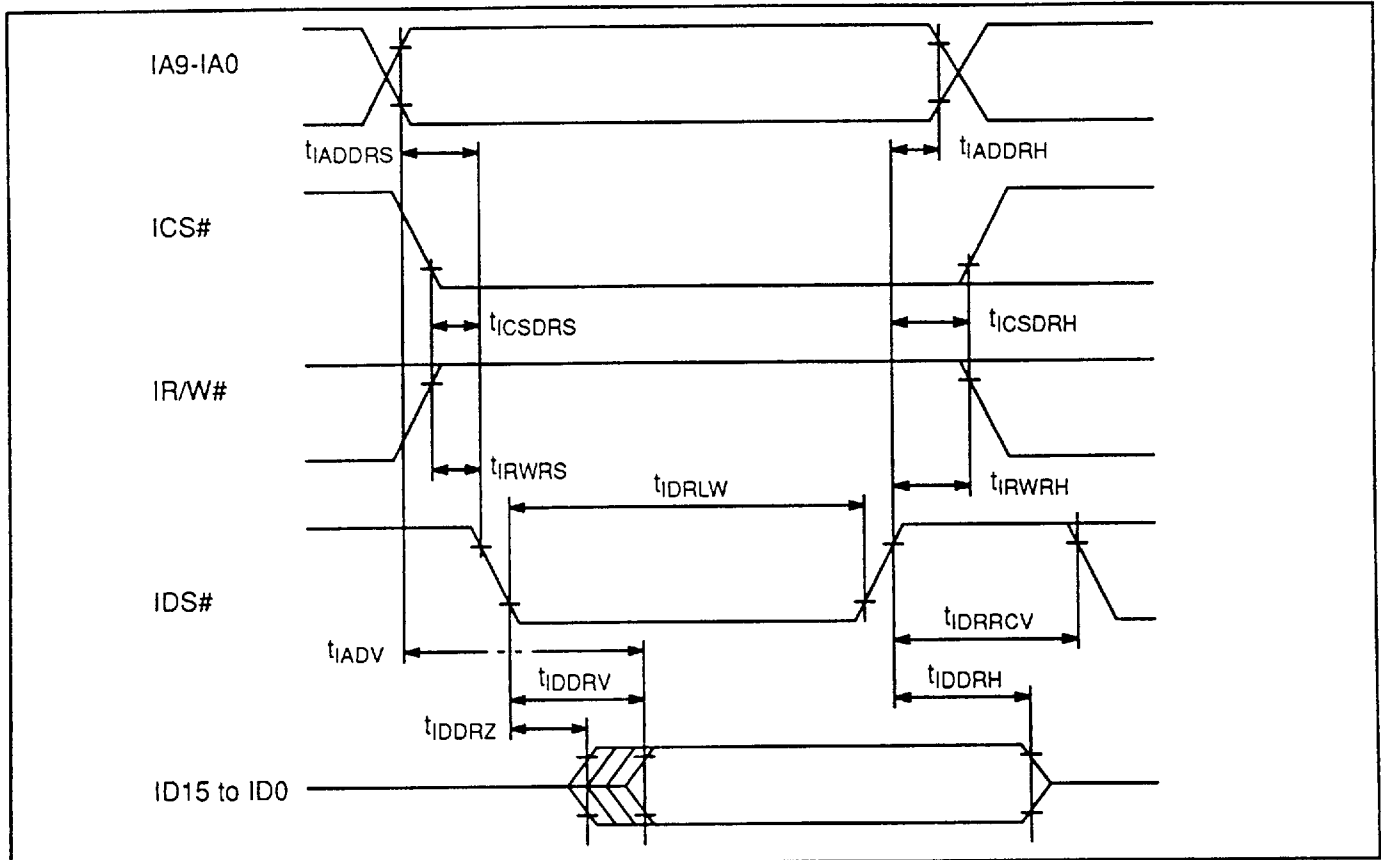
Parameter	Symbol	Min. value (ns)	Max. value (ns)
CS# Low setup time for DS#↓	t_{CSDWS}	15	—
R/W# Low setup time for DS#↓	t_{RWWS}	15	—
CS# Low hold time for DS#↑	t_{CSDWH}	0	—
R/W# Low hold time for DS#↑	t_{RWWH}	15	—
DS#↓ inhibit time from DRDY#↓	t_{DWDRI}	0	—
DRDY#↑ release time from DS#↓	t_{DRDWR}	—	45
DS# Low pulse width	t_{DWLW}	30	—
D15 – D0 setup time for DS#↑	t_{DDWS}	40	—
D15 – D0 hold time for DS#↑	t_{DDWH}	0	—

(9) Image Bus Read Cycle (Random access mode: FORMAT = L)



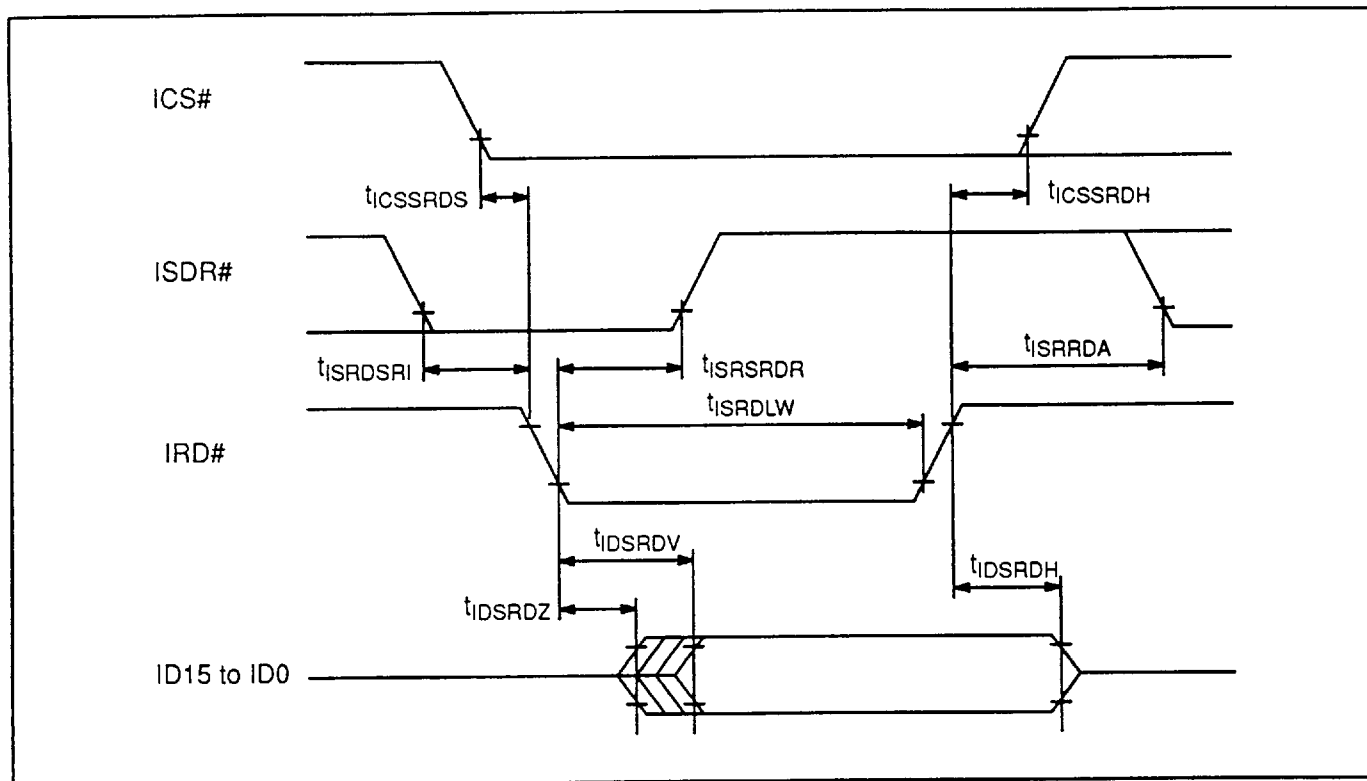
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IRD#↓ inhibit time from IWR#↑	t_{IRDWRI}	70	—
IA9 – IA0 setup time for IRD#↓	t_{IADRDS}	15	—
ICS# Low setup time for IRD#↓	t_{ICSRDS}	15	—
IA9 – IA0 hold time for IRD#↑	t_{IADRDH}	0	—
ICS# Low hold time for IRD#↑	t_{ICSRDH}	0	—
IRD# Low pulse width	t_{IRDLW}	60	—
IRD# recovery time	t_{IRDRCV}	70	—
ID15 – ID0 drive delay time from IRD#↓	t_{IDRDZ}	0	—
ID15 – ID0 valid delay time from IRD#↓	t_{IDRDV}	—	50
ID15 – ID0 valid delay time from IA9 – IA0	t_{IADV}	—	85
ID15 – ID0 hold time for IRD#↑	t_{IDRDH}	10	60

(10) Image Bus Read Cycle (Random access mode: FORMAT = H)



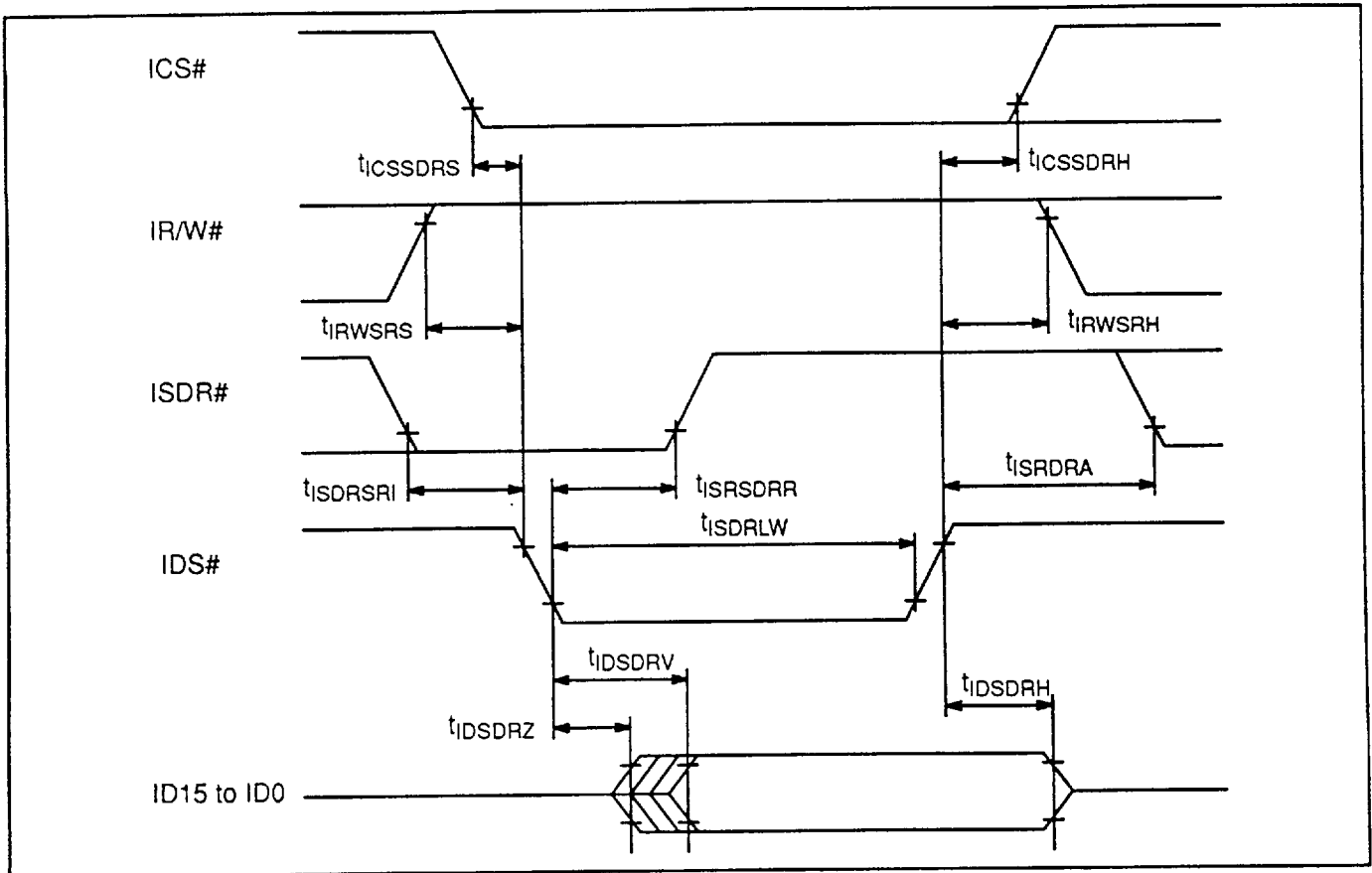
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IA9 – IA0 setup time for IDS#↓	t_{IADDRS}	15	—
ICS# Low setup time for IDS#↓	t_{ICSDRS}	15	—
IR/W# High setup time for IDS#↓	t_{IRWRS}	15	—
IA9 – IA0 hold time for IDS#↑	t_{IADDRH}	0	—
ICS# Low hold time for IDS#↑	t_{ICSDRH}	0	—
IR/W# High hold time for IDS#↑	t_{IRWRH}	0	—
IDS# Low pulse width	t_{IDRLW}	60	—
IDS# recovery time	t_{IDRRCV}	70	—
ID15 – ID0 drive delay time from IDS#↓	t_{IDRRZ}	0	—
ID15 – ID0 valid delay time from IDS#↓	t_{IDDRV}	—	50
ID15 – ID0 valid delay time from IA9 – IA0	t_{IADV}	—	85
ID15 – ID0 hold time for IDS#↑	t_{IDRRH}	10	60

(11) Image Bus Read Cycle (Sequential read mode: FORMAT = L)



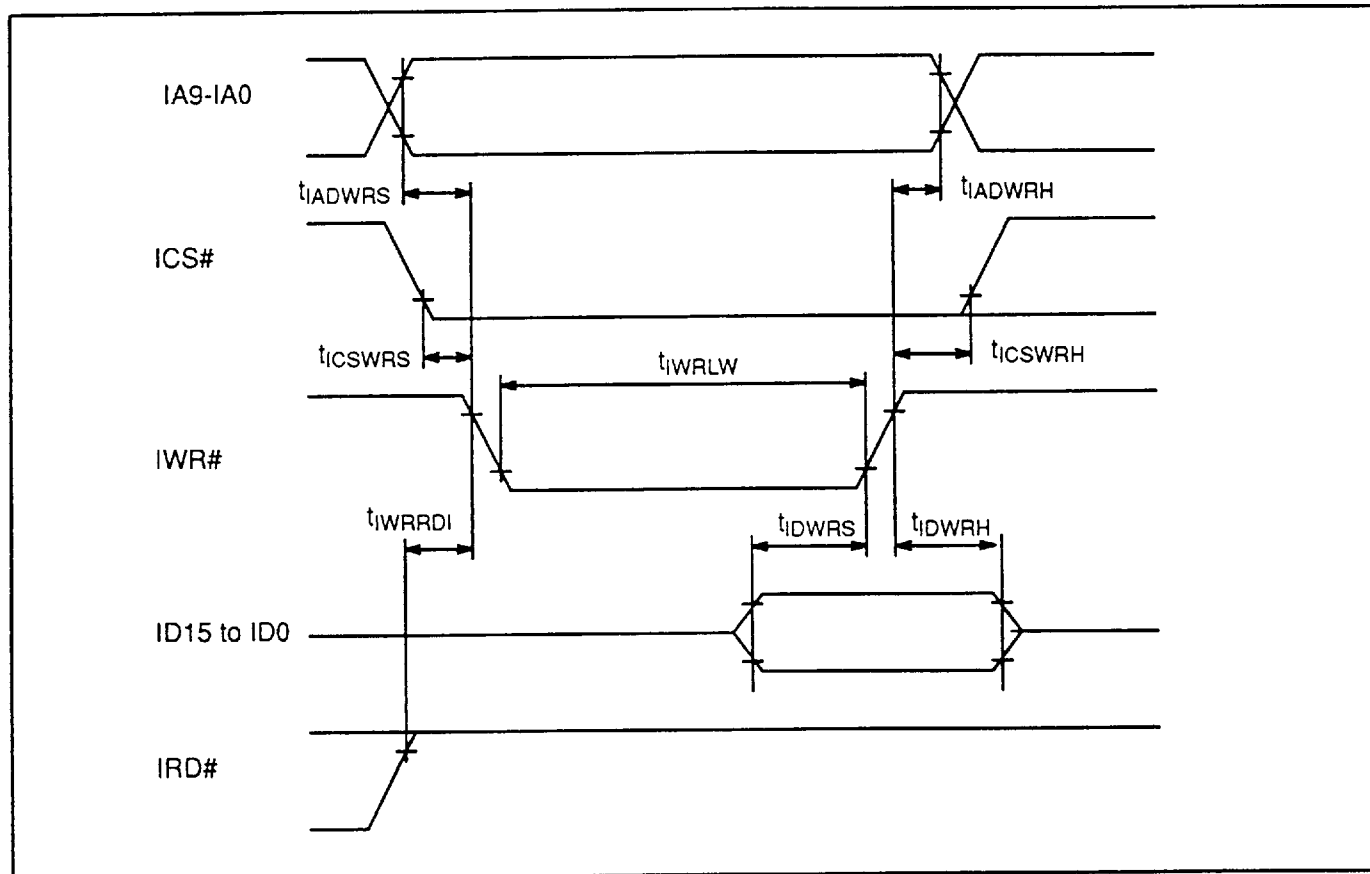
Parameter	Symbol	Min. value (ns)	Max. value (ns)
ICS# Low setup time for IRD#↓	$t_{ICSSRDS}$	15	—
ICS# Low hold time for IRD#↑	$t_{ICSSRDH}$	0	—
IRD#↓ inhibit time from ISDR#↓	$t_{ISRDSRI}$	0	—
ISDR#↑ release time from IRD#↓	$t_{ISRSRDR}$	—	45
IRD# Low pulse width	t_{ISDRLW}	60	—
ID15 – ID0 drive delay time from IRD#↓	t_{IDSVDZ}	0	—
ID15 – ID0 valid delay time from IRD#↓	t_{IDSVDV}	—	50
ID15 – ID0 hold time for IRD#↑	t_{IDSVDH}	10	60
ISDR# Low recovery time from IRD#↑	t_{ISRRDA}	—	6 t_{cyc}

(12) Image Bus Read Cycle (Sequential read mode: FORMAT = H)



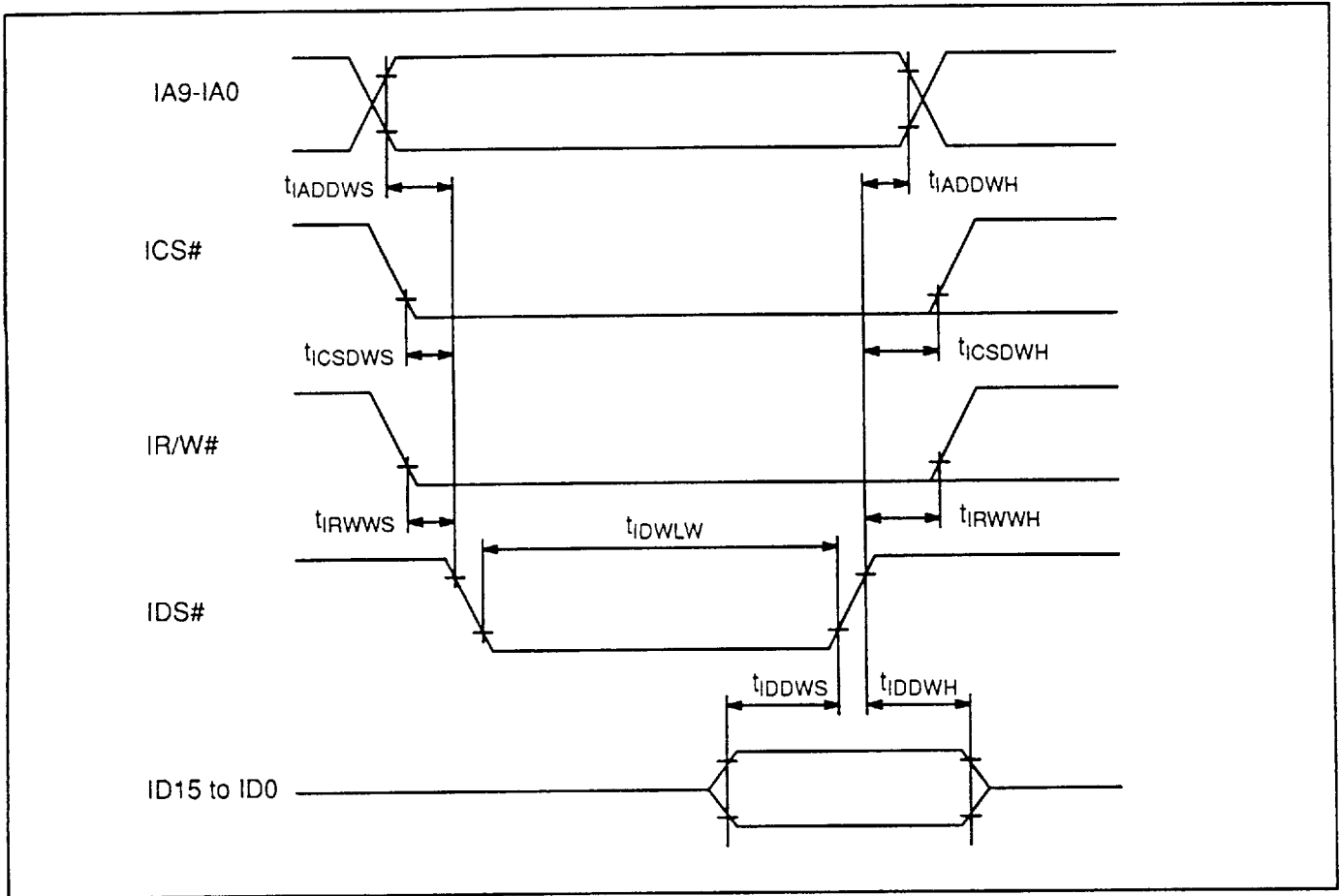
Parameter	Symbol	Min. value (ns)	Max. value (ns)
ICS# Low setup time for $IDS\#$	$t_{ICSSDRS}$	15	—
IR/W# High setup time for $IDS\#$	t_{IRWSRS}	15	—
ICS# Low hold time for $IDS\#$	$t_{ICSSDRH}$	0	—
IR/W# High hold time for $IDS\#$	t_{IRWSRH}	0	—
$IDS\#$ inhibit time from $ISDR\#$	$t_{ISDRSRI}$	0	—
$ISDR\#$ release time from $IDS\#$	$t_{ISRSDRR}$	—	45
$IDS\#$ Low pulse width	t_{ISDRLW}	60	—
$ID15 - ID0$ drive delay time from $IDS\#$	t_{IDSDRZ}	0	—
$ID15 - ID0$ valid delay time from $IDS\#$	t_{IDSDRV}	—	50
$ID15 - ID0$ hold time for $IDS\#$	t_{IDSDRH}	10	60
$ISDR\#$ Low recovery time from $IDS\#$	t_{ISRDRA}	—	$6 t_{cyc}$

(13) Image Bus Write Cycle (FORMAT = L)



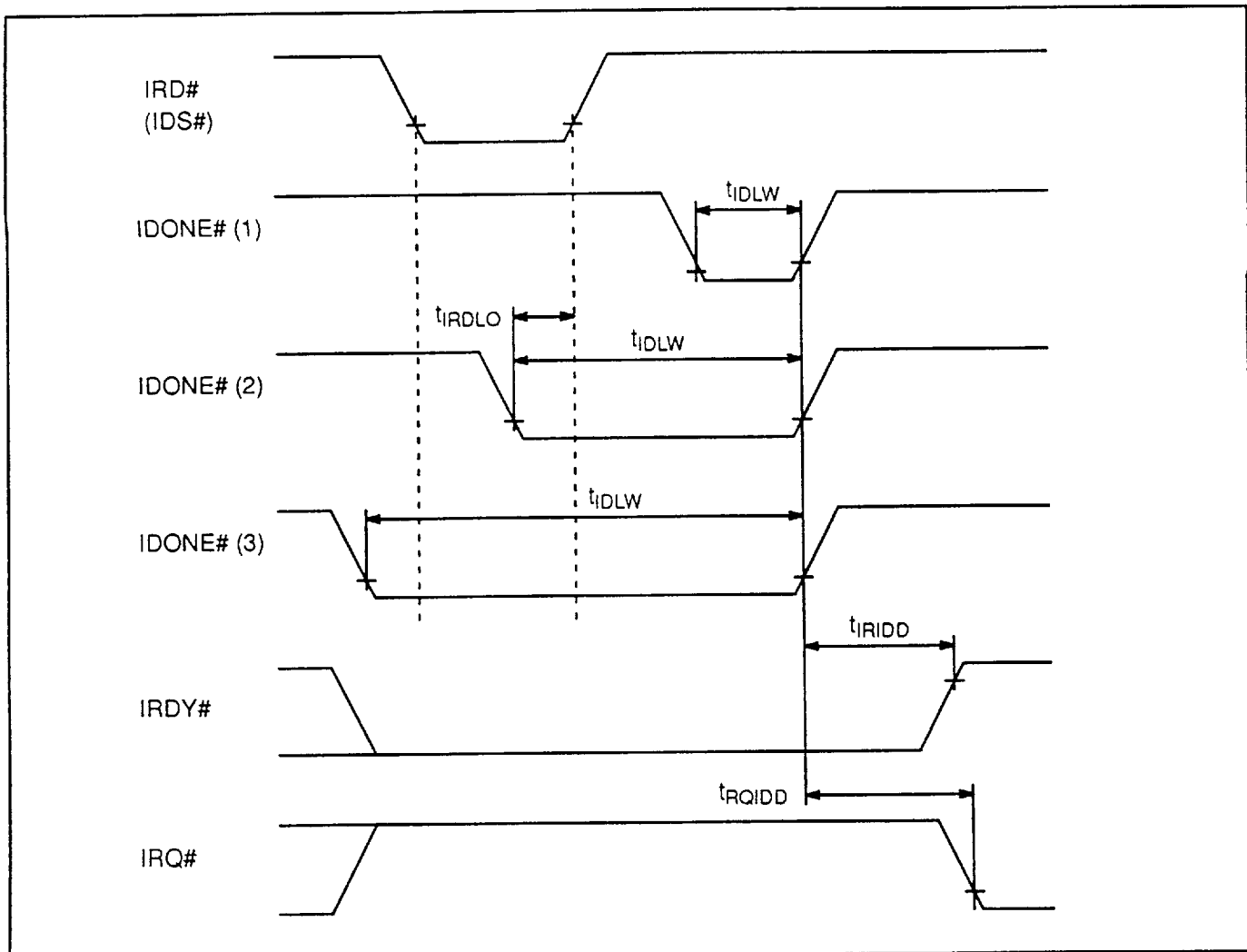
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IWR#↓ inhibit time from IRD#↑	t_{IWRDL}	70	—
IA9 – IA0 setup time for IWR#↓	t_{IADWRS}	15	—
ICS# Low setup time for IWR#↓	t_{ICSWRS}	15	—
IA9 – IA0 hold time for IWR#↑	t_{IADWRH}	0	—
ICS# Low hold time for IWR#↑	t_{ICSWRH}	0	—
IWR# Low pulse width	t_{IWRLW}	50	—
ID15 – ID0 setup time for IWR#↓	t_{IDWRS}	60	—
ID15 – ID0 hold time for IWR#↑	t_{IDWRH}	0	—

(14) Image Bus Write Cycle (FORMAT = H)



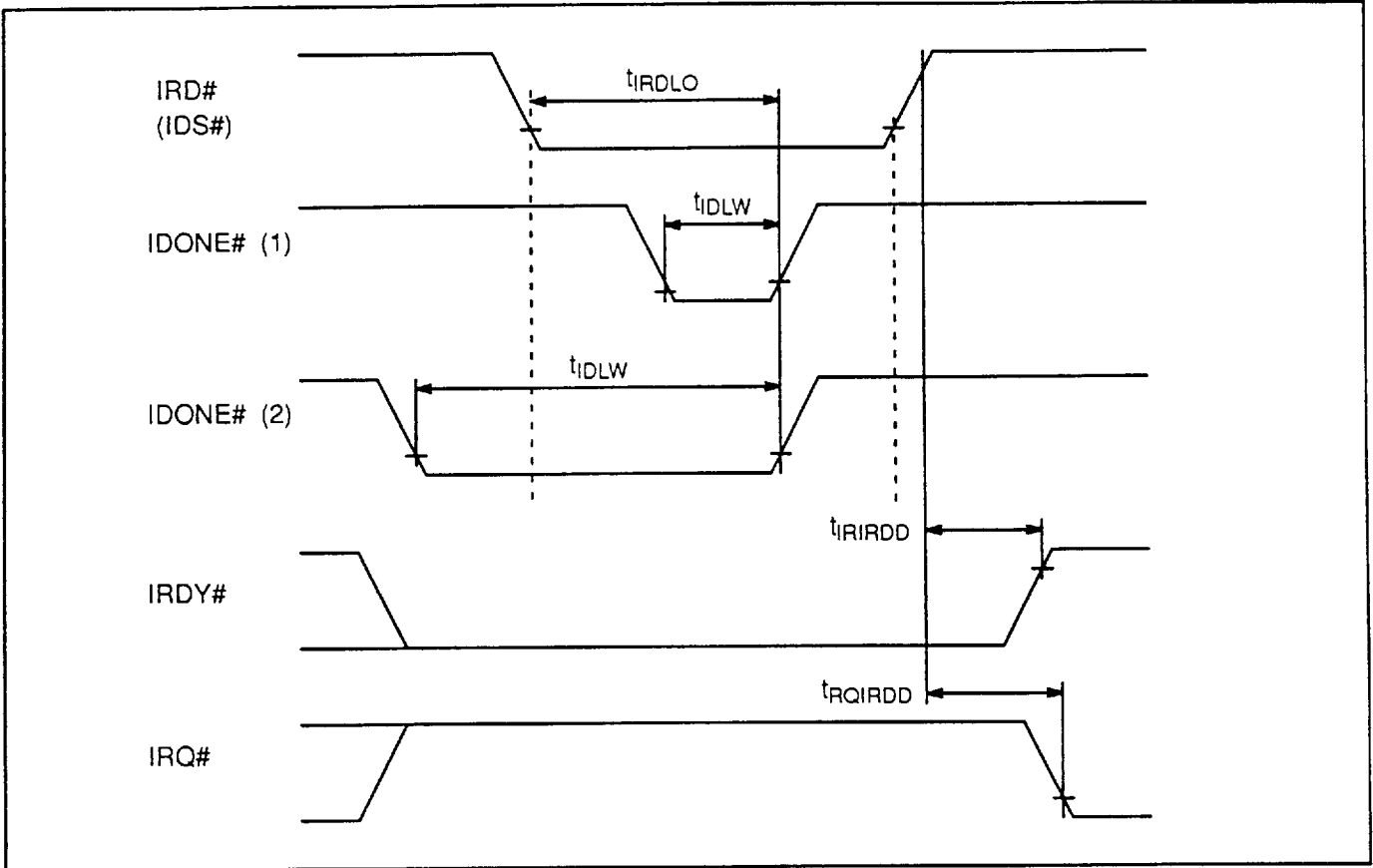
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IA9 – IA0 setup time for IDS#↓	t_{IADDWS}	15	—
ICS# Low setup time for IDS#↓	t_{ICSDWS}	15	—
IR/W# Low setup time for IDS#↓	t_{IRWWS}	15	—
IA9 – IA0 hold time for IDS#↑	t_{IADDWH}	0	—
ICS# Low hold time for IDS#↑	t_{ICSDWH}	0	—
IR/W# Low hold time for IDS#↑	t_{IRWWH}	0	—
IDS# Low pulse width	t_{IDWLW}	50	—
ID15 – ID0 setup time for IDS#↑	t_{IDDWS}	60	—
ID15 – ID0 hold time for IDS#↑	t_{IDDWH}	0	—

(15) IDONE# Input Timing 1



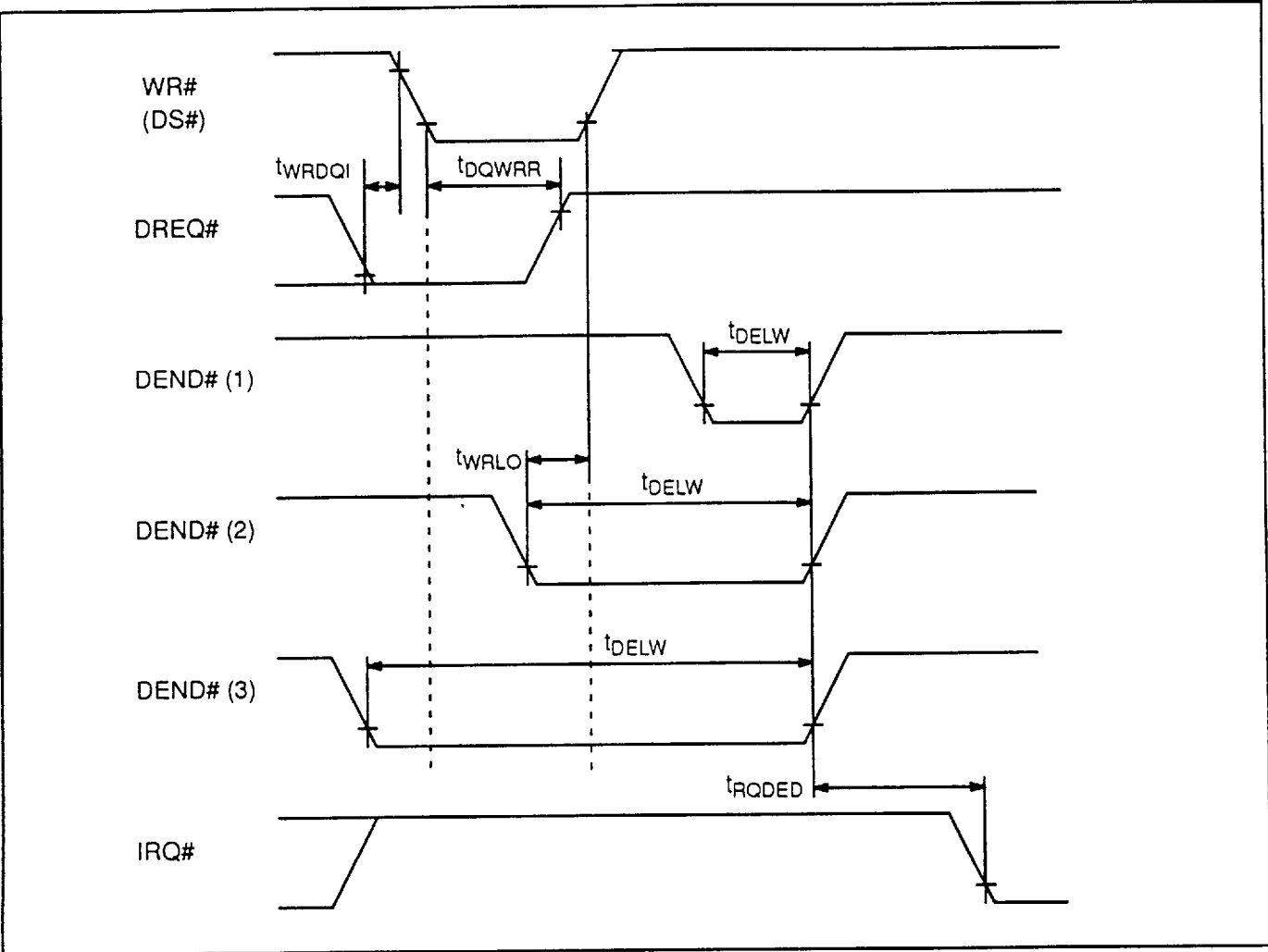
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IRD#/IDONE# Low overlap time	t_{IRDLO}	10	—
IDONE# Low pulse width	t_{IDLW}	30	—
IRDY# negate delay time from IDONE#↑	t_{IRIDD}	—	45
IRQ# assert delay time from IDONE#↑	t_{ROIDD}	—	45

(16) IDONE# Input Timing 2



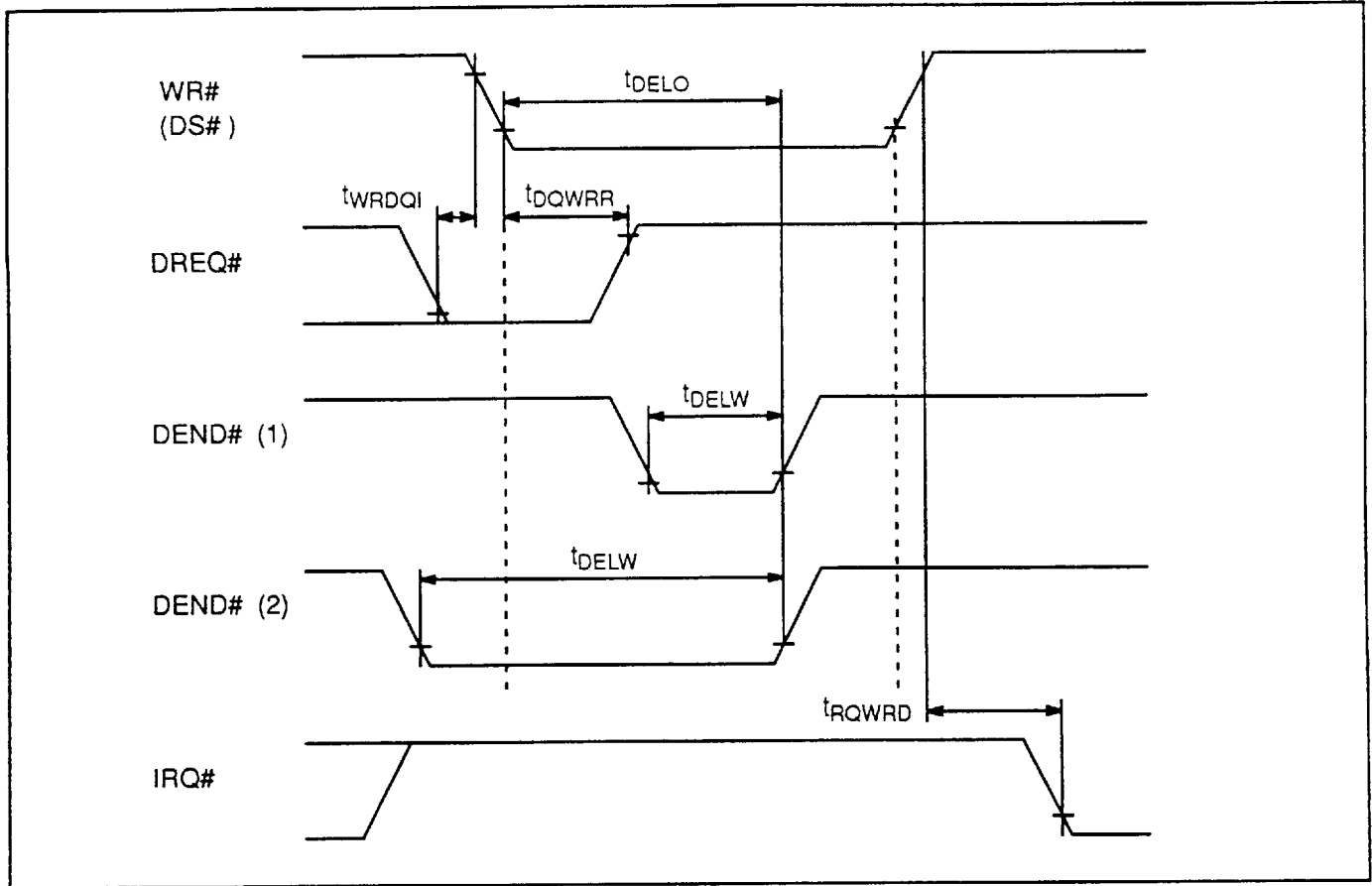
Parameter	Symbol	Min. value (ns)	Max. value (ns)
IRD# /IDONE# Low overlap time	t_{IRDLO}	10	—
IDONE# Low pulse width	t_{IDLW}	30	—
IRDY# negate delay time from IRD#↑	t_{IRIRDD}	—	45
IRQ# assert delay time from IRD#↑	t_{RQIRDD}	—	45

(17) DEND# Input Timing 1



Parameter	Symbol	Min. value (ns)	Max. value (ns)
WR#↓ inhibit time from DREQ#↓	t_{WRDQI}	0	—
DREQ#↑ release time from WR#↓	t_{DQWRR}	45	—
WR#/DEND# Low overlap time	t_{WRLO}	10	—
DEND# Low pulse width	t_{DELW}	30	—
IRQ# assert delay time from DEND#↑	t_{RQDED}	—	45

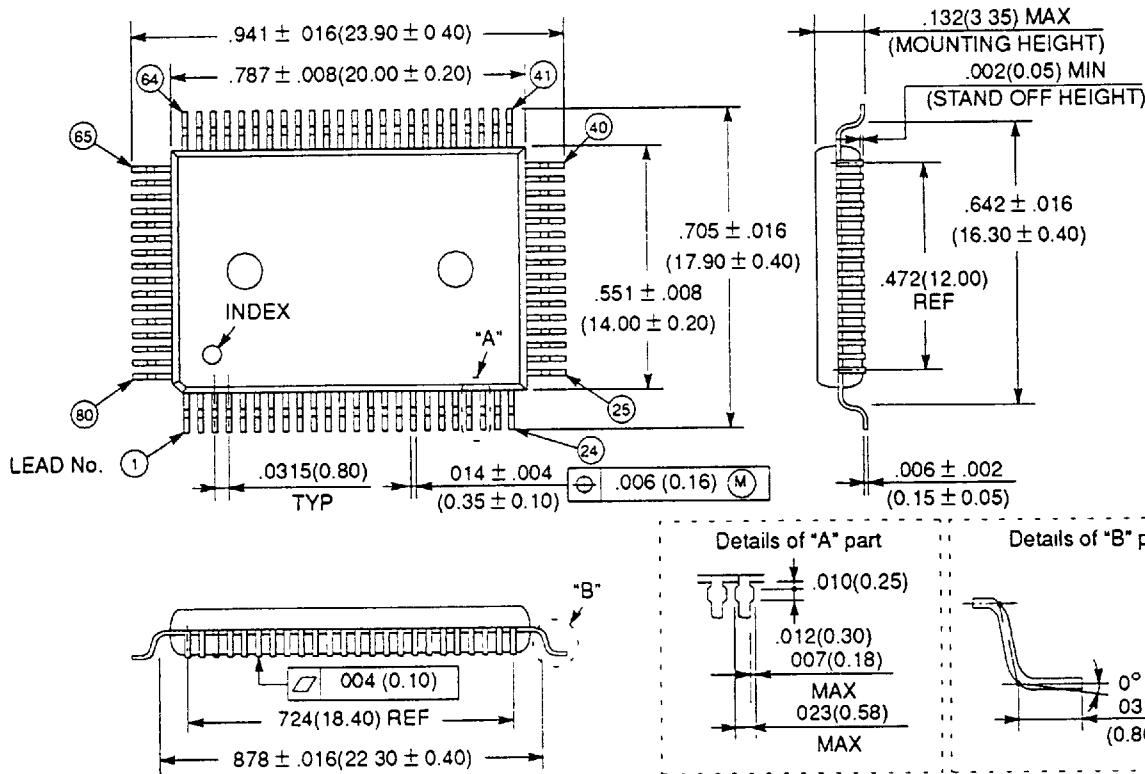
(18) DEND# Input Timing 2



Parameter	Symbol	Min. value (ns)	Max. value (ns)
WR#↓ inhibit time from DREQ#↓	t_{WRDQI}	0	—
DREQ#↑ release time from WR#↓	t_{DQWRR}	45	—
WR#/DEND# Low overlap time	t_{WRLO}	10	—
DEND# Low pulse width	t_{DELW}	30	—
IRQ# assert delay time from WR#↑	t_{RQWRD}	—	45

PACKAGE DIMENSIONS

80-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-80P-M06)



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Dimensions in inches (millimeters)

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