HD153031RF
36-Mbps Data Channel Processor

HITACHI

Rev. 1
Aug. 1993
Preliminary

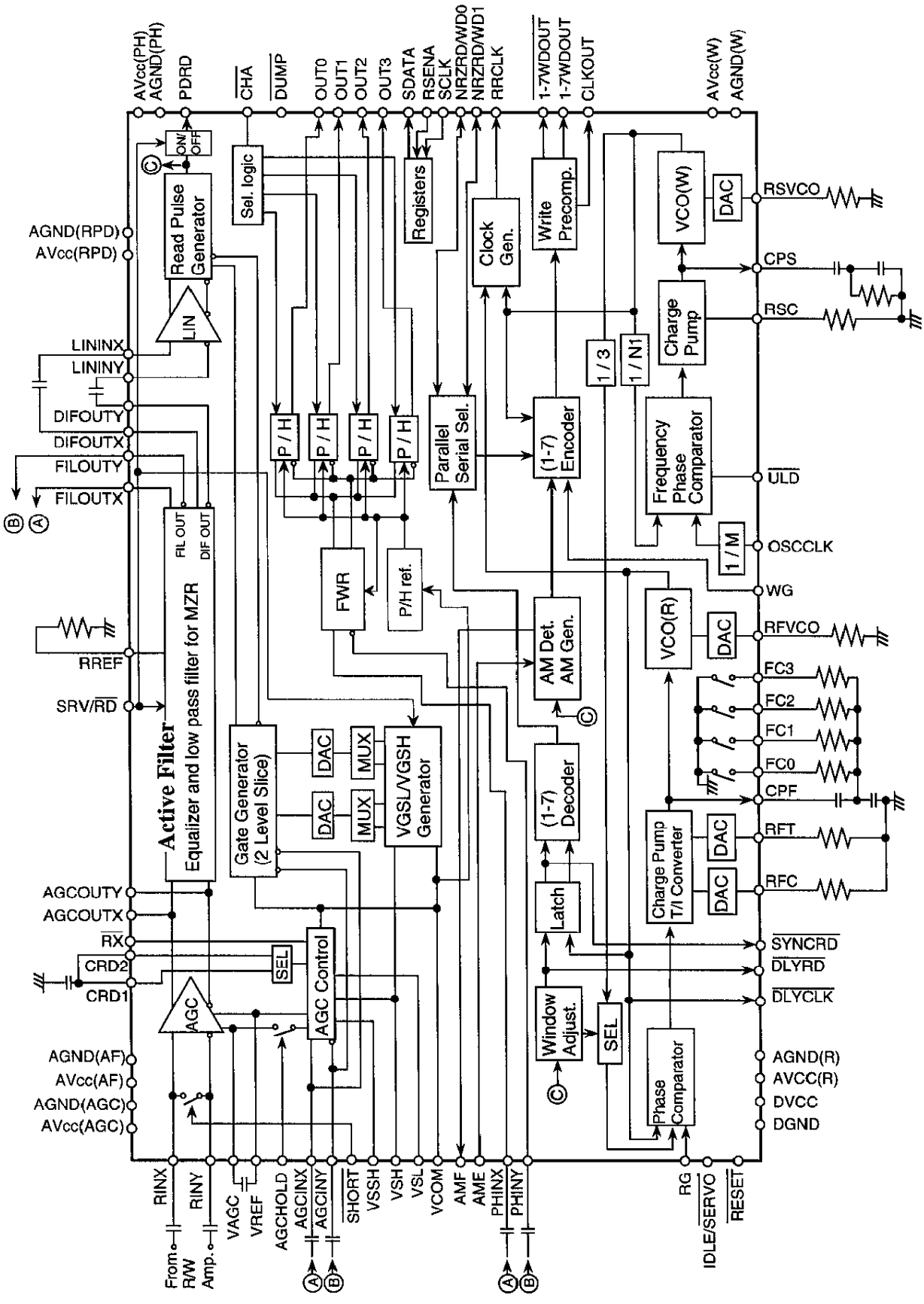
Description

The HD153031RF is a 36 Mbps 1-7 ENDEC data separator with built-in read pulse detector, active filter, frequency synthesizer and synchronizer developed for use in magnetic disk drives. In read mode the HD153031RF decords the read wave form output from the read/write amplifier into an NRZ signal. In write mode it encodes the NRZ signal output from the controller into a 1-7 RLL code.

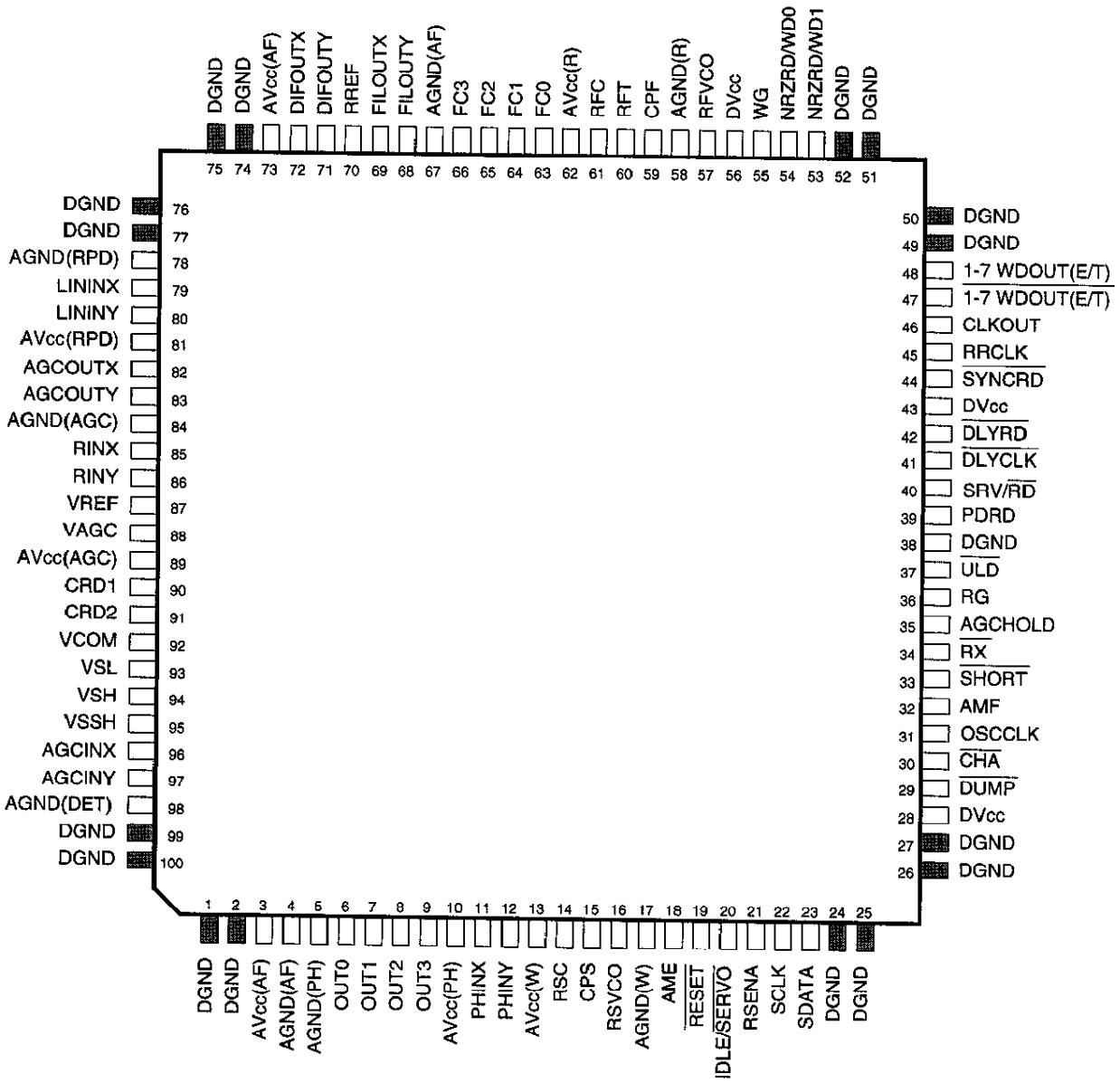
Features

- Maximum NRZ data transfer rate : 36Mbps.
- Data transfer clock frequency : 1.5 data transfer rate (54MHz maximum).
- Settings are micro-computer programmable.
- On-chip frequency synthesizer generates encode clock for writing (1% steps at f_{MAX}/f_{MIN}=2.55).
- Programmable window centering adjustment and window monitoring functions.
- User-selectable single zone recording or multiple zone recording options. The following are programmable for multiple zone recording : VCO center frequency (192 settings), loop Filter constant (2 settings), charge pump current levels (8 settings), T/I converter output current (8 settings), active filter cutoff frequency for servo and data modes (128 settings).
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- Built-in active filter 7-bit programmable cut-off frequencies.
- Two sets of 4-bit High and Low slice levels for reliable pulse detection .
- 1-7WDOUT outputs are selectable differential pseudo-ECL or TTL pair for high speed transfer without timing error.
- High-speed acquisition can be accomplished with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.
- VCO oscillation timing capacitor is built in for better noise immunity.
- PLL characteristic frequency and damping rate are defined without 2T-8T (1-7RLL) signal cycle.
- Built-in AGC amplifier for stable reproduction despite varying media and head characteristics.
- Gate generator eliminates incorrect read pulse problems that occur with time-domain filtering with appropriate slice-level setting.
- Head resolution can be increased without incorrect read pulse worries.
- AGC amplifier gain can be set to zero during writing.
- Built-in write phase compensation function with programmable delay time.
- Early or Late write pre-compensation amounts can be programmed independently.
- High speed data transfer inputs and outputs are done via complementary TTL output pairs.
- Hi-BiCMOS process achieves high speed with low power dissipation.
- Idle mode and power down functions.
- QFP-100 pin package suitable for compact surface mounting (resin size : 14mm x 14mm)
- Required only a single 5V supply.

2. Block diagram



3. Pin arrangement



(Top view)

4. Pin Functions

Pin Name	Pin No.	Type	Function
RG (Read gate)	36	In	High level at the input selects read mode. This signal switches the clock for counters and internal circuits, and begins phase synchronization of the decode clock generator's VFO with the 1-7 decode data.
PHINX PHINY	11 12	In	Differential inputs for the servo Peak/Hold circuit.
$\overline{\text{RESET}}$	19	In	Low input initializes internal circuits. Drive this line low at power-up. Low input also locks the two built-in VCOs to their center frequencies. Keep this line high during normal operation.
OSCCLK (Oscillator clock)	31	In	Clock synthesizer's reference clock input. The frequency synthesizer generates encode clock frequencies from the input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized with frequency 1.5 times the data transfer rate.
1-7WDOUT $\overline{\text{1-7WDOUT}}$ (Write Data outputs)	48 47	Out	1-7 RLL Write Data Differential Output. Pseudo ECL/TTL are available by bit 6 of register"$hD". When this bit is "H", these outputs are TTL. When this bit is "L", these outputs are ECL.These Pin provide the 1-7WDOUT write data that goes to the Read/Write amplifier after the write pre-compensation. When WG goes high, 1-7 WDOUT pin are output mode.
CLKOUT	46	Out	This clock is for the external write pre-compensation in the Write mode. This clock(TTL level) is synchronized with 1-7WDOUT.
$\overline{\text{ULD}}$ (Unlock detect)	37	Out	Error output from the encode clock generator's frequency synthesizer. ULD goes low to indicate that the PLL in the encode clock generator's frequency synthesizer has lost lock. The disk controller should immediately halt the write operation. Data must be written again from the beginning.
RSVCO	16	External component required	Connect a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer.
CPS	15	External component required	Current output to an external loop filter.
RSC	14	External component required	Connect a resistor to set the charge pump output current for the encode clock generator's frequency synthesizer.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
RFC	61	External component required	Connect a resistor to set the charge pump output current for the decode clock generator's VFO. The charge pump current level is set by GAC[5:3] and CPO[4:0] registers.
RFT	60	External component required	Connect a resistor to set the T/I converter's sampling feedback gain to 1(nominal). The T/I converter's output current is determined by this resistor, and registers VFC[4:0] & GAC[2:0] & TIO[4:0].
CPF	59	External component required	Current output to the external loop filter.
RREF	70	External component required	Connect to a resistor to set the reference current for the Active Filter's DAC.
FC0 FC1 FC2 FC3	63 64 65 66	External component required	Connect to a loop filter resistor to set the attenuation ζ of the PLL. Each line is grounded through an MOS switch is selected by PLL gain mode and bit 6 of register GAC.

Bit 6 of register GAC	PLL gain mode	Pin			
		FC0	FC1	FC2	FC3
"0"	High	ON	ON	OFF	OFF
	Normal	ON	OFF	OFF	OFF
"1"	High	OFF	OFF	ON	ON
	Normal	OFF	OFF	ON	OFF

RFVCO	57	External component required	Connect to a resistor to set the center frequency of the VCO in the decode clock generator's VFO.
SRV/$\overline{RD}$	40	Input	"H":Servo Mode,"L":Read Mode. In the servo mode ,"CFCB" register set the A/F's cutoff frequency and VGSLB register set the gate slice low level. In the read mode ,"CFCA" register set the A/F's cutoff frequency and VGSLA register set the gate slice level.
RINX RINY	85 86	Differen-tial input	Differential input lines for the signal read from the recording medium.
LININX LININY	79 80	Differen-tial input	Differential input lines for the zero-crossing comparator. Normally connect to DIFOUTX/Y of the active filter with bypass capacitors.
AGCINX AGCINY	96 97	Differen-tial input	Differential input lines for the AGC output amplitude detector. Connect to FILOUTX/Y outputs of the AF with bypass capacitors.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{RX}$	34	In	TTL-level input that switches the AGC loop on or off. $\overline{RX}$ input: High → AGC loop on. $\overline{RX}$ input: Low → AGC loop off.
AGCHOLD	35	In	TTL-Level input that locks the AGC amplifier gain. When AGCHOLD goes high, the gain is locked at its immediately preceding value.
AGCOUTX AGCOUTY	82 83	Differential output	Differential output lines for monitor from the AGC amplifier. The outputs are open-emitter type and would need ext. 1~10K pulldowns.
VREF	87	Monitor line	Monitor line for the AGC amplifier reference voltage.
VAGC	88	Monitor line	Monitor line for the AGC amplifier gain setting voltage.
PDRD	39	Out	Output line for the data read from disk as reshaped into digital data by the read pulse detector. When SRV/$\overline{RD}$(40Pin) goes high, PDRD outputs read data pulse. When SRV/RD goes low, PDRD is disenable mode.
VCOM	92	External component required	Reference voltage output line for the AGC output amplitude detector and the Gate generator.
VSL	93	External component requird	Voltage input line for seting the low slice level of AGC output amplitude detector. Corresponds to the discharge current threshold. Normally this level is set 67% of the VSH level.
VSH	94	External component required	Voltage input line for settiing the high slice level of the AGC output amplitude detector. Corresponds to the charge current threshold
VSSH	95	External component required	Voltage inputline for setting the fast attack(high gain) high slice voltage of the AGC output amplitude detector. Normally this level is set 160% of the VSH level.
IDLE/$\overline{SERVO}$	20	In	The input is used in combination with the two Mode bits in the PCN register to reduce power consumption in the Idle mode. When PCN= 00, device is in the R/W normal mode, all circuits are ON. When PCN = 11, device is in the Sleep mode, all circuits are OFF except the I/O and logic. When PCN = 10, then depending on the logic level of the IDLE/$\overline{SERVO}$ pin; if it is High, then chip is in the Idle mode and all circuits are OFF except for the I/O, logic, and the bias CKT's; if it is Low, then the device is in the Servo mode and the I/O, logic, bias CKT's, AGC, active filter, Read Pulse Detector, and Peak/Hold should be ON with only the RD PLL and the WR PLL being OFF.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
CRD1	90	External component required	In reading the normal data, the charge /discharge current output line for the AGCoutput amplitude detector. connected to 91PIN (CRD2)
CRD2	91	External component required	External capacitor is needed for AGC output amplitude detector.
FILOUTX FILOUTY	69 68	Differential output	Differential output line from Active Filter. Connect to AGCINX,Y and PHINX,Y through capacitors.
DIFOUTX DIFOUTY	72 71	Differential output	Differential output line from Active Filter. Connect to LININX,Y through capacitors.
$\overline{\text{SHORT}}$	33	In	When this terminal is 'L', RINX and RINY are shorted.
OUT0~ OUT3	6,7,8,9	External component required	Connect to external capacitors for servo peak/hold.
WG	55	In	Write gate signal input. Set this PIN high during writing
NRZRD/WD1	53	In/Out	I/O pin of NRZ signal. This pin is effective only in the case of parallel transferring. NRZ Data select bit 7 of register($h8) controls parallel/serial. (When this bit is " H" , NRZ mode is parallel)
NRZRD/WD0	54	In/Out	I/O pin of NRZ signal. In the serial transfer mode, only this pin is effective. NRZ Data select bit 7 of register($h8) controls parallel/ serial. (When this bit is " L" , NRZ mode is serial)
SDATA	23	In/Out	Data is transmitted in 16-bit packet MSB first. The first 2 bits determine the read or write mode, the next bit is "Don't Care", the next 4 bits are for the register address, followed by 1 "Don't Care" bit, then the last 8 bits are for the Write or Read Data.
RSENA	21	In	This active low input selects the device and enables the serial port.
AMF	32	Out	Output pin of the address mark found signal in the soft sector mode.
AME	18	In	Input pin for the address mark enable inthe soft sector mode. In the hard sector mode, this pin must set low.
$\overline{\text{CHA}}$	30	In	Input pin of the control signal of Peak/hold circuit(TTL level) Position signal is sampled by $\overline{\text{CHA}}$="L"
$\overline{\text{DUMP}}$	29	In	Input pin of the discharge control signal of Peak/Hold circuit. TTL level, $\overline{\text{DUMP}}$="L" is for discharge.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
SCLK	22	In	This is the serial clock sent in by the hard disk controller or other ASIC device. When the serial port is not enabled, this clock line should be driven low. For either read or write transfer, a 16 clock burst is required for proper operation. Data is latch in during write or sent out during read with the rising edge of the SCLK.
$\overline{\text{DLYCLK}}$	41	Out	Monitor pin(TTL level) for Window adjustment. This pin allows the VCO clock signal output by the PLL circuit to be monitored. Contact Hitachi,Ltd. for special instrustions if use of this function is required.
$\overline{\text{DLYRD}}$	42	Out	Monitor pin(TTL level) for Window adjustment. This pin allows the read data signal output from the window adjustment circuit to be monitored. Contact Hitachi,Ltd. for special instructions if use of this function is required.
$\overline{\text{SYNCRD}}$	44	Out	Monitor pin(TTL level) for Window adjustment. This pin outputs the read data outputs the read data input to the PLL block latched by the VCO clock. Contact Hitachi,Ltd. for the special instructions if use of this function is required.
RRCLK	45	Out	Read refernce clock output(TTL level). At read time,this pin provides a clock which is synchronized with the converted NRZRD signal. This controller should read NRZRD by this clock. Other than read, reefernce clock is provided to disk controller.
DGND	1, 2, 24,25,26, 27, 38, 49, 50, 51, 52, 74, 75, 76, 77, 99,100	Ground	Digital ground.
DVcc	28, 43, 56	Power	Digital Vcc power supply.
AVcc(PH)	10	Power	Analog Vcc power supply for peak hold.
AGND(PH)	5	Ground	Analog ground for peak hold.
AVcc(W)	13	Power	Analog Vcc power supply for synthesizer.
AGND(W)	17	Ground	Analog ground for synthesizer.
AVcc(R)	62	Power	Analog Vcc power supply for synchronizer.
AGND(R)	58	Ground	Analog ground for synchronizer.
AVcc(AF)	3, 73	Power	Analog Vcc power supply for active filter.
AGND(AF)	4, 67	Ground	Analog ground for active filter.
AVcc(AGC)	89	Power	Analog Vcc power supply for AGC.
AGND(AGC)	84	Ground	Analog ground for AGC.
AVcc(RPD)	81	Power	Analog Vcc power supply for read pulse detector.
AGND(RPD)	78	Ground	Analog ground for read pulse detector.
AGND(DET)	98	Ground	Analog ground for AGC control circuit

5. Registers

The HD153031RF has 16 address's 8 bits-register that control the center frequency of the decode clock generator's VFO and the frequency of the encode clock generator's frequency synthesizer, control thc synthesizer's gain, control the read data pulse width and its polarity, control the synchronizer's gain and offset, adjust the decode window, apply the early/late write precompensation, control the prescaling value, adjust the active filter's cut-off frequency, and controls various functions.

Address register value MSB LSB	Name	Abbreviation
0 0 0 0	VCO center frequency control register	VFC register
0 0 0 1	RD-PLL Gain control register	GAC register
0 0 1 0	RD-PLL Charge Pump offset control register Write precompensation delay control register (L)	CPO register WPL register
0 0 1 1	RD-PLL T/I offset control register Write precompensation delay control register (S)	TIO register WPS register
0 1 0 0	Window adjustment register (0.67ns typ. /step) Window fine adjustment register(0.25ns typ. /step)	WAJ register WFA register
0 1 0 1	AGC Mode control bit (FAST / SLOW) Read data (PDRD) polarity control register Read data (PDRD) pulse width control register WR-PLL Gain control register	AGS bit RDSEL register PW register SGC register
0 1 1 0	Prescaler of WR-PLLcontrol register	PSC register
0 1 1 1	AF cut-off frequency control register(for Read)	CFCA register
1 0 0 0	NRZ Data 1bit - serial / 2bits parallel select bit AF cut-off frequency control register(for Servo)	NRZM bit CFCB
1 0 0 1	Unlock detect gain control register (for WR-PLL) Boost level control register	ULD register BLC register
1 0 1 0	High pass filter cut-off frequency control register(for Read)	HPCA register
1 0 1 1	High pass filter cut-off frequency control register(for Servo)	HPCB register
1 1 0 0	Gate generator's High-slice level control register(for Read) Gate generator's Low-slice level control register(for Read)	VGSHA register VGSLA register
1 1 0 1	1-7 WDOUT output type control bit (ECL / TTL) Wrlte precompensation delay control register (E) Write precompensation delay control register (N)	WDM bit WPE register WPN register
1 1 1 0	AGCOUT enable control bit Power management control register Gate generator's Low-slice level control register(forServo)	AOE bit PCN register VGSLB register
1 1 1 1	Test Mode control register	MDC register

6. Register Descriptions

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Register Functions
0 0 0 0	VFC7	VFC6	VFC5	VFC4	VFC3	VFC2	VFC1	VFC0	VFC: controls the center frequency of the WR-PLL & RD-PLL.
0 0 0 1	0	RFCA	GAC5	GAC4	GAC3	GAC2	GAC1	GAC0	GAC: controls the RD-PLL's T/I and Charge Pump gain.
0 0 1 0	WPL2	WPL1	WPL0	CPO4	CPO3	CPO2	CPO1	CPO0	CPO: controls the Off-Set of the RD-PLL's Charge Pump circuit. WPL: sets the write precompensation delays. (L)
0 0 1 1	WPS2	WPS1	WPS0	TIO4	TIO3	TIO2	TIO1	TIO0	TIO: controls the Off-Set of the RD-PLL's T/I converter. WPS: sets the write precompensation delays. (S)
0 1 0 0	WFA2	WFA1	WFA0	WAJ4	WAJ3	WAJ2	WAJ1	WAJ0	WFA: fine adjusts data window. WAJ: adjusts data window.
0 1 0 1	AGCSEL	RDSEL1	RDSEL0	PW1	PW0	SGC2	SGC1	SGC0	AGCSEL: sets AGC mode Fast or Slow. RDSEL: controls PDRD pulse polarity PW: controls PDRD pulse width. SGC: sets the WR-PLL gain.
0 1 1 0	0	PSC6	PSC5	PSC4	PSC3	PSC2	PSC1	PSC0	PSC: sets the WR-PLL prescaler's counter value.
0 1 1 1	0	CFCA6	CFCA5	CFCA4	CFCA3	CFCA2	CFCA1	CFCA0	CFCA: controls Read Mode Active Filter's Cut-Off frequency.
1 0 0 0	NRZM	CFCB6	CFCB5	CFCB4	CFCB3	CFCB2	CFCB1	CFCB0	NRZM: selects 1bit or 2bits NRZ data CFCB: controls Servo Mode Active Filter's Cut-Off frequency.
1 0 0 1	TSTBF	ULD1	ULD0	BLC4	BLC3	BLC2	BLC1	BLC0	ULD: sets unlock detect period. BLC: controls AF's Boost level.
1 0 1 0	0	0	0	HPCA4	HPCA3	HPCA2	HPCA1	HPCA0	HPCA: controls high-pass filter cut-off frequency(for Read)
1 0 1 1	TSTPD	0	0	HPCB4	HPCB3	HPCB2	HPCB1	HPCB0	HPCB: controls high-pass filter cut-off frequency(for Servo)
1 1 0 0	VGSHA3	VGSHA2	VGSHA1	VGSHA0	VGSLA3	VGSLA2	VGSLA1	VGSLA0	VGSHA: sets high-slice level of the gate generator(for Read) VGSLA: sets low-slice level of the gate generator(for read)
1 1 0 1	0	WDM	WPN2	WPN1	WPN0	WPE2	WPE1	WPE0	WDM: selects output type of 1-7 WDOUT (TTL / pseudo ECL) WPE / WPN: sets the write precompensation delays. (E/N)
1 1 1 0	AOE	0	PCN1	PCN0	VGSLB3	VGSLB2	VGSLB1	VGSLB0	AOE: AGCOUTX/Y outputs enable control PCN: power saving control register for the analog modules. VGSLB: sets low-slice level of the gate generator(for Servo)
1 1 1 1	TEST	0	MDC5	MDC4	MDC3	MDC2	MDC1	MDC0	MDC: TEST mode control register.

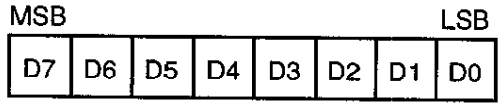
: these bits are set to "1" during reset time.

Register Descriptions (cont)

VCO Center Frequency Control register (VFC)

Address $h0 (at write = "C0" hex, at read = "80" hex),

VFC Register



VFC register is 8 bits long.
This register is used in multiple-zone recording to set the center frequency of the decode clock generator's VCO, the T/I converter's reference current, and the oscillation frequency of the encode clock generator's frequency synthesizer. Bit D7 is cleared when reset pin is asserted.

Resistors connected to the RFVCO and RSVCO lines set these values for the minimum data transfer rate. The VFC register raises these values in step of 1.56%, permitting 192 settings up to a maximum transfer rate 3.98 times of the minimum rate.

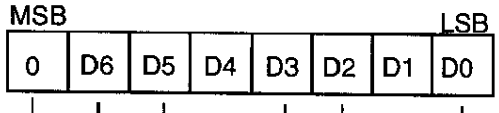
0 1 0 0 0 0 0 0 Minimum transfer rate (reference rate)

.
.
.

1 1 1 1 1 1 1 1 Maximum transfer rate (3.98 times speed)

Gain Control Register (GAC) : RFCA, GAC[5:0] for Read PLL synchronizer

Address $h1 (at write = "C2" hex, at read = "82" hex)



GAC[2:0]

Bits 2 to 0: Select the output current of the T/I converter to vary the gain. Eight gain settings are possible.

0 0 0 Minimum gain (L=0)

.
.
.

1 1 1 Maximum gain (L=7)

GAC[5:3]

Bits 5 to 3: Select the output current of the Charge pump to vary the gain. Eight gain settings are possible.

0 0 0 Minimum gain (P=1)

.
.
.

1 1 1 Maximum gain (P=8)

RFCA

Bit 6 selects the resistors that determine the attenuation ξ of the loop filter for the decode clock generator's VFO.

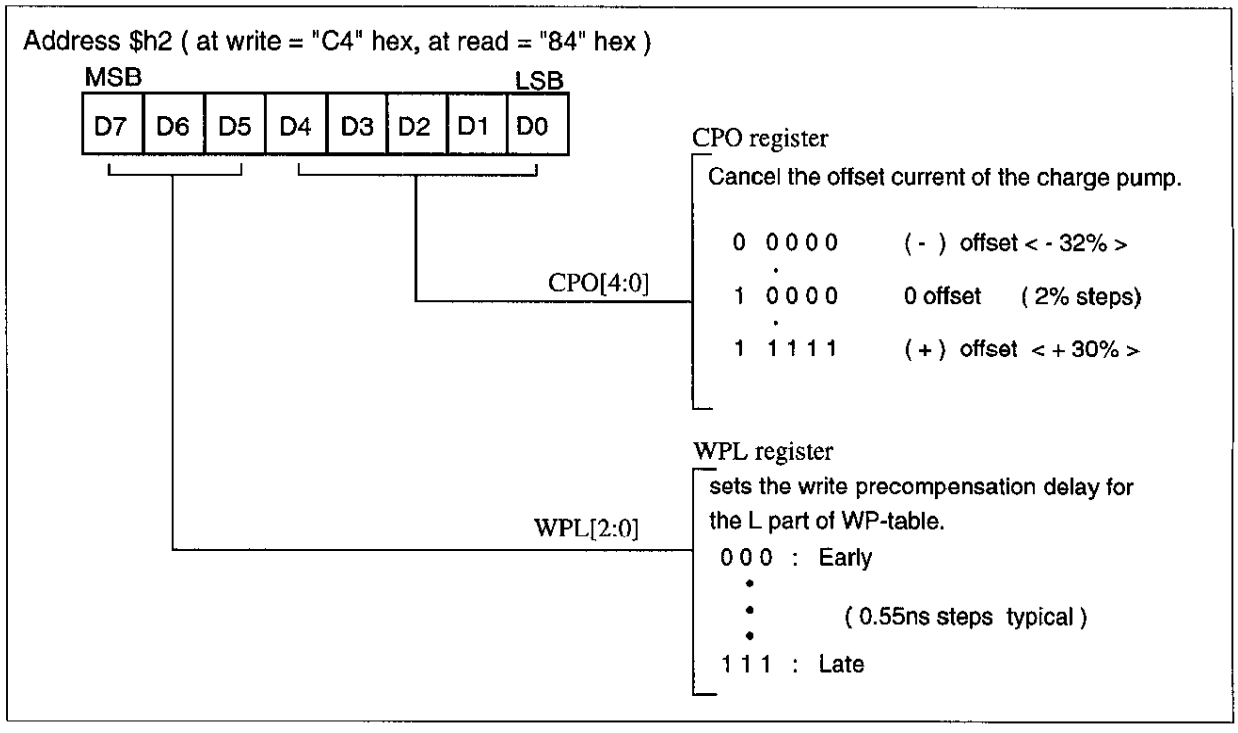
Bit 6 = 0: resistors connected to the FC0 and FC1 are selected

Bit 6 = 1: resistors connected to the FC2 and FC3 are selected

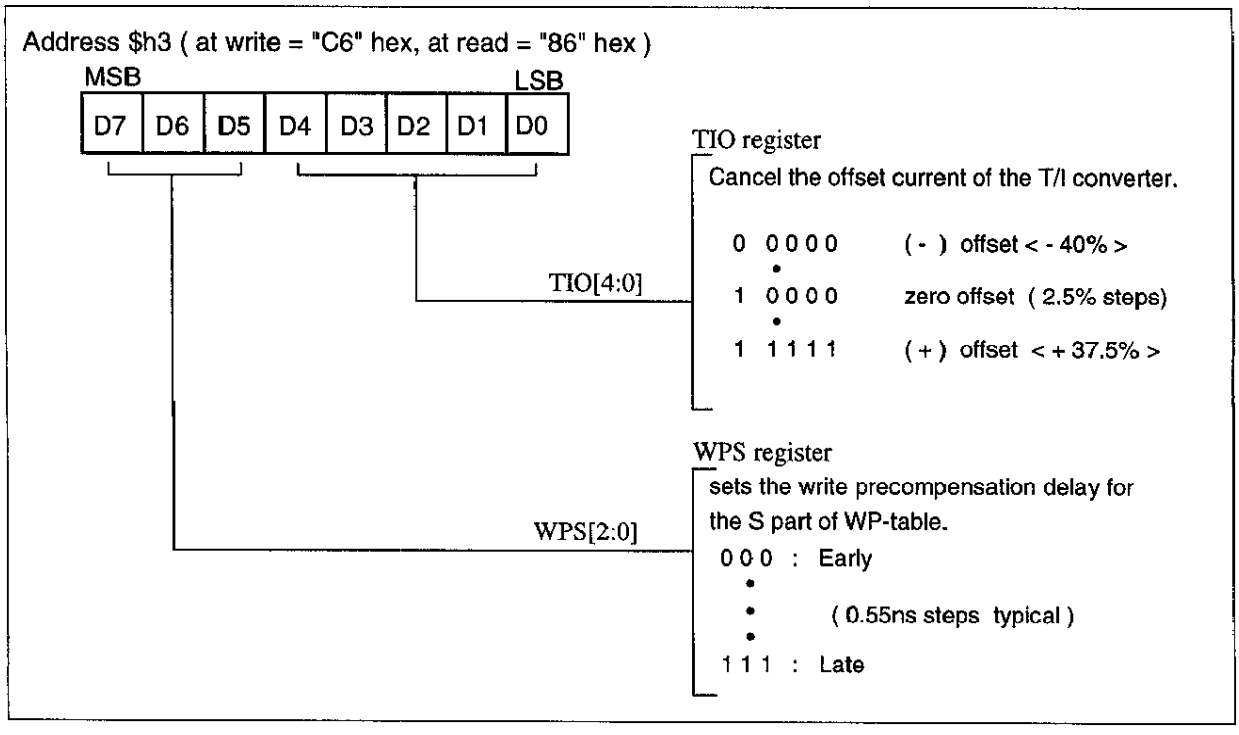
Unused bit. must be 0 when written.

Register Descriptions (cont)

Charge Pump Offset Control Register (CPO), Write Precompensation delay control Register (WPL)



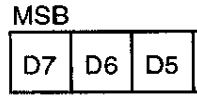
T/I Offset Control Register (TIO) , Write Precompensation delay control Register (WPS)



Register Descriptions (cont)

Window Fine Adjust Register WFA[2:0] and Window Adjust Register WAJ[4:0]

Address $h4 (at write = "C8" hex, at read = "88" hex)



WAJ register

WAJ[4:0]

This register adjusts the setting of the window. Window centering can be adjusted to 32 positions by an on-chip delay line. Bit D4 will always be cleared during reset. The microcontroller can center the window automatically with firmware by changing these values.

0 0000
.
.
0 1111 (-) negative delay adjustment
1 0000 (0.67ns steps typical)
1 0001
. (+) positive delay adjustment
.
1 1111

WFA register

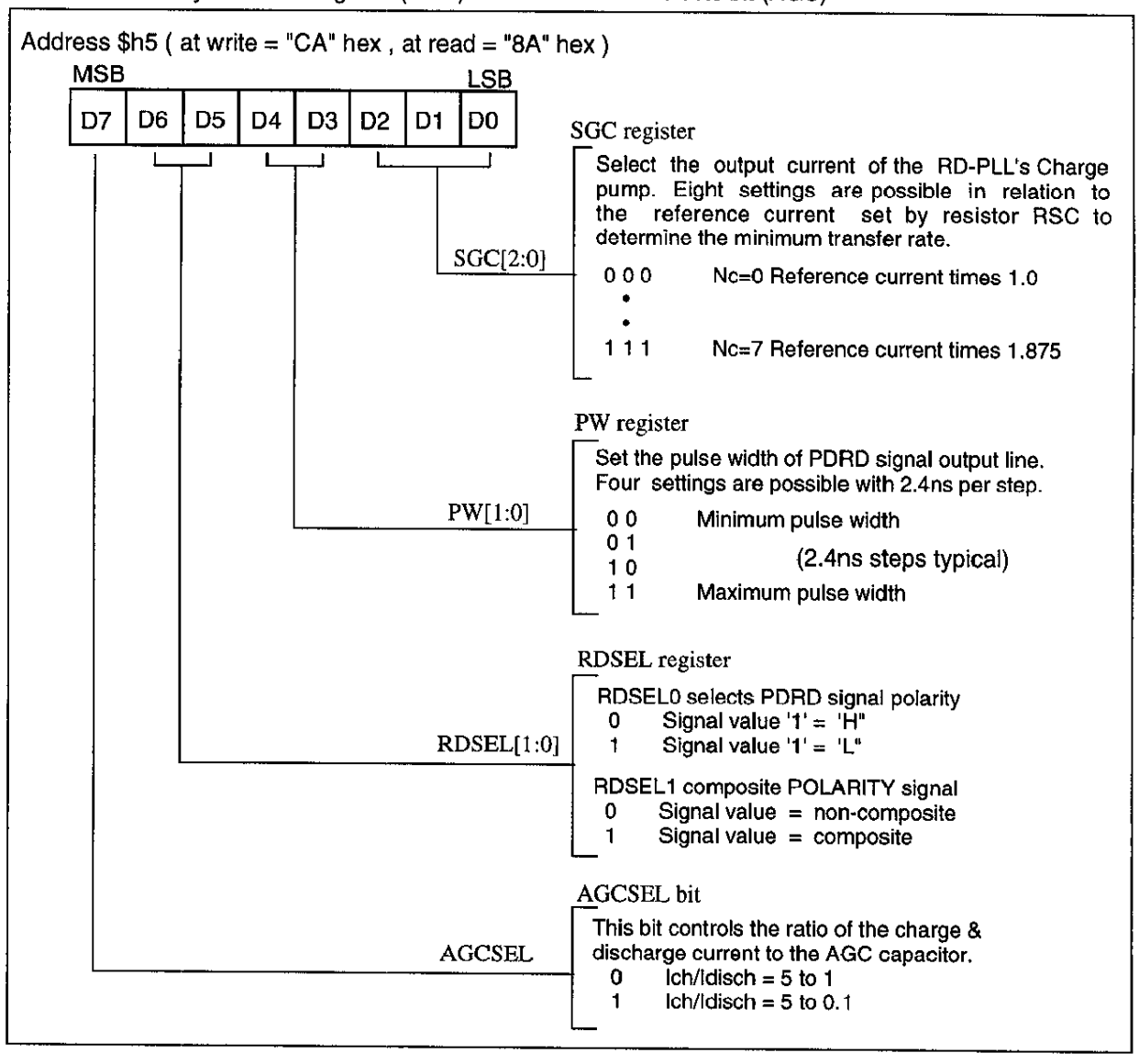
WFA[2:0]

This register adjusts eight setting of the window fine adjust circuit. The register setting adds fine delay to the Window adjustment circuit.

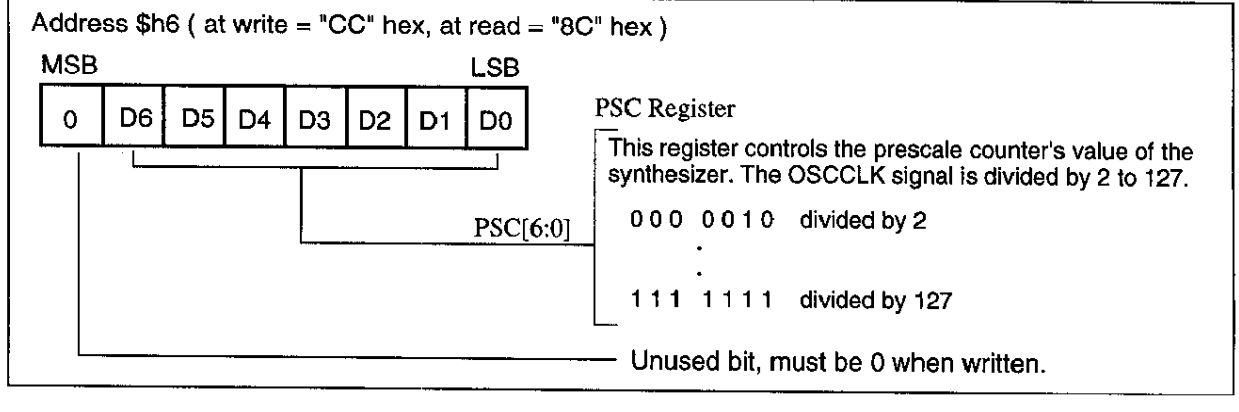
0 0 0 Minimum delay
0 0 1 Initial delay (4.9ns typical)
•
• (0.25ns steps typical)
1 0 1 Maximum delay

Register Descriptions (cont)

RD-PLL Gain Control Register (SGC), Read data Pulse Width Control Register (PW), Read data Polarity Control Register (RPC) and AGC Mode Selects bit (AGS)

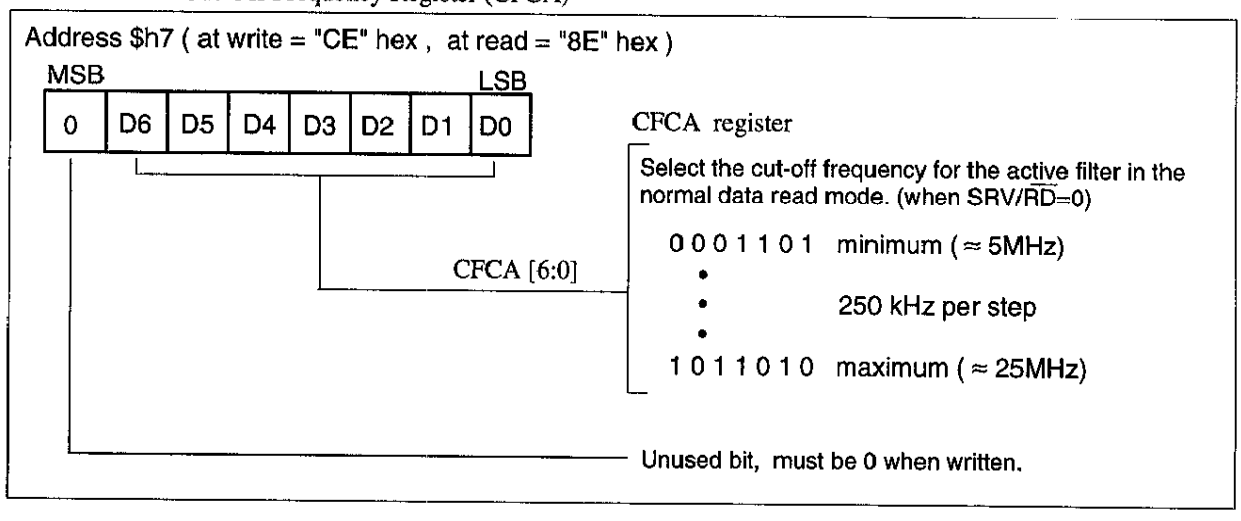


Prescaler of the Synthesizer Control Register (PSC) [M value]

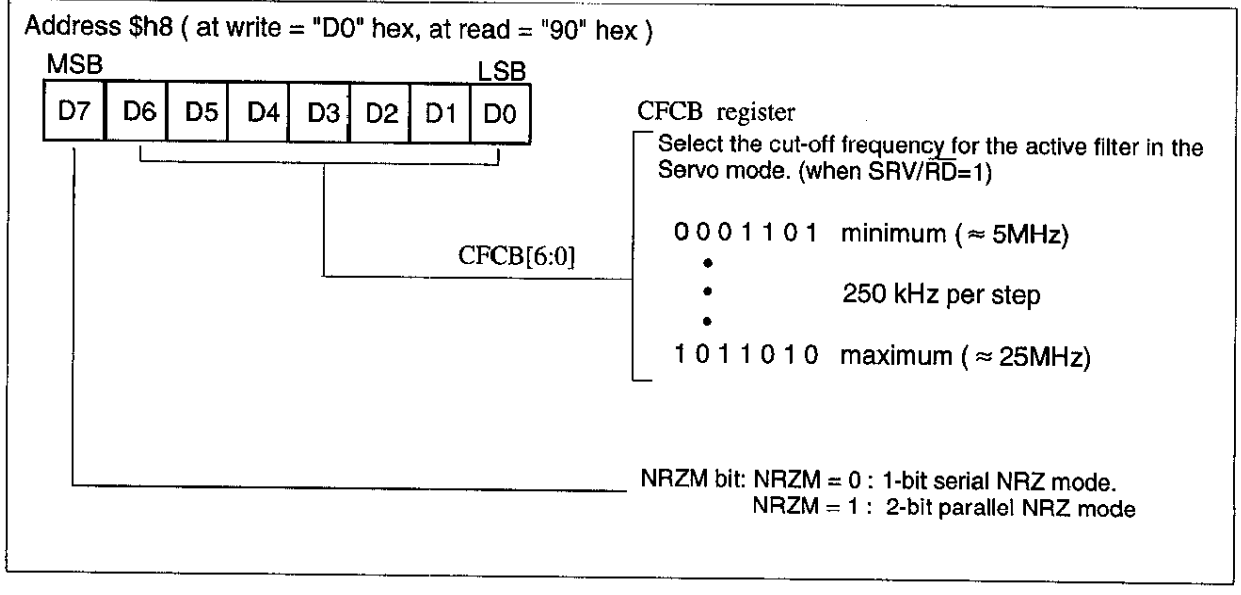


Register Descriptions (cont)

Read Mode AF Cut-Off Frequency Register (CFCA)



NRZ Data mode select bit (NRZM), Servo Mode AF Cut-Off Frequency Register (CFCB)



Register Descriptions (cont)

Unlock Detect Register (ULD) and Boost Level Control Register (BLC)

Address $h9 (at write = "D2" hex, at read = "92" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

BLC register

This register sets the boost amplifier's gain of the active filter for the equalization.

BLC[4:0]

0 0000 Minimum gain
.
.
1 1111 Maximum gain

ULD register

Select the unlocked detect gain for the RD-PLL synthesizer to activate the ULD~ output when unlock condition occurs.

ULD[1:0]

00: 2 OSCCLK
01: 4 OSCCLK
10: 6 OSCCLK
11: 8 OSCCLK

TESTBF

When this bit sets "1" , $\overline{\text{SYNCRD}}$(44Pin), $\overline{\text{DLYRD}}$(42Pin), $\overline{\text{DLYCLK}}$(41Pin) are output mode. Normaly this bit sets "0".

High-Pass Filter Cutoff Frequency Control Register (HPCA)

Address $hA (at write = "D4" hex, at read = "94" hex)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

HPCA Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit in the normal data read mode. (when SRV/$\overline{\text{RD}}$=0)The register changes it by 6.25% step.

HPCA[4:0]

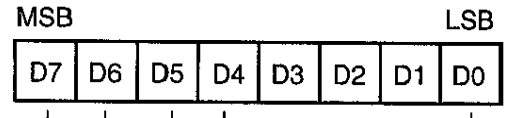
0 1111 Maximum cutoff frequency (193.75%)
•
•
0 0001
0 0000 Center cutoff frequency
1 1111 (100%, depend on CFCA)
•
•
1 0000 Miniimum cutoff frequency (50%)

Unused bit, must be 0 when written.

Register Descriptions (cont)

High-Pass Filter Cutoff Frequency Control Register (HPCB)

Address $hB (at write = "D6" hex , at read = "96" hex)



HPCB Register

This register controls the cutoff frequency of the high-pass filter in the active filter circuit in the Servo mode.
(when SRV/RD=1)The register changes it by 6.25% step.

HPCB[4:0]

0 1 1 1 1 Maximum cutoff frequency (193.75%)
•
•
0 0 0 0 1
0 0 0 0 0 Center cutoff frequency
1 1 1 1 1 (100%, depend on CFCB)
•
•
1 0 0 0 0 Miniimum cutoff frequency (50%)

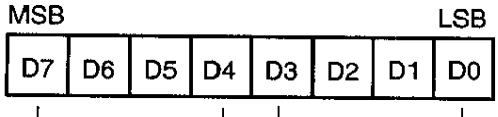
Unused bit, must be 0 when written.

TSTPD

When this bit sets "1", PDRD output is enable.

High-Slice Level Register (VGSHA), low-Slice Level Register (VGSLA)

Address $hC (at write = "D8" hex, at read = "98" hex)



VGSLA Register

These are input to the internal DAC using VCOM as refenrece source to generate the programmable Low-Slice level for the Pulse detection circuit in the read mode. (when SRV/RD="L")

VGSLA[3:0]

0 0 0 0 Minimum high-slice level (0% of Vpeak)
.
.
1 1 1 1 Maximum high-slice level (100% of Vpeak)

VGSHA Register

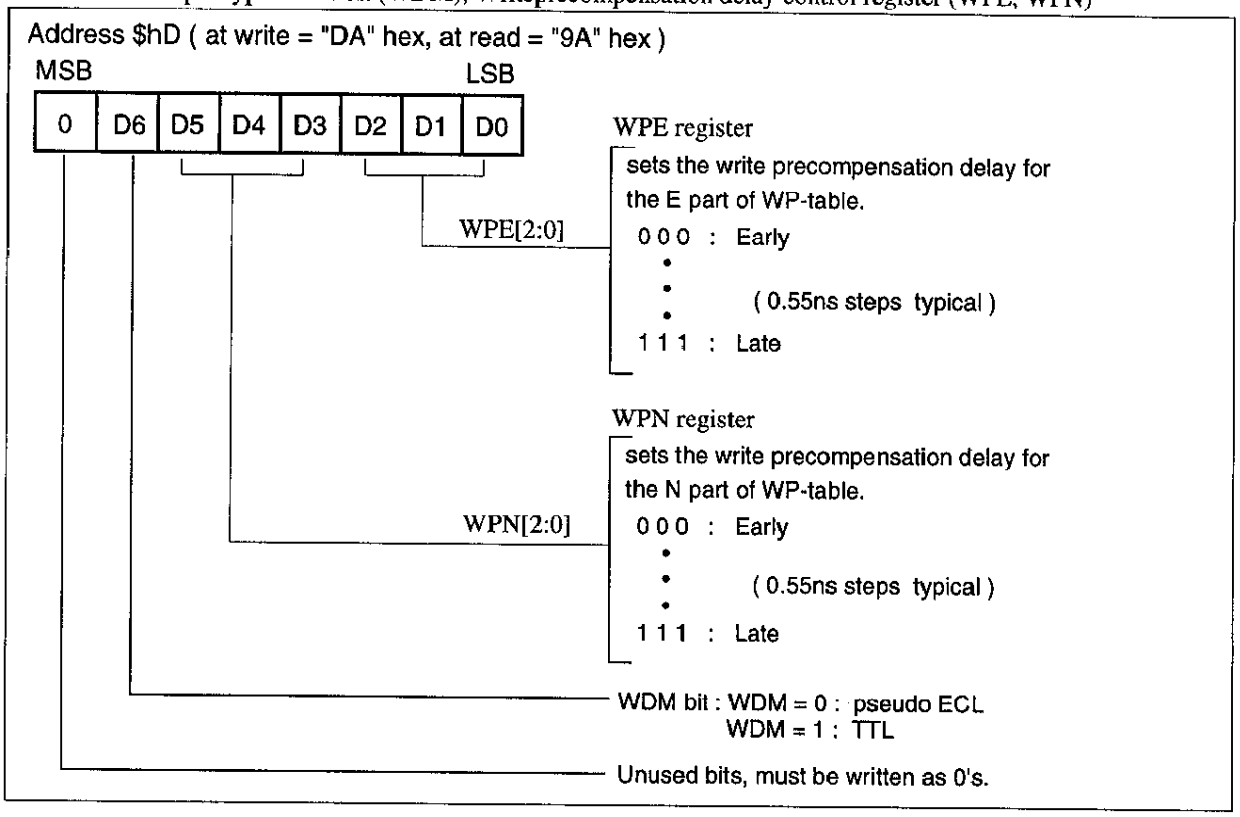
These are input to the internal DAC using VCOM as refenrece source to generate the programmable High-Slice level for the Pulse detection circuit both in the read and servo mode.

VGSHA[3:0]

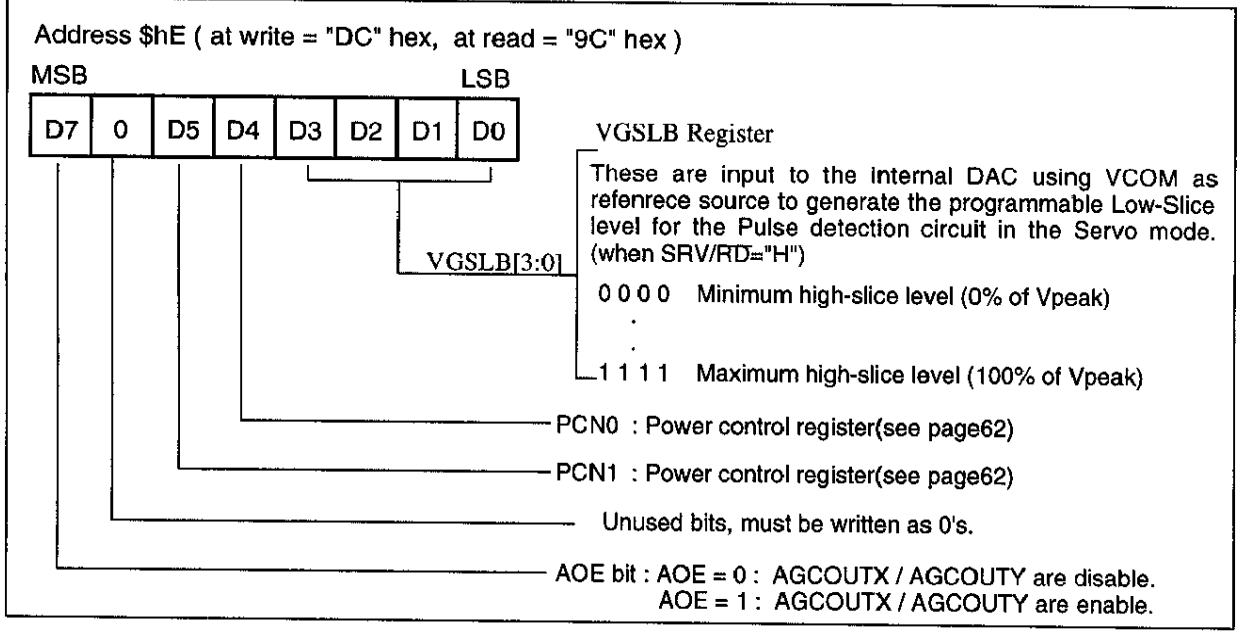
0 0 0 0 Minimum high-slice level (0% of Vpeak)
.
.
1 1 1 1 Maximum high-slice level (100% of Vpeak)

Register Descriptions (cont)

1-7WDOUT output type select bit (WDM), Writeprecompensation delay control register (WPE, WPN)



AGCOUTX/Y enable control bit (AOE), Power Control Register (PCN)



Register Descriptions (cont)

Test Mode Control Register (MDC)

Address = $hF

MSB							LSB
D7	0	D5	D4	D3	D2	D1	D0

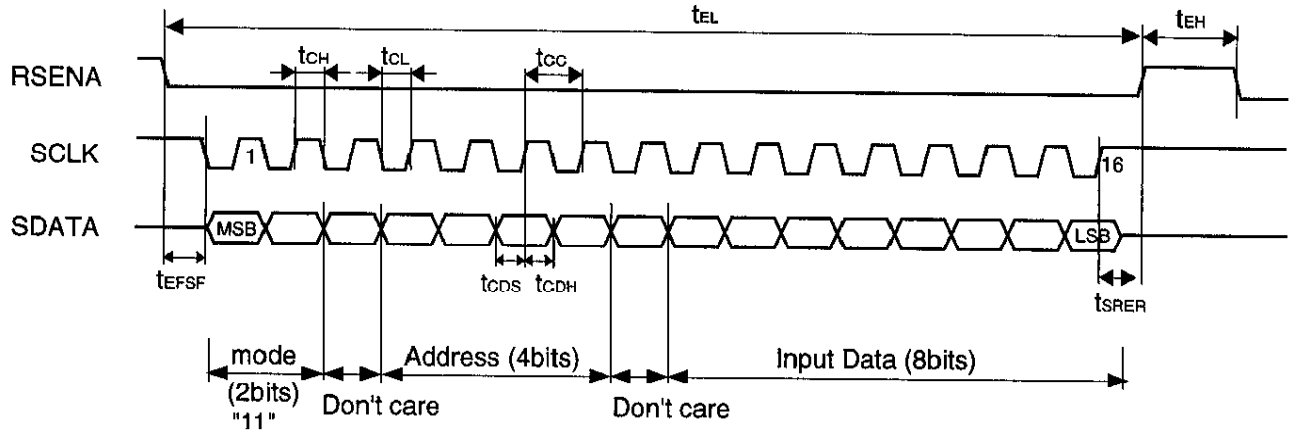
MDC[4:0] — *Reserved*

Unused bit, must be written as 0.

TEST: when set to "1", it enables the internal test mode.

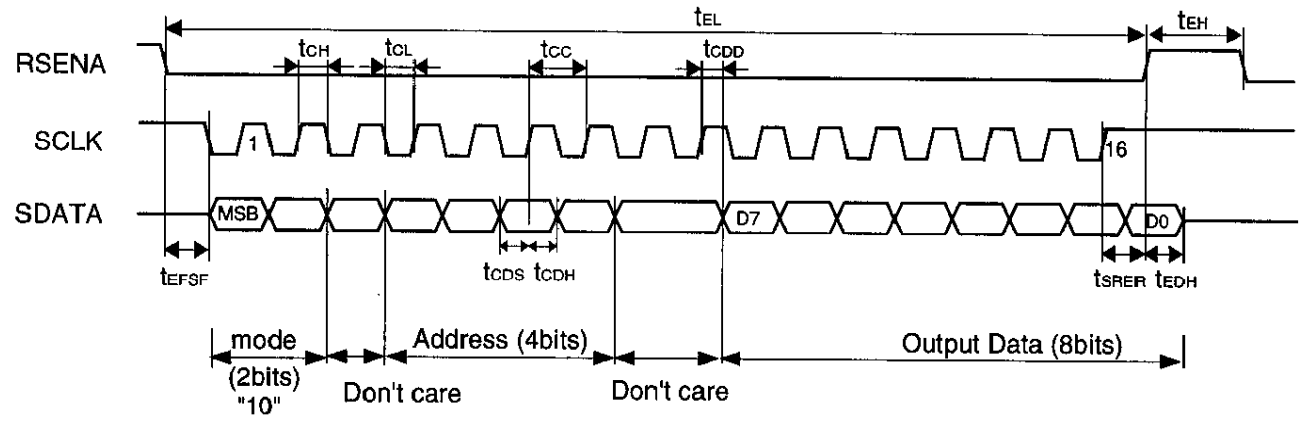
7. Read/Write timing of the control registers

< Write >



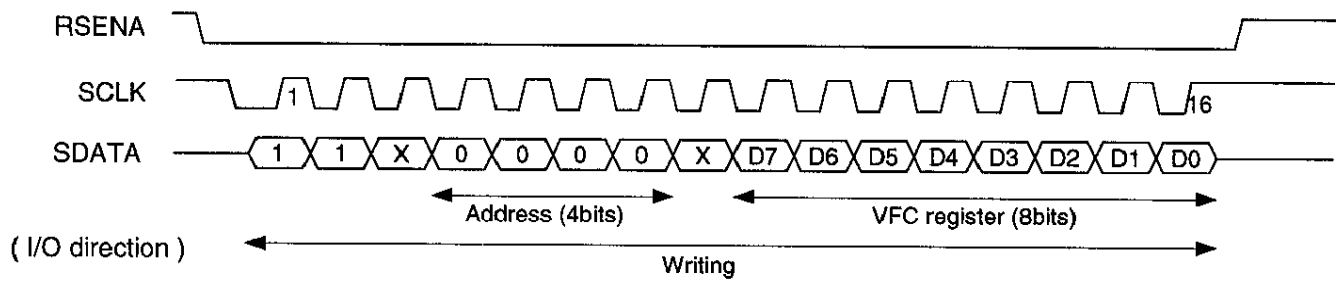
Read/Write timing of the control registers (cont)

< Read >

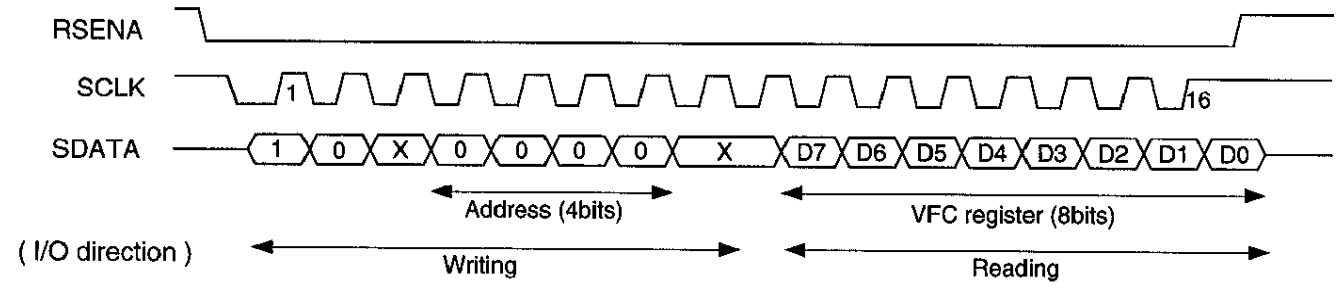


Write and read registers (cont)

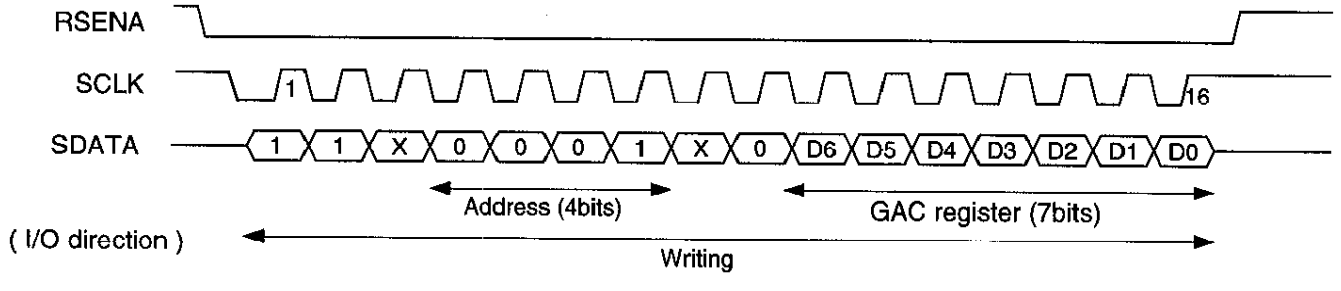
Write to VFC register



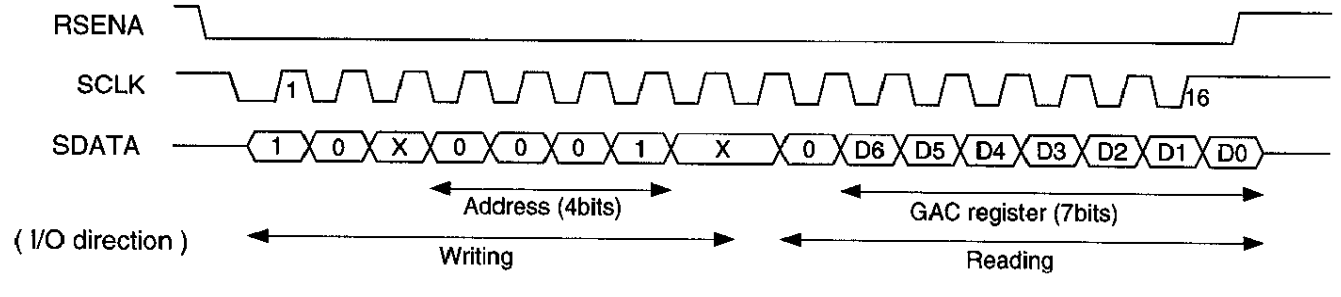
Read from VFC register



Write to GAC register

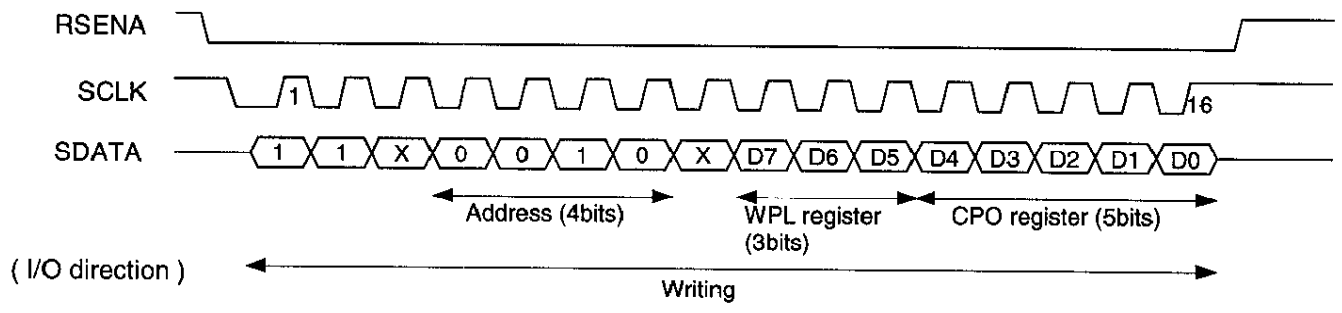


Read from GAC register

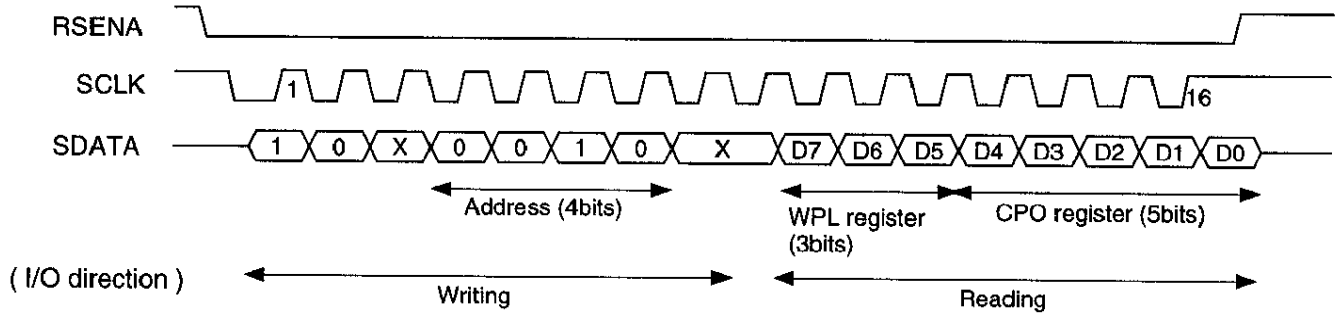


Write and read registers (cont)

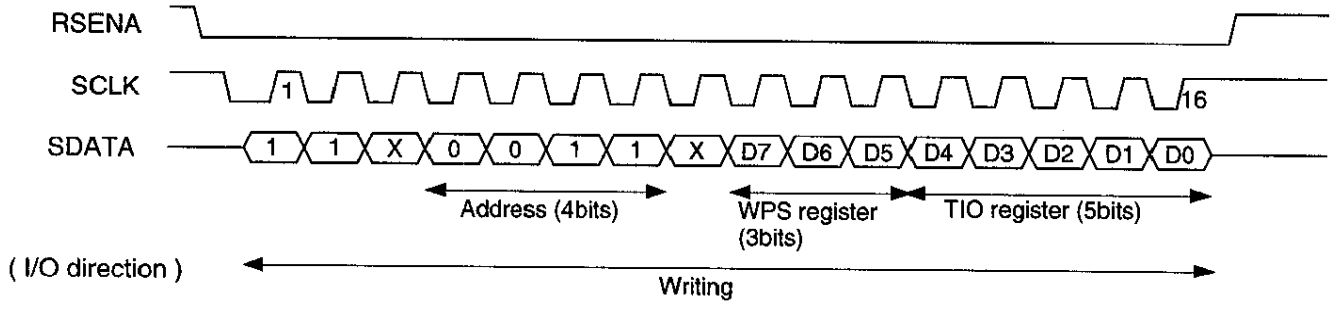
Write to WPL & CPO register



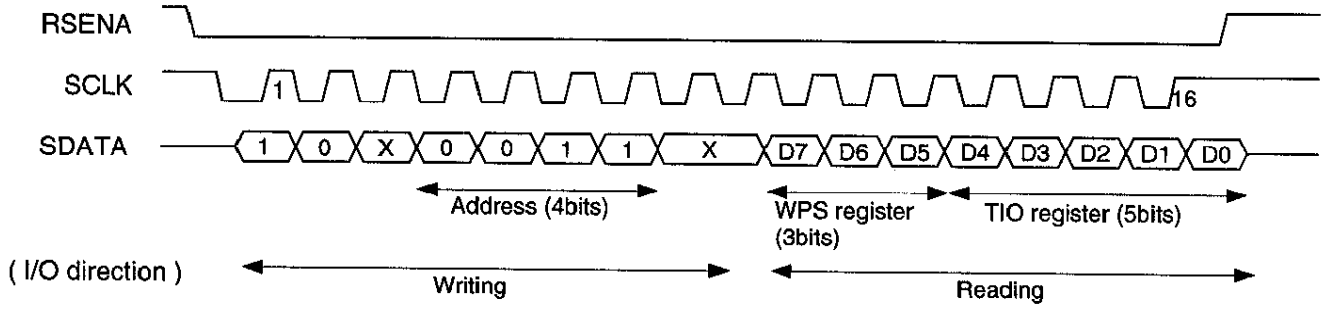
Read from WPL &CPO register



Write to WPS & TIO register

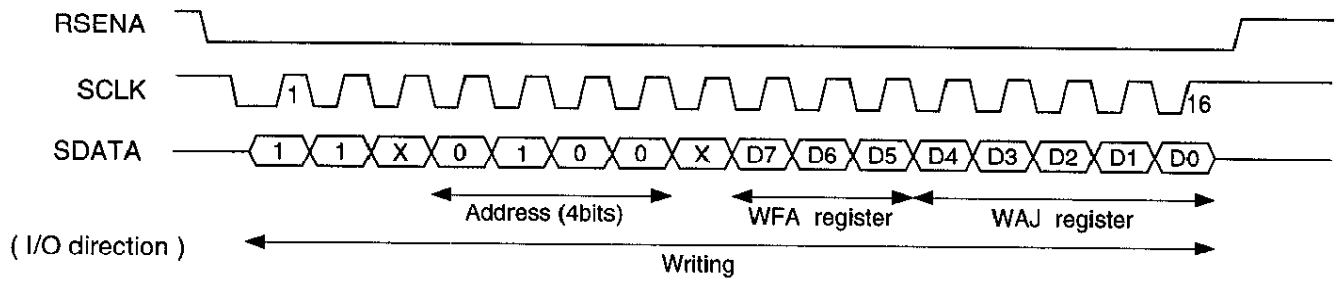


Read fromWPS & TIO register

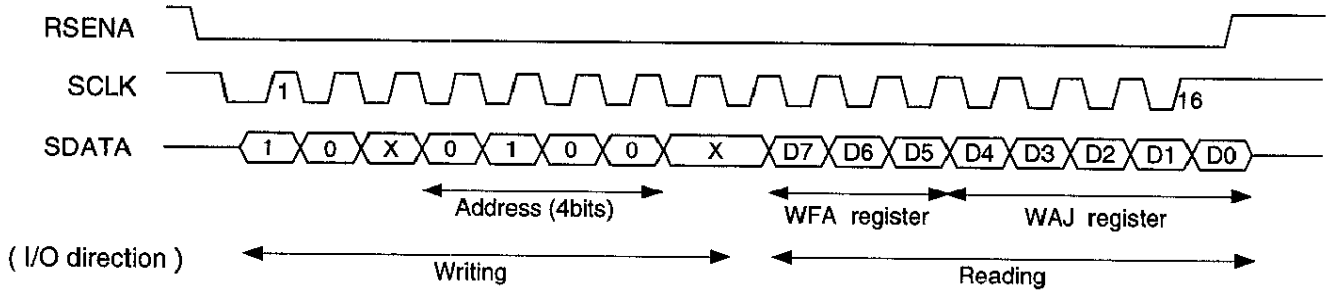


Write and read registers (cont)

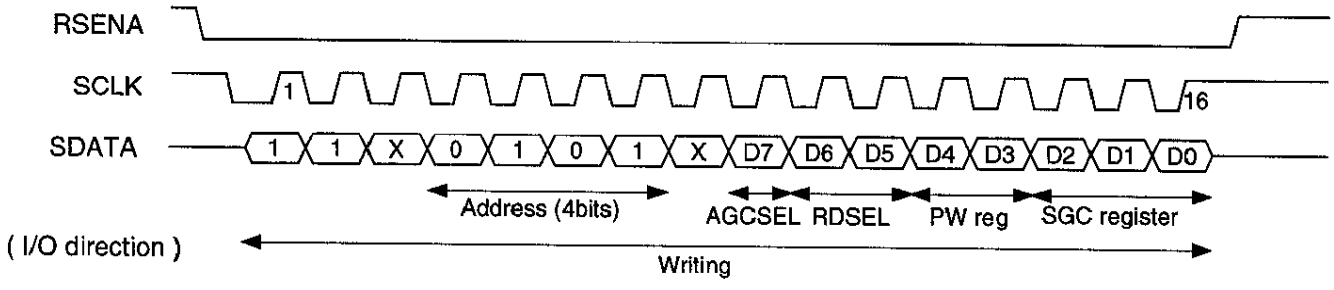
Write to WFA & WAJ register



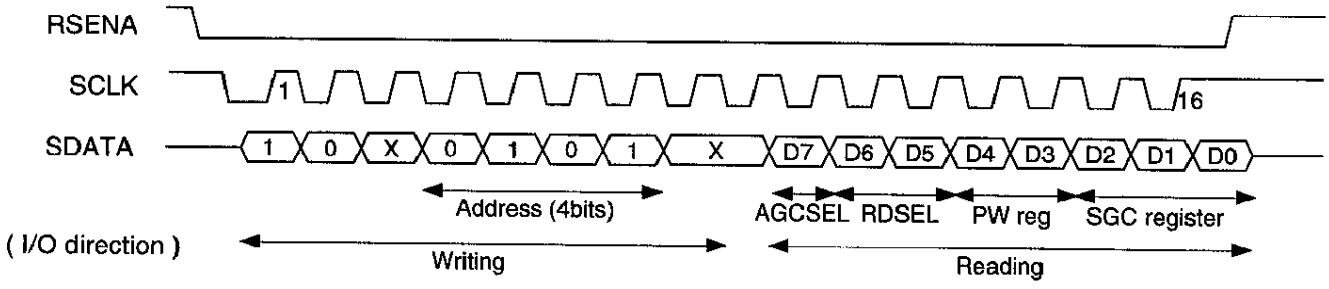
Read from WFA & WAJ register



Write to AGCSEL bit, RDSEL, PW & SGC register

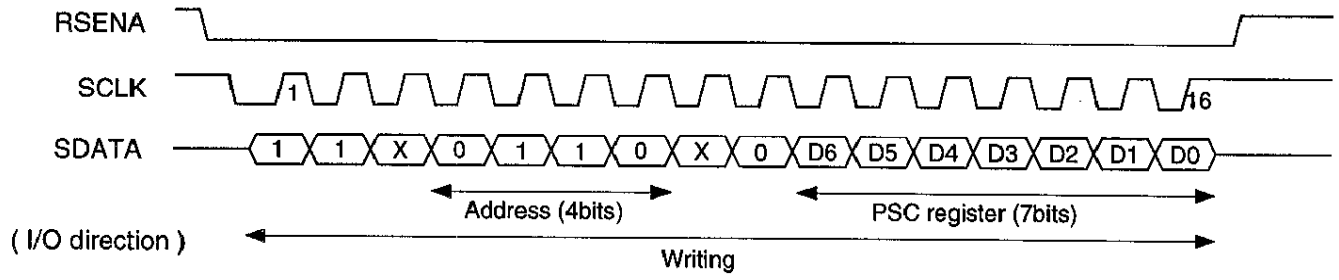


Read from AGS bit, RDS, PW & SGC register

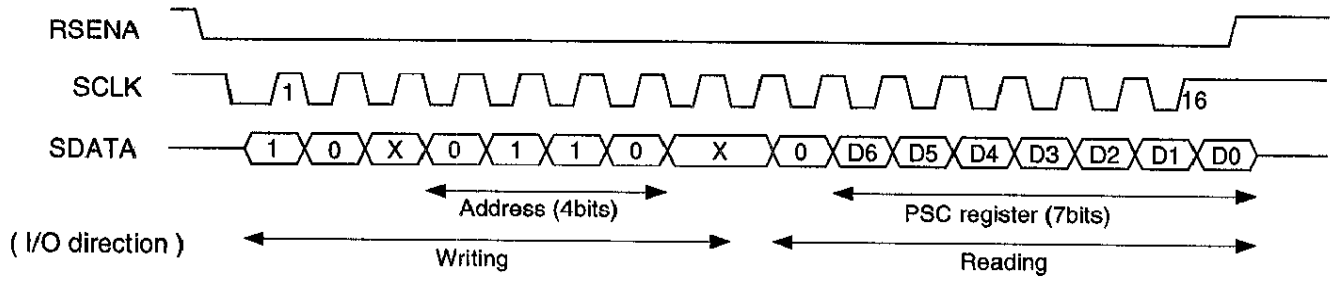


Write and read registers (cont)

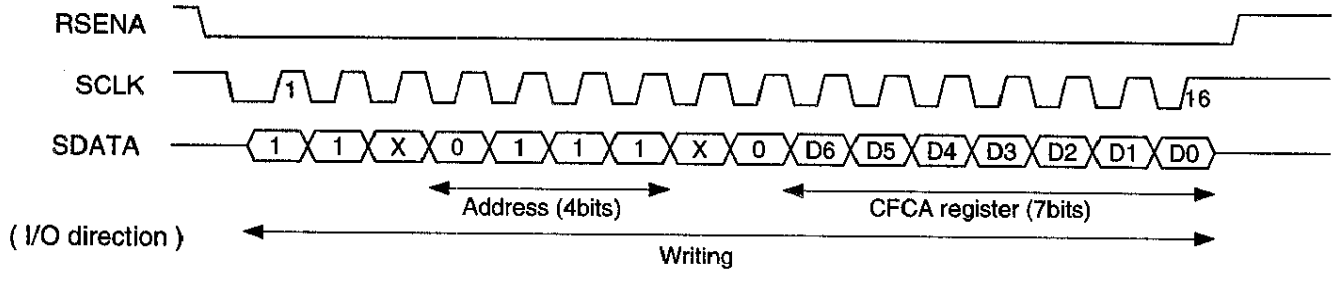
Write to PSC register



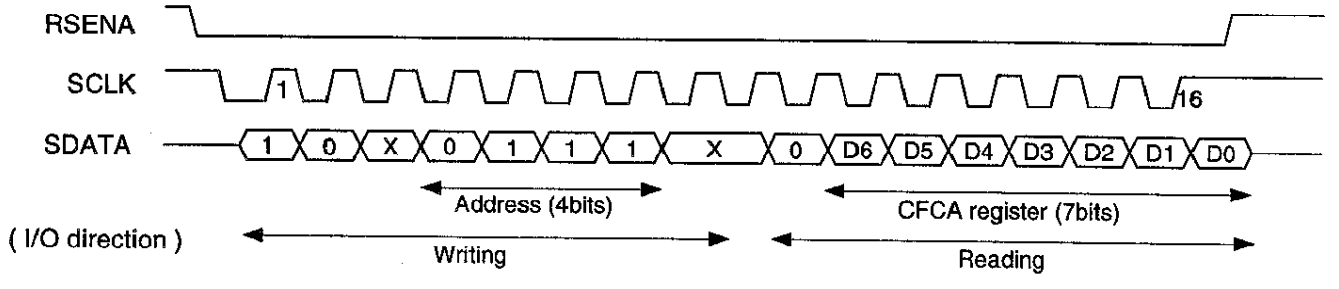
Read fromPSC register



Write to CFCA register

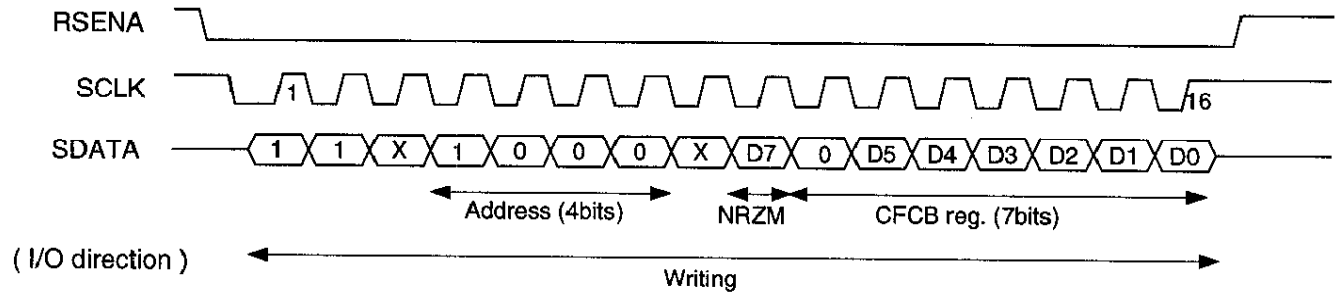


Read from CFC register

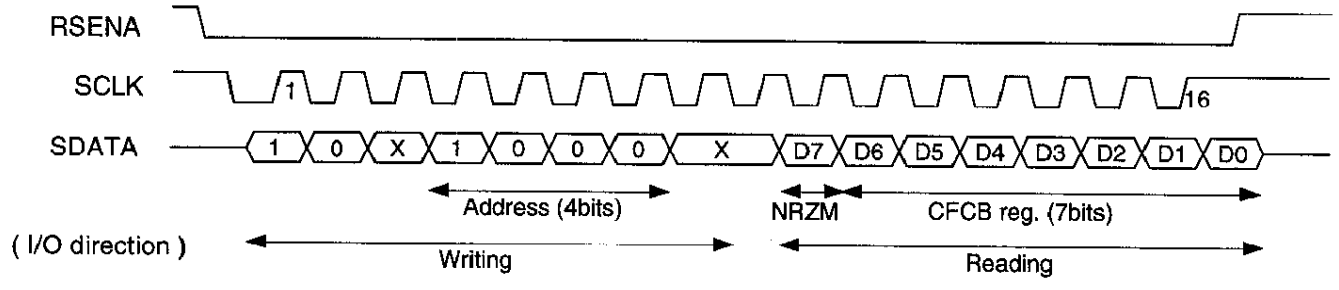


Write and read registers (cont)

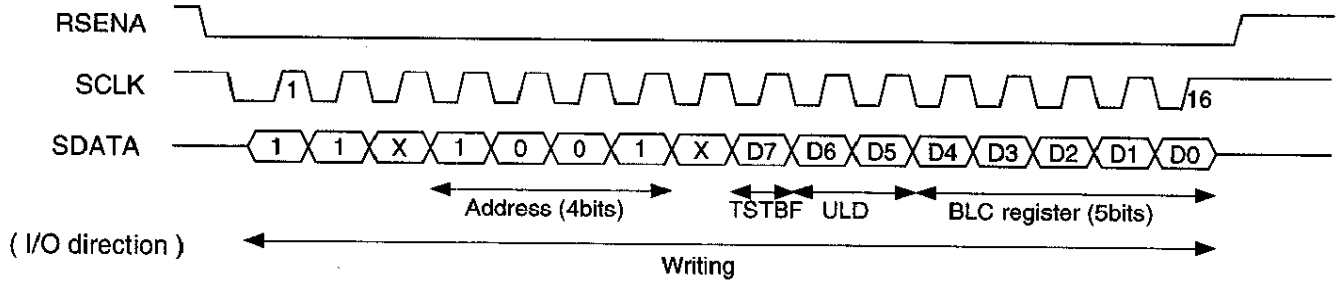
Write to NRZM bit & CFCB register



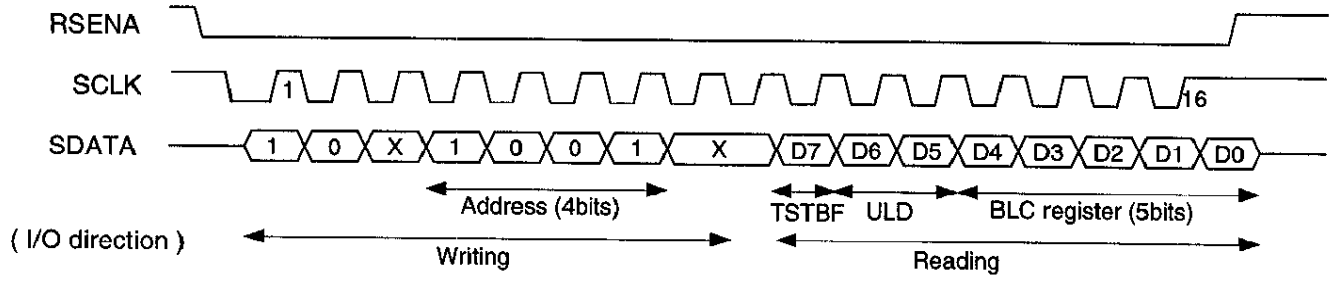
Read from NRZM bit & CFCB register



Write to ULD & BLC register

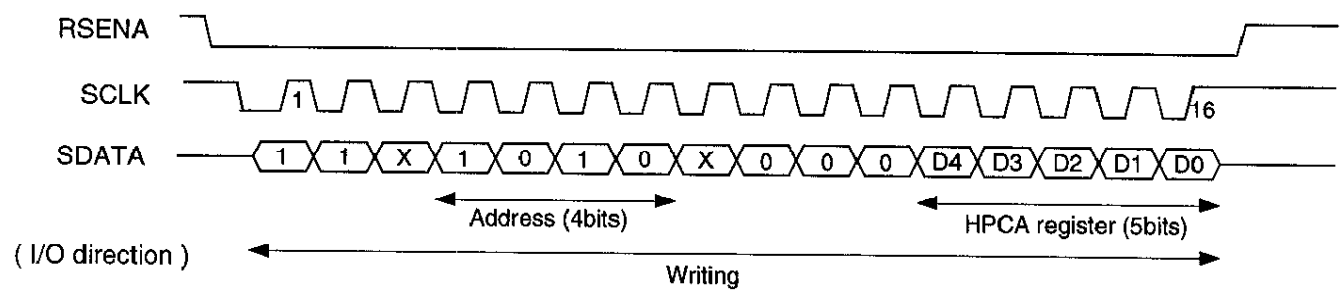


Read from ULD & BLC register

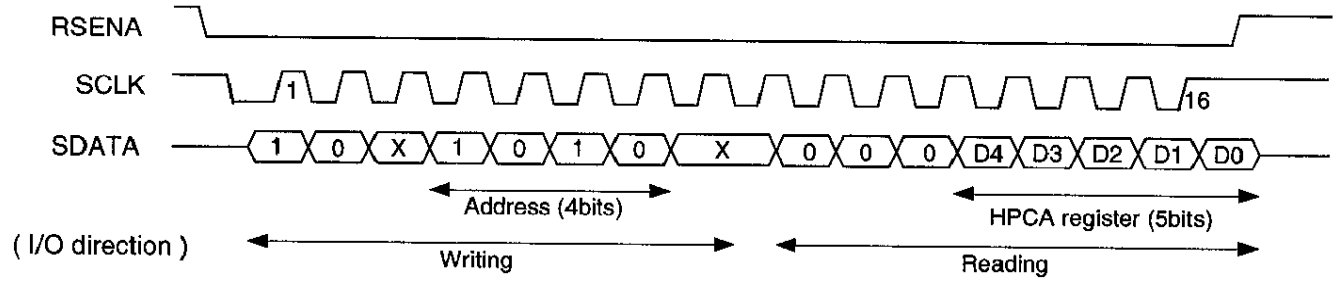


Write and read registers (cont)

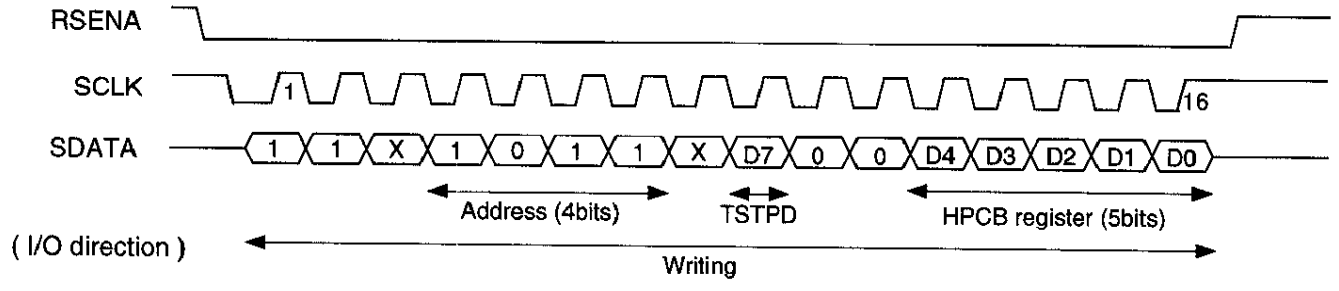
Write to HPCA register



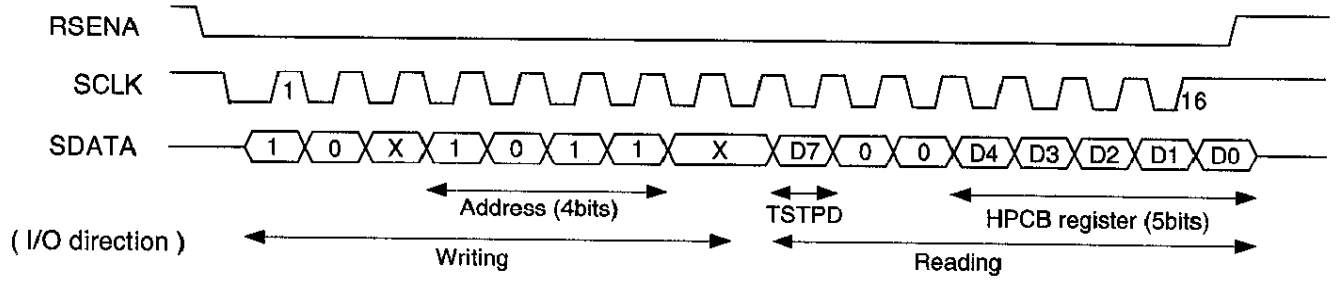
Read from HPCA register



Write to HPCB register

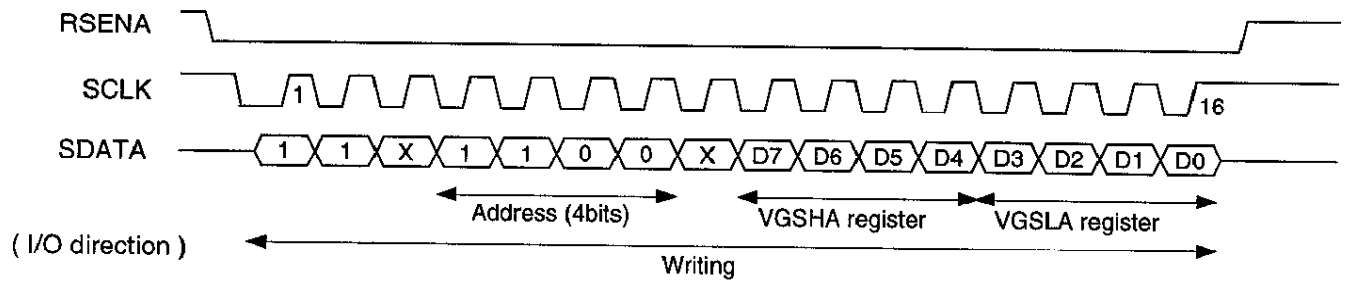


Read from HPCB register

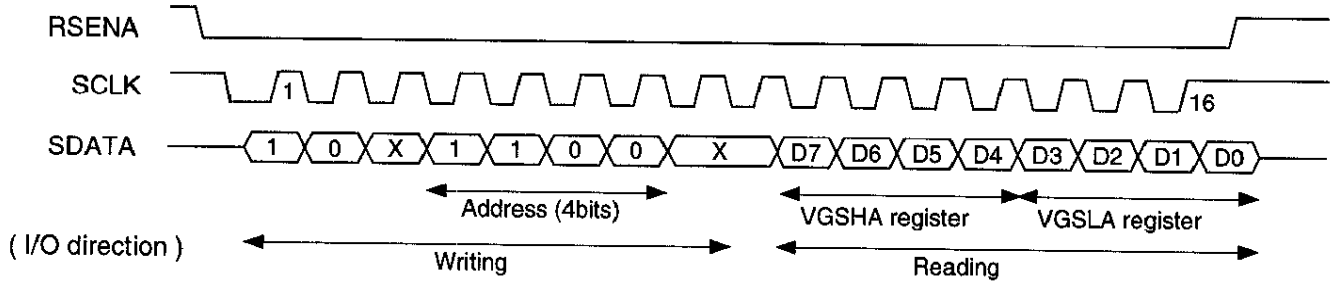


Write and read registers (cont)

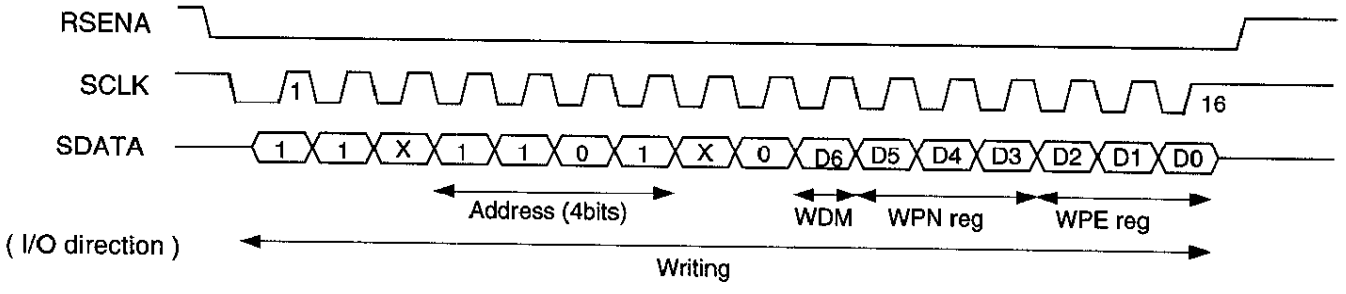
Write to VGSHA & VGSLA register



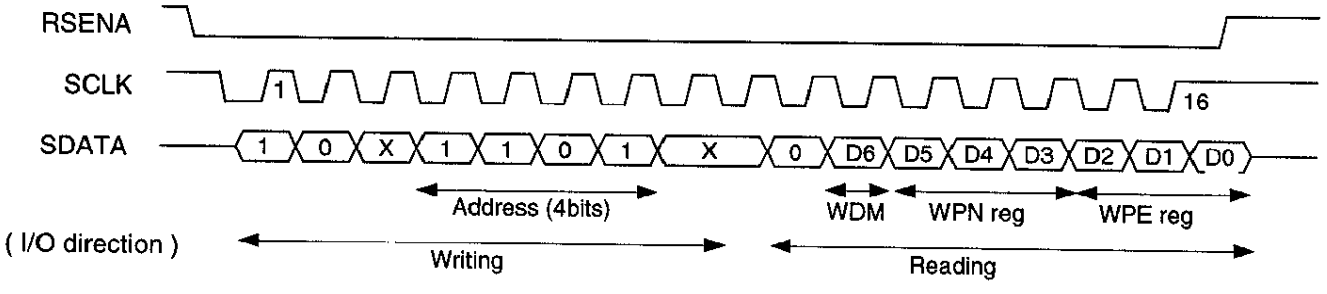
Read from VGSHA & VGSLA register



Write to WDM bit, WPN & WPE register

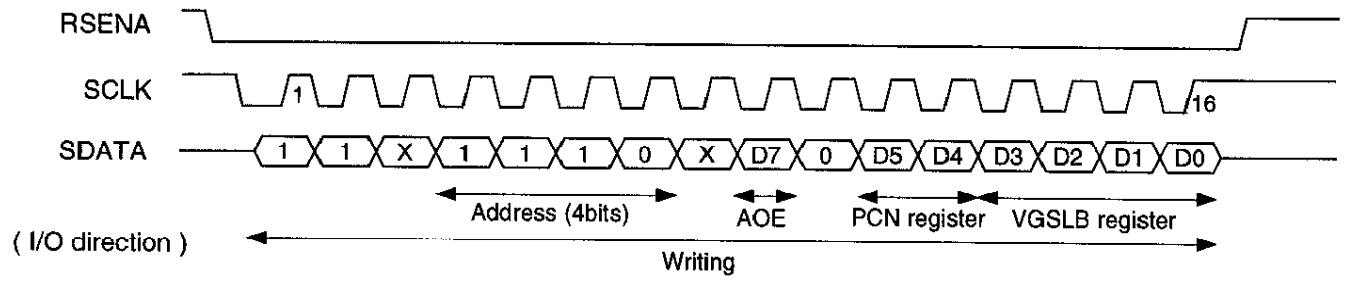


Read from WDM bit, WPN & WPE register

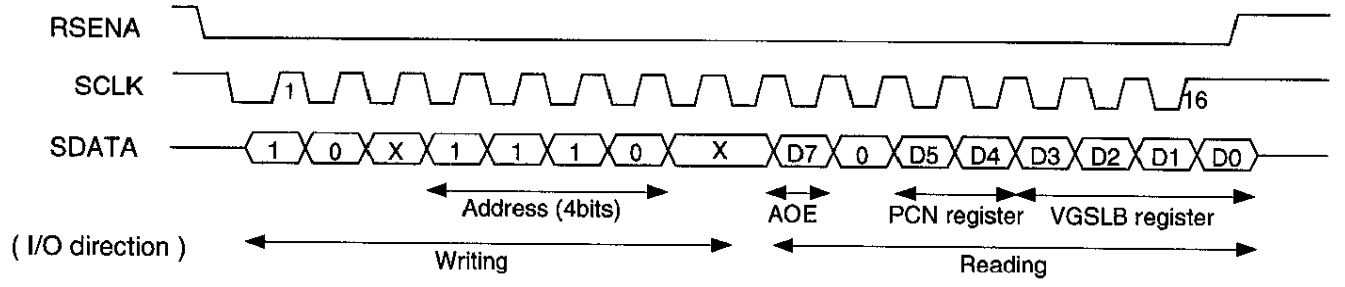


Write and read registers (cont)

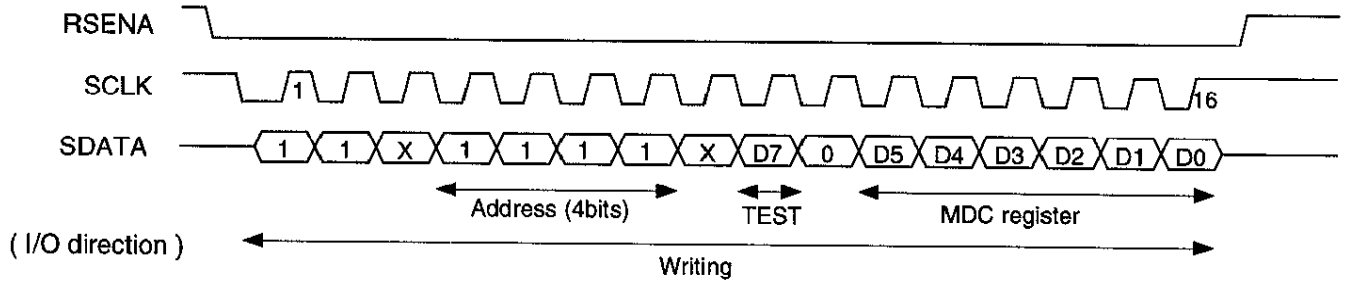
Write to AOE bit, VGSLB & PCN register



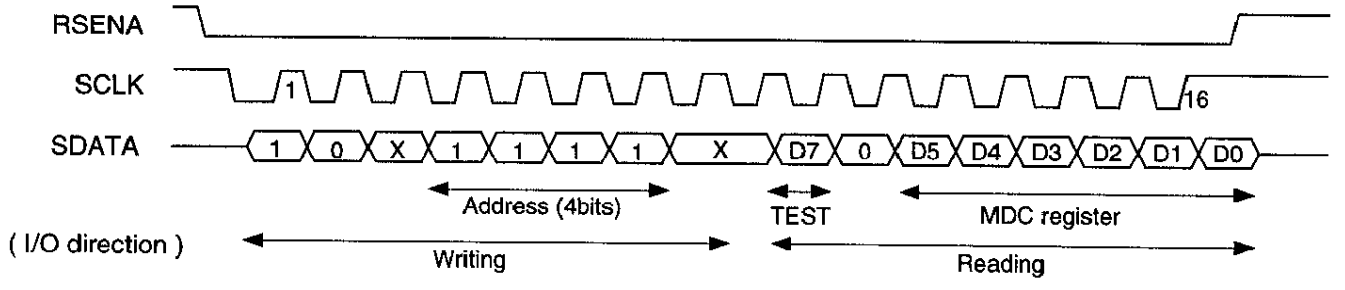
Read from AOE bit, VGSLB & PCN register



Write to MDC register



Read from MDC register



9. 1-7 ENDEC

Encoder and Decoder

The encoder converts an NRZ signal to a (1,7) encoding, and the decoder converts a (1,7) signal back to an NRZ signal. The conversion table is shown in Table4.

The NRZ signal is encoded after being inverted. The inverted $\overline{\text{NRZ}}$ signal is encoded according to the conversion rules shown in figure5.

Therefore the disk controller should input the sequence " 0000..." in the sync region. This will be converted to the (1,7) encoding 3T pattern "100100...".

The NRZ signal is encoded after being inverted. For example, if the $\overline{\text{NRZ}}$ data 00 is to be (1,7) encoded, it is first inverted to 11.

Table4 Encoding Table (NRZ to (1,7) Code)

No.	Last Bit of the Previous (1,7) Code	$\overline{\text{NRZ}}$ Data Bit				(1,7) Code Bits (C_2,C_3,C_4)		
		Current (D_1,D_2)		Next (D_3,D_4)				
1	0	1	0	0	X	1	0	1
2	0	1	0	1	X	0	1	0
3	0	1	1	0	0	0	1	0
4	0	1	1	$\overline{0\ 0}$		1	0	0
5	0	0	0	0	X	0	0	1
6	0	0	0	1	X	0	0	0
7	0	0	1	0	X	0	0	1
8	0	0	1	1	X	0	0	0
9	1	0	0	0	X	0	0	1
10	1	0	0	1	X	0	1	0
11	1	0	1	0	0	0	1	0
12	1	0	1	$\overline{0\ 0}$		0	0	0

$\overline{0\ 0}$: Anything other than 0 0
X : Don't care

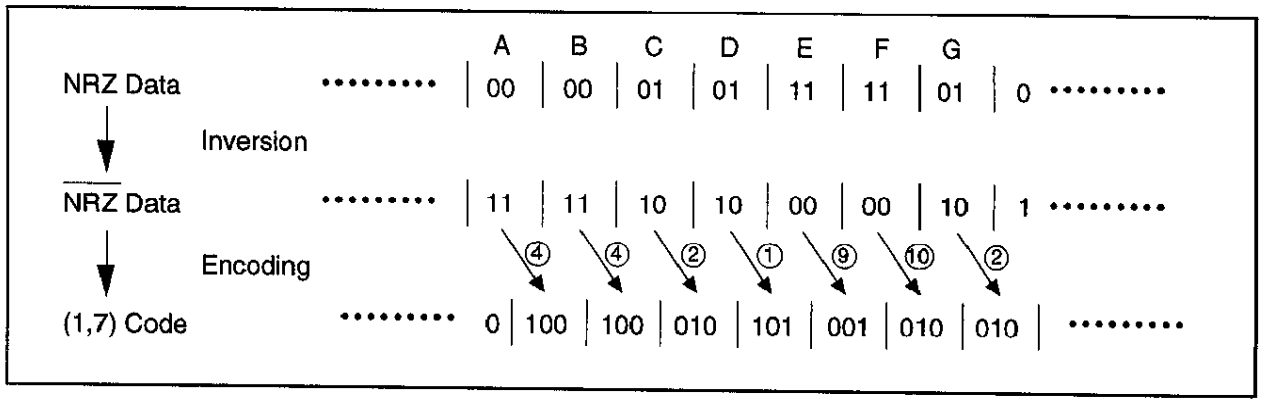


Fig.5 Shows an Example of NRZ to (1,7) Code Conversion.

Next, since the last bit of the previous conversion result A (100) was 0, and the next state of the NRZ data C is 0 1($\overline{C}$= 10), the NRZ data B (00) is converted to the (1,7) code 100.

In decoding the (1,7) code I (=100) to NRZ data (see Figure6), since the previous data H was 100 and the next data J is 010, the decoding table gives 11 as the $\overline{NRZ}$ data. Inverting this gives the NRZ data 00, which is then output.

Table 5 Decoding Table ((1,7) Code to NRZ)

No.	(1,7) Code Bits									$\overline{NRZ}$ Data Bit	
	Previous			Current			Next				
1	X	1	0	0	0	0	X	X	X	0	0
2	X	0	0	0	0	0	X	X	X	0	1
3	X	X	X	1	0	0	X	X	X	1	1
4	X	X	0	0	1	0	$\overline{0\ 0}$		X	1	0
5	X	X	0	0	1	0	0	0	X	1	1
6	X	X	X	1	0	1	X	X	X	1	0
7	X	0	0	0	0	1	X	X	X	0	1
8	X	1	0	0	0	1	X	X	X	0	0
9	X	X	1	0	0	1	X	X	X	0	0
10	X	X	1	0	1	0	$\overline{0\ 0}$		X	0	0
11	X	X	1	0	1	0	0	0	X	0	1
12	X	X	1	0	0	0	X	X	X	0	1

$\overline{0\ 0}$: Anything other than 0 0
X : Don't care

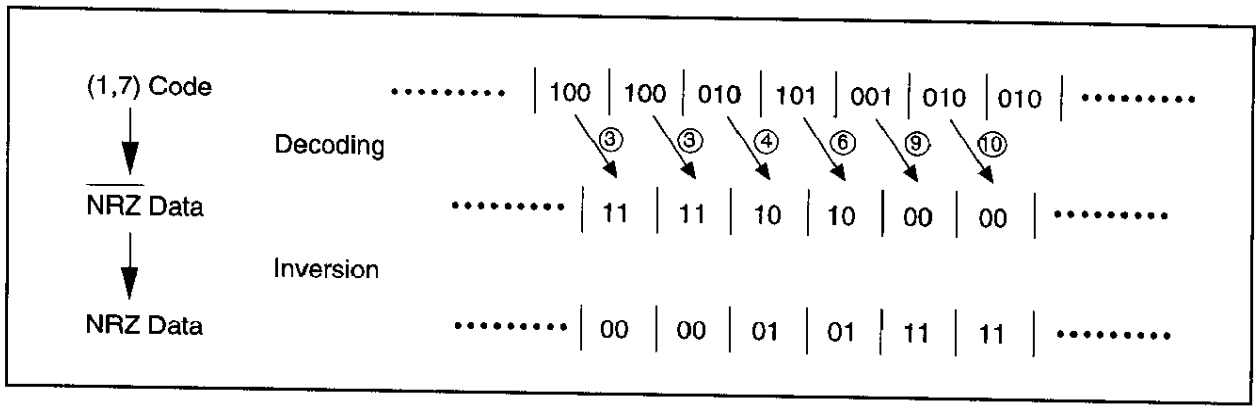
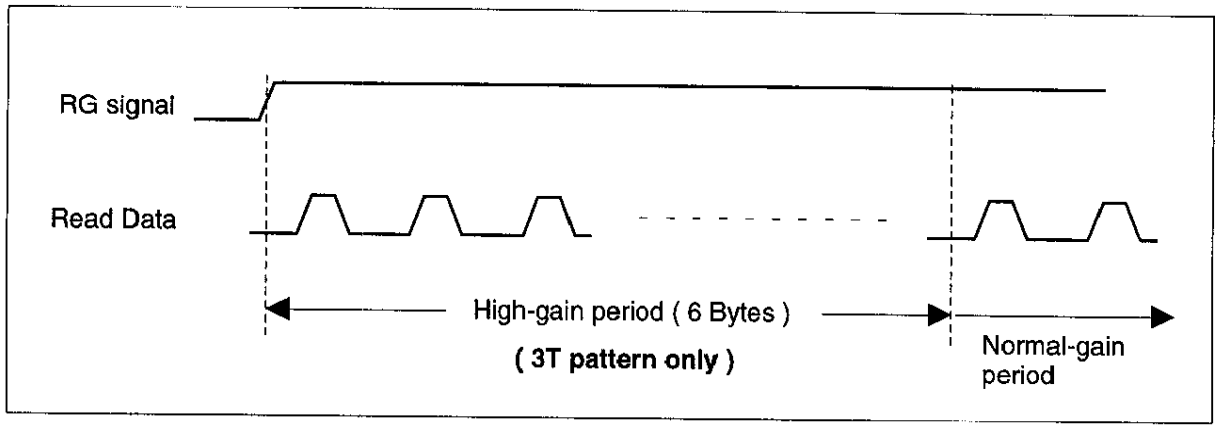


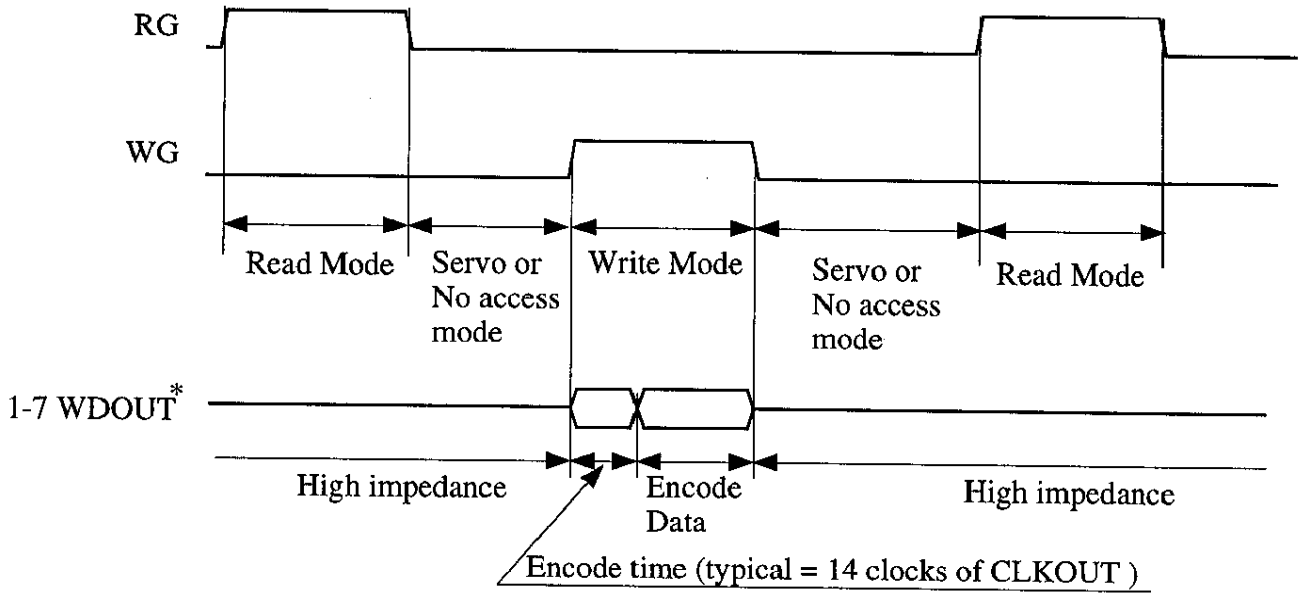
Fig. 6 (1,7) Code to NRZ Decoding Example

10. Sync Field Detection

The high-gain period can be set to last six bytes after the RG signal is goes active.



Read and write mode

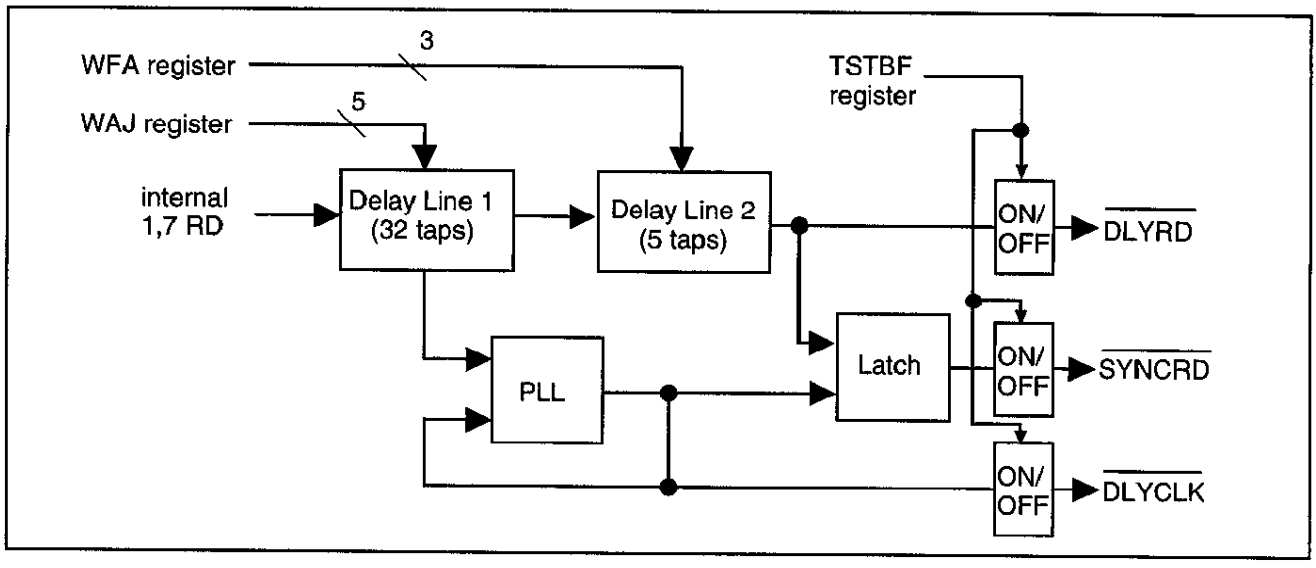


*) 1-7 WDOUT is synchronized rising edge of CLKOUT

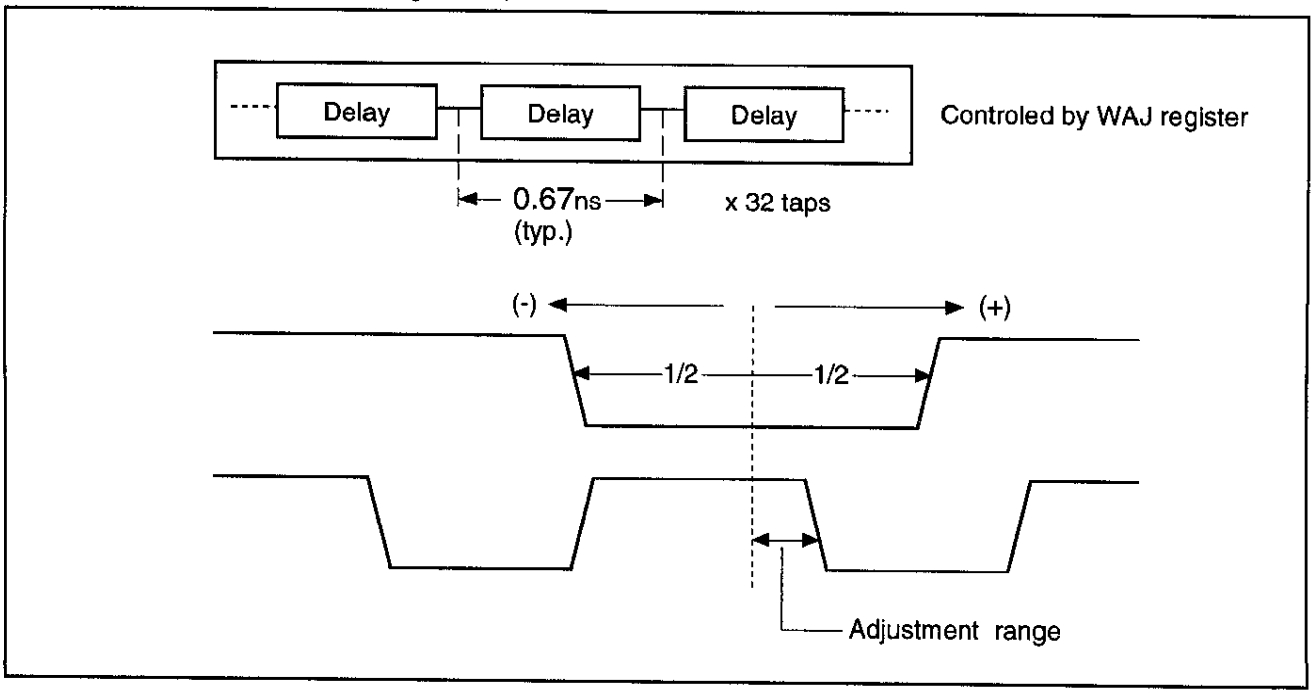
11. Window Adjustment Circuit

The HD153031RF has two on-chip delay lines for centering the decode window. First delay line has 32 taps for coarse adjustment that can be selected by register WAJ. Second delay line has 5 taps for fine adjustment that can be selected by register WFA. Centering adjustment can beperformed automatically by a microcontroller. This adjustment function can also be used for preshipment window margin test.

(1) Circuit Configuration



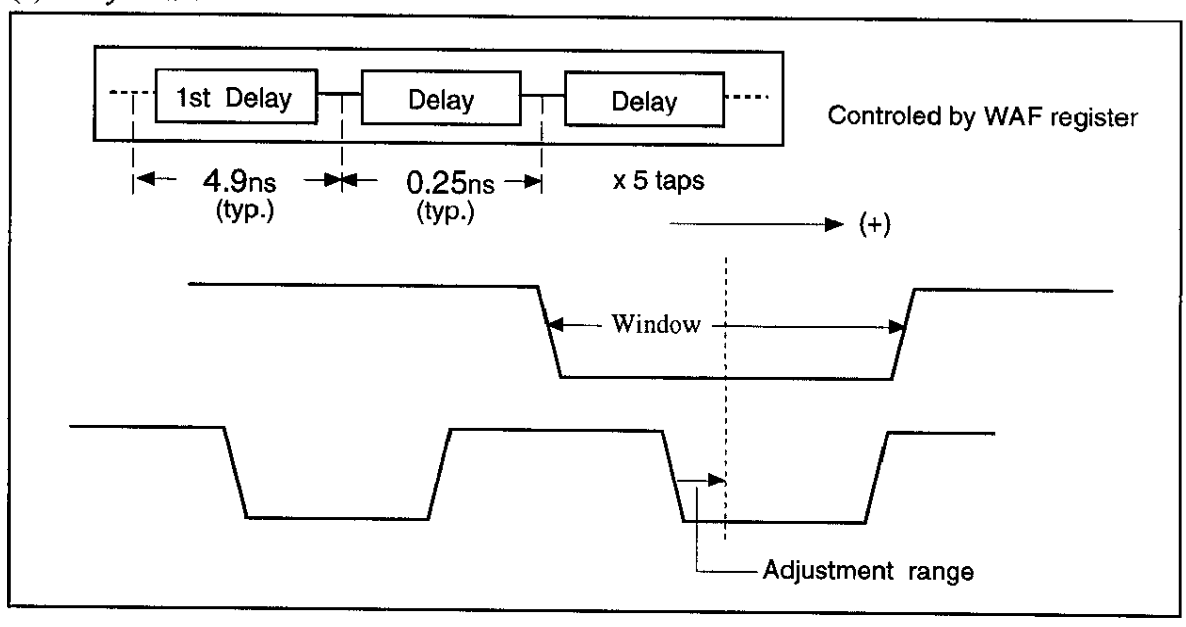
(2) Delay Line 1 (Coarse Window Adjustment)



WAJ Register

MSB				LSB	
4	3	2	1	0	Delay line 1 tap No.
0	0	0	0	0	− 16
	⋮				⋮
0	1	1	1	0	− 2
0	1	1	1	1	− 1
1	0	0	0	0	0
1	0	0	0	1	+ 1
1	0	0	1	0	+ 2
	⋮				⋮
1	1	1	1	1	+15

(3) Delay Line 2



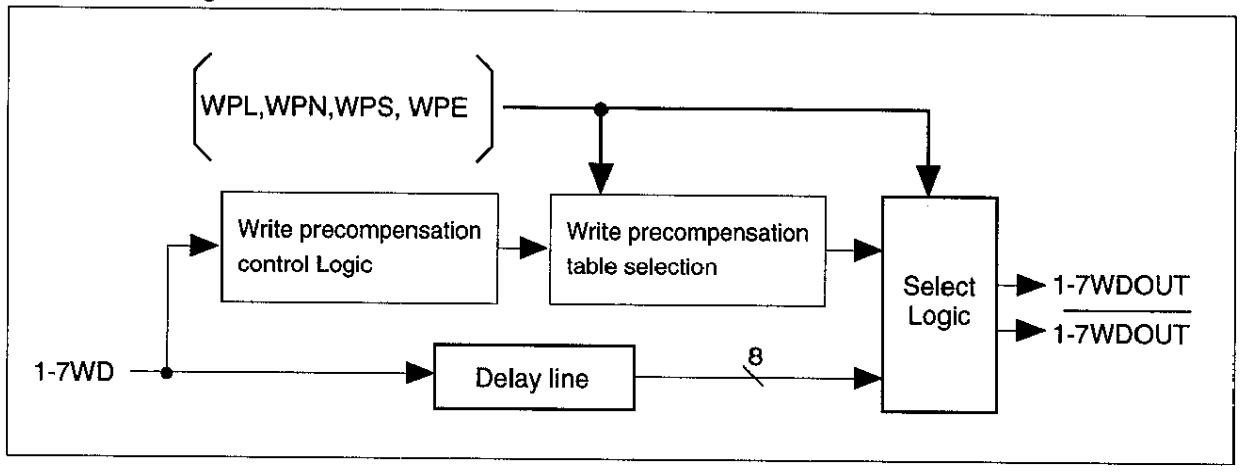
WAF Register

MSB		LSB	
2	1	0	Delay line 2 tap No.
0	0	0	0
0	0	1	+ 1
0	1	0	+ 2
0	1	1	+ 3
1	0	0	+ 4

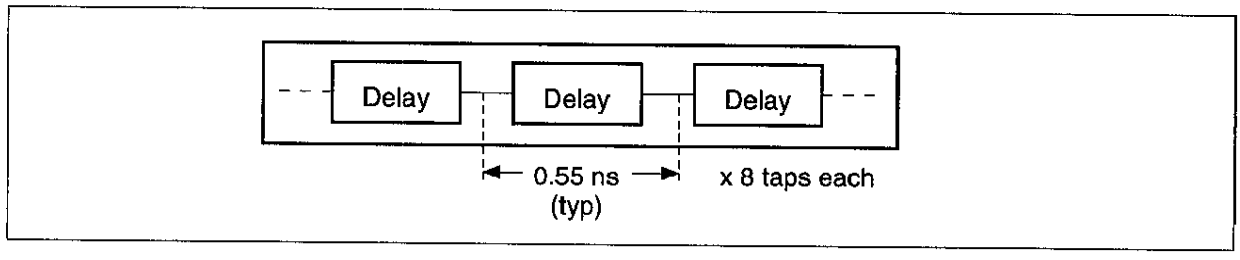
12. Write Precompensation Circuit

The HD153031RF has a built-in synchronous write precompensation circuit, and the 4 matrix delay levels from the write precompensation table shown below can be selected independently for the EARLY and LATE sides.

(1) Circuit Configuration

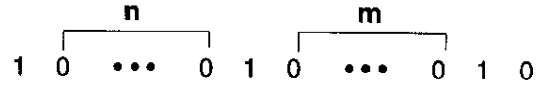


(2) Programmable Delay Line



(3) Table

n \ m	1	2	3	4	5	6	7
1	N	E	E	E	E	E	E
2	L	S	S	S	S	S	S
3	L	S	S	S	S	S	S
4	L	S	S	S	S	S	S
5	L	S	S	S	S	S	S
6	L	S	S	S	S	S	S
7	L	S	S	S	S	S	S



n: The number of zeros between the current 1 bit and the previous 1 bit

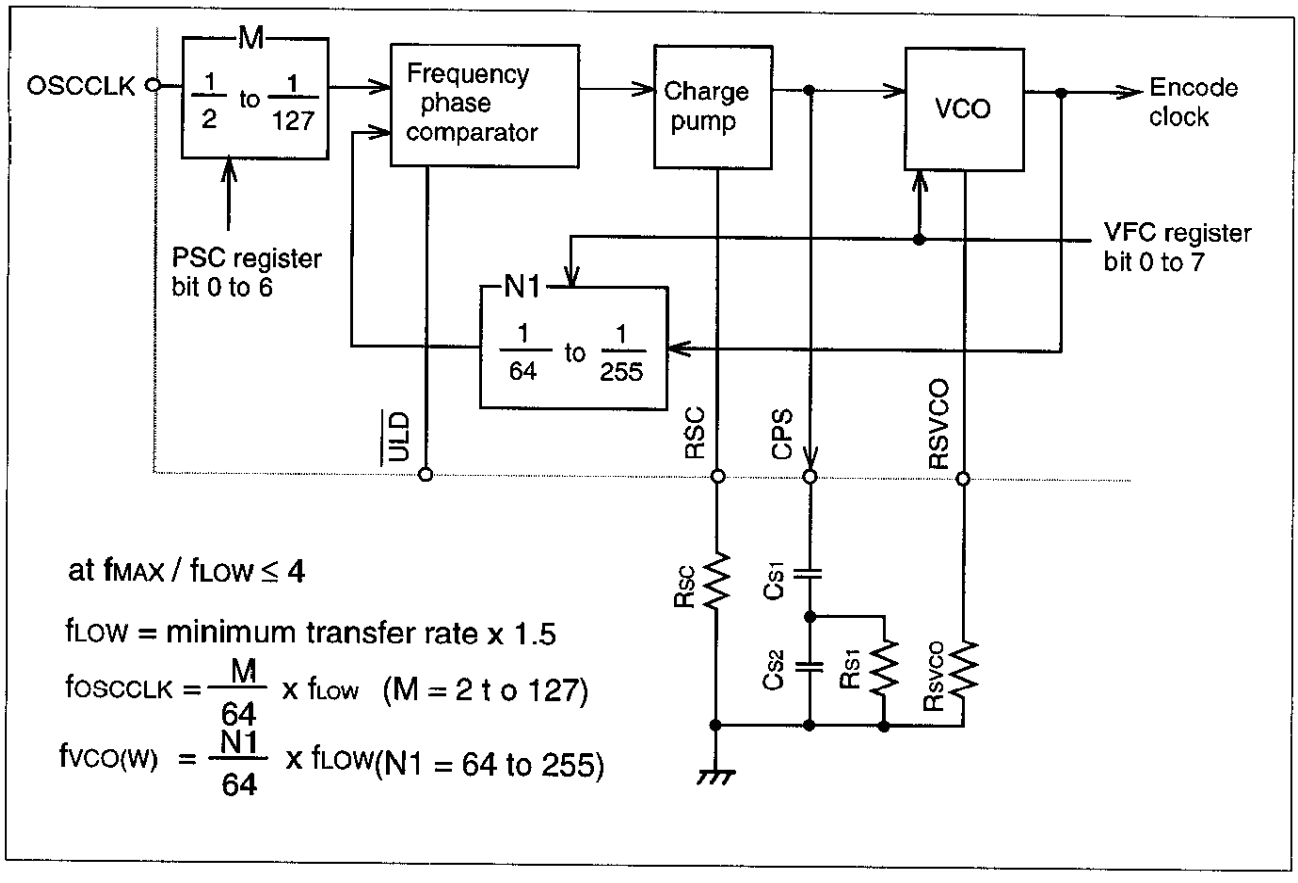
m: The number of zeros between the current 1 bit and the next 1 bit

The precompensation delay time for each the 4 matrix entries in the precompensation table (see Table) can be set independently.

The delay time (8 levels) is selected by the each part of register.

13. Encode Clock Generator's Frequency Synthesizer

Block diagram



Function

- A PLL-type frequency synthesizer generates the encode clock.
- The encode clock frequency can be set by bits 0 to 7 of register VFC to a value N/64 times the minimum data transfer rate (innermost track on the disk), where 64≤ N≤ 255.
- The lock/unlock function ($\overline{\text{ULD}}$ line) can prevent data from being written when a drive fault occurs.
- Direct, external input of the encode clock (at 1.5 times the treansfer rate) is also possible without using the on-chip frequency synthsizer.
- The VCO center frequency can be selected by bits 0 to 7 of register VFC, so a single external resistor RSVCO covers the entire setting range.

Operation

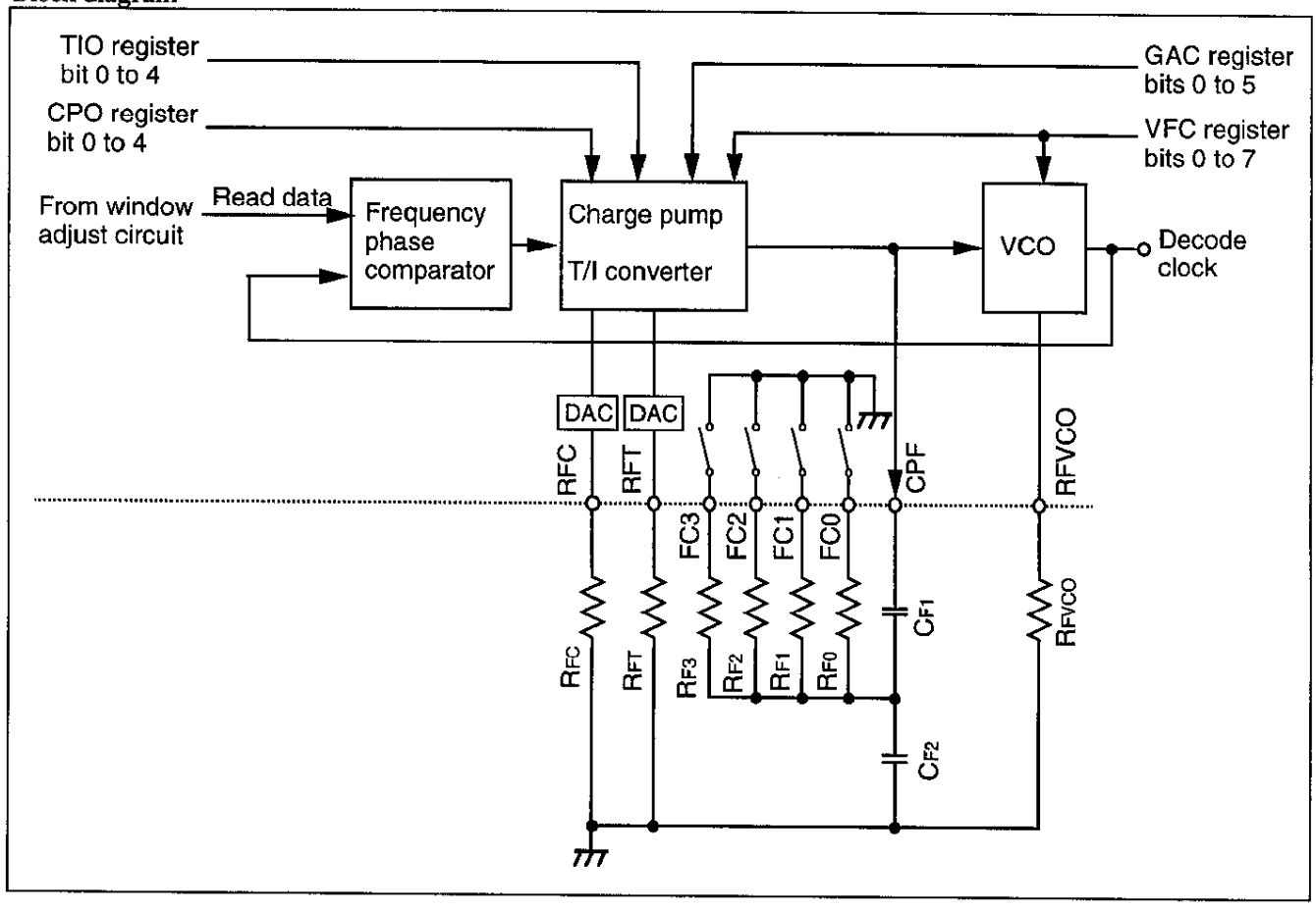
- Input a reference clock to OSCCLK at (1.5•M)/6 4 times the driver's minimum transfer rate.
  This signal input to the frequency-phase
- comparator at 1/M .
  The VCO clock is devided by 1/64 to 1/255,
- depending on bits 0 to 7 of register VFC, and input to the frequency-phase comparator.

$2 \le M \le 127$, $64 \le N1 \le 255$.

fVCO(W) : VCO output frequency
fLOW : Encoder clock frequency corresponding to minimum transfer rate.

14. Decode Clock Generator's VFO

Block diagram



Function

- The phase of the VCO clock is synchronized with the read data from the window adjust circuit.
- The frequency-phase comparator operates in the frquency-phase comparison mode whilc acquiring phase lock in the sync field, and in phase comparison mode during synchronization in the date field.
- The charge pump and T/I converter circuits both operate while phase lock is being acquired. During synchronization, only the T/I converter operates.
- The VFO is synchronized with the encode clock until the read gate signal (RG) is asserted.
- The VCO center frequency can be changed by rewriting bits 0 to 7 of the VFC register, so multiple zone recording can be implemented with only a single external resistor(R_{FVCO}).
- The charge pump can select eight levels currents, the reference value of which is controlled by external resistor R_{FC}. Bit 3 to 5 in register GAC selects these eight currents.
- The T/I converter provides one of eight output currents as selected by bits 0 to 2 of register GAC.
- The loop filter attenuation ζ can be selected by bit 6 of register GAC (two selections). Independent settings can be made for high gain and normal gain.

15. Calculation of PLL Constants

I. Encode Clock Generator's Frequency Synthesizer (W-PLL)

1. VCO center frequency f_{OW}

$$f_{OW} = \frac{(6.975 \times 10^9) \cdot N}{R_{SVCO}} \text{ (Hz)} \quad \text{Note1} \qquad \text{(I.1)}$$

2. VCO gain K_{OW}

$$K_{OW} = (1.056 \times 10^9) \cdot \sqrt{\frac{N}{R_{SVCO}}} \left(\frac{rad}{sec \cdot V}\right) \qquad \text{(I.2)}$$

3. Charge pump current ratio Nc

$$N_C = \text{int}\left[16 \cdot \sqrt{\frac{N1}{N1_{MAX}}} - 8\right] \quad \text{Note2} \qquad \text{(When } N1=N1_{MAX}\text{, set the Nc=7)} \qquad \text{(I.3)}$$

Note2: int[ ] is the integer value calculated by discarding the fractional part of the value.

4. Charge pump current I_{CW}

$$I_{CW} = \frac{5.3}{R_{SC}} \cdot \left(1 + \frac{Nc}{8}\right) \text{ (A)} \qquad \text{(I.4)}$$

5. Characteristic frequency ω_{nW}

$$\omega_{nW} = \sqrt{\frac{K_{OW} \cdot I_{CW}}{2\pi \cdot N1 \cdot C_{S1}}} \left(\frac{rad}{sec}\right) \qquad \text{(I.5)}$$

6. Attenuation ζ_W

$$\zeta_W = \frac{(C_{S1} + C_{S2})}{2} \cdot R_{S1} \cdot \omega_{nW} \qquad \text{(I.6)}$$

II. Decode Clock Generator's VFO

1. VCO center frequency f_{OR}

$$f_{OR} = \frac{(3.375 \times 10^9) \cdot N}{R_{FVCO}} \text{ (Hz)} \qquad \text{(II.1)}$$

2. VCO gain K_{OR}

$$K_{OR} = (1.536 \times 10^9) \cdot \sqrt{\frac{N}{R_{FVCO}}} \left(\frac{rad}{sec \cdot V}\right) \qquad \text{(II.2)}$$

3. Charge pump current I_{CR}

$$I_{CR} = \frac{2.5 \times 10^4}{R_{FC}} \cdot \frac{P}{8} \quad (mA) \qquad (II.3)$$

where $1 \leq P \leq 8$

4. T/I converter current I_{TR}

$$I_{TR} = (3.52 \times 10^3) \cdot \frac{N \cdot L}{500 + R_{FT}} \quad (\mu A) \qquad (II.4)$$

where $0 \leq L \leq 7$

5. Characteristic frequency (high gain) ω_{nRH}

$$\omega_{nRH} = \sqrt{\frac{K_{OR} \cdot \left(\frac{I_{CR}}{6} + I_{TR}\right)}{\pi \cdot C_{F1}}} \quad \left(\frac{rad}{sec}\right) \qquad (II.5)$$

6. Characteristic frequency (normal gain) ω_{nRN}

$$\omega_{nRN} = \sqrt{\frac{K_{OR} \cdot I_{TR}}{\pi \cdot C_{F1}}} \quad \left(\frac{rad}{sec}\right) \qquad (II.6)$$

7. Attenuation (high gain) ζ_{RH}

$$\zeta_{RH} = \frac{(C_{F1} + C_{F2})}{2} \cdot \frac{1}{\frac{1}{R_{FA}} + \frac{1}{R_{FB}}} \cdot \omega_{nRH} \qquad (II.7)$$

where R_{FA} and R_{FB} = R_{F0} and R_{F1} when GAC register bit 6 = 0
R_{F2} and R_{F3} when GAC register bit 6 = 1

8. Attenuation (normal gain) ζ_{RN}

$$\zeta_{RN} = \frac{(C_{F1} + C_{F2})}{2} \cdot R_{FA} \cdot \omega_{nRN} \qquad (II.8)$$

where R_{FA} = R_{F0} when GAC register bit 6 = 0
R_{F2} when GAC register bit 6 = 1

Table 15. 1 VCO Oscillation Frequency and Transfer Speed for Settings of Register VFC

(at fMAX / fLOW = 3.98)

N1	VFC register MSB 7 6 5 4 3 2 1 0 LSB	N	VCO oscillation frequency and transfer speed ratio	Example: RFVCO= 3.0 kΩ, RSVCO = 6.2 kΩ VCO center frequency (MHz)	Transfer speed (Mbps)
0					
•	Inhibit				
•					
63					
64	0 1 0 0 0 0 0 0	16	1.000	18.00	12.00
65	0 1 0 0 0 0 0 1	16	1.016	18.28	12.19
66	0 1 0 0 0 0 1 0	16	1.031	18.56	12.38
67	0 1 0 0 0 0 1 1	16	1.047	18.84	12.56
68	0 1 0 0 0 1 0 0	17	1.063	19.13	12.75
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
127	0 1 1 1 1 1 1 1	31	1.984	35.72	23.81
128	1 0 0 0 0 0 0 0	32	2.000	36.00	24.00
129	1 0 0 0 0 0 0 1	32	2.016	36.28	24.19
130	1 0 0 0 0 0 1 0	32	2.031	36.56	24.38
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
253	1 1 1 1 1 1 0 1	63	3.95	71.16	47.44
254	1 1 1 1 1 1 1 0	63	3.97	71.44	47.63
255	1 1 1 1 1 1 1 1	63	3.98	71.72	47.44

Table 15. 2 Charge pump Output Current Settings in Register GAC

Bits	GAC register 5	4	3	P	Charge pump output current ratio	Example:R_{FC} = 5.1kΩ Charge pump output current (mA)
1	0	0	0	1	1	0.613
2	0	0	1	2	2	1.226
3	0	1	0	3	3	1.838
4	0	1	1	4	4	2.451
5	1	0	0	5	5	3.064
6	1	0	1	6	6	3.677
7	1	1	0	7	7	4.289
8	1	1	1	8	8	4.902

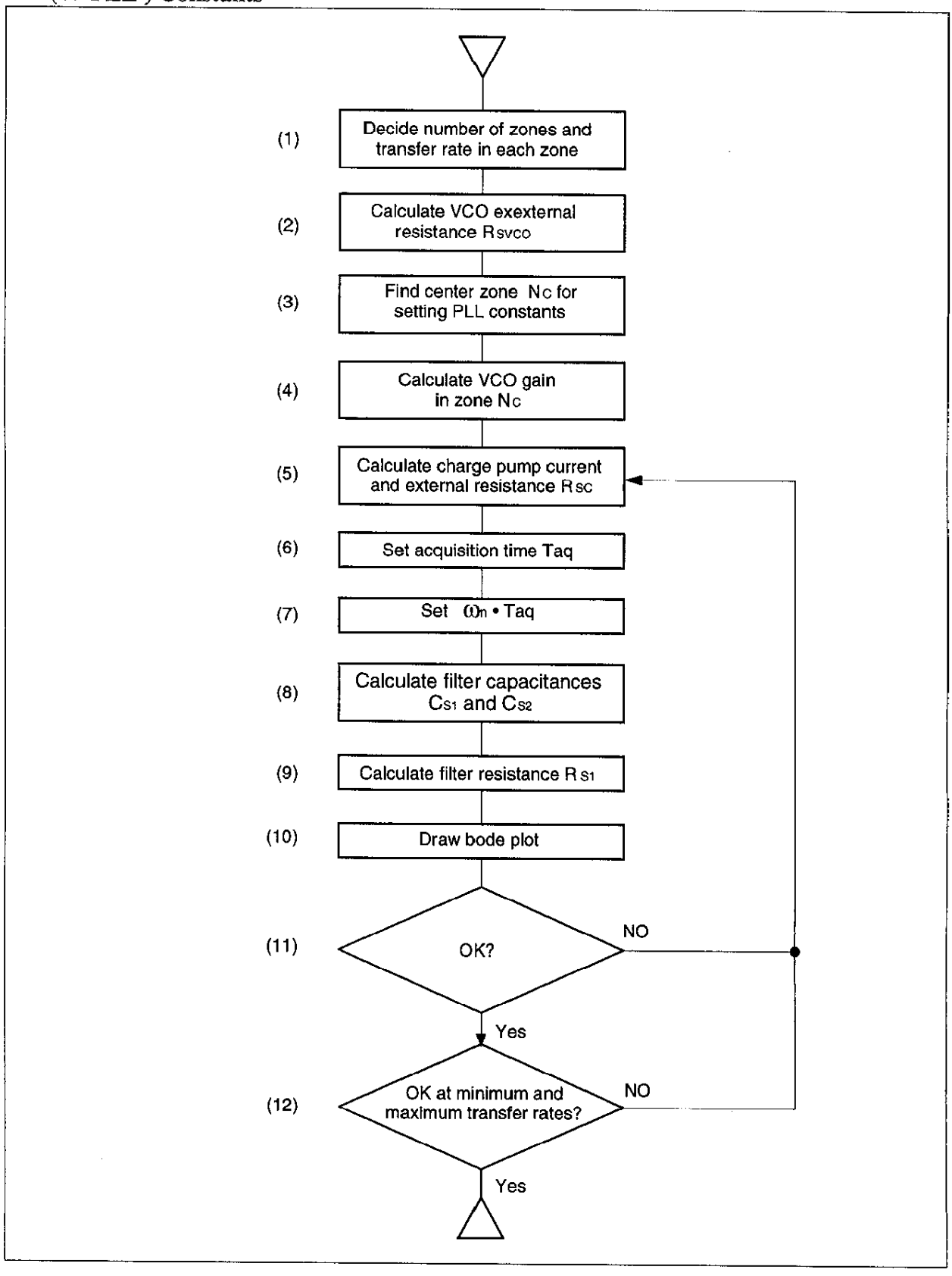
$$I_{CR} = \frac{2.5 \times 10^{4}}{R_{FC}} \bullet \frac{P}{8} \quad (A)$$

Table 15. 3 T/I Output Current Settings in Register GAC

Bits	GAC register 2	1	0	L	T/I output current ratio	Example:R_{FT} =12kΩ N=63 T/I output current (μA)
1	0	0	0	0	0	0.0
2	0	0	1	1	1	17.7
3	0	1	0	2	2	35.5
4	0	1	1	3	3	53.2
5	1	0	0	4	4	71.0
6	1	0	1	5	5	88.7
7	1	1	0	6	6	106.5
8	1	1	1	7	7	124.2

$$I_{TR} = (3.52 \times 10^{3}) \bullet \frac{N \bullet L}{500 + R_{FT}} \quad (\mu A)$$

16. Flowchart of Procedure for Setting Encode Clock Generator's Frequency Synthesizer (W-PLL) Constants



17. Flowchart Explanation (W-PLL)

(1) Decide number of zones and transfer rate in zone

The HD153031RF uses a frequency synthesizer to generate the reference clock, so the value of the transfer rate is quantized. If the lowest rate corresponds to N=16, the available rates are given by the formula:

$$TR_N = TRmin, \quad 16 \leq N \leq 63$$

where, TR_N : Transfer rates in different zones
TRmin : Minimum transfer rate (innermost track)

(2) Calculate VCO external resistance R svco

Use equation (I.1) to calculate the external resistance R svco that makes the VCO oscillate at 1.5 times the minimum transfer rate (N=16)

(3) Find center zone (TRcen)

Calculate the midpoint (TRcen) between the minimum transfer rate (TRmin) and maximum transfer rate (TRmax), and from the zones selected in step (1), find the value of N (N_c) that comes closest to TRcen.

$$TRcen = \frac{TRmin+TRmax}{2}$$

(4) VCO gain Kow

Use equation (I.2) to calculate the VCO gain ζ in the center zone ($N=N_c$)

(5) Charge pump current I cw

Select the charge pump current within the following range:

$$Icw \leq 500 \ (\mu A)$$

Calculate the necessary external resistance R sc from equation (I.4).

(6) Setting phase-lock acquisition time Taq

Decide the phase-lock acquisition time Taq, considering the change in characteristic frequency from zone to zone and the head seek time.

(7) Setting $\omega_n \cdot T_{aq}$

Decide $\omega_n \cdot T_{aq}$ the end of the phase-lock acquisition.

(8) Filter capacitances C_{S1} and C_{S2}

Decide the phase-lock acquisition time Taq, considering the charge in characteristic frequency from zone to zone and the head seek time.The value used in this data sheet is:

$$Taq = 0.1 \quad (ms)$$

The following formula gives an estimate of the acquisition time:

$$\omega_{nW} \cdot Taq = 2.25$$

Substitute the values of K_{CW} and Iow into equation (I.5) and combine with the formula above to calculate the filter capacitance C_{S1}. To suppress jitter and allow a phase margin, the following value is recommended for C_{S2} :

$$C_{S2} = \frac{1}{45} \cdot C_{S1}$$

(9) Filter resistance R_{S1}

To ensure loop stablIity, set the attenuation to approximately:

$$\zeta_{nw} = 1.0$$

Substitute this value into equation (I.6) to calculate the filter resistance R_{S1}.

(10) Bode plot

Calculate the open-loop transfer function G(s) and draw a Bode plot.

(11) OK?

Decide whether the open -loop and closed -loop characteristics are satisfactory.

(12) OK at TRmin and TRmax?

Repeat steps (8) and (9) for the minimum and maximum transfer rates.

18. Caluculation example of HD153031RF W-PLL Constants

Transfer rate ; 18Mbps , 36Mbps 2 zone

(1) Oscillation frequency f_{ow} = 36MHz , N=32

$$Rsvco = \frac{(6.975 \times 10^{9}) \cdot 32}{fow} = 6.2\ k\Omega$$

(2) VCO gain Kow

$$Kow_{18} = 1.056 \times 10^{9} \sqrt{\frac{24}{6.2 \times 10^{3}}} = 65.7\ Mrad/s \cdot V$$

$$Kow_{36} = 1.056 \times 10^{9} \sqrt{\frac{48}{6.2 \times 10^{3}}} = 92.9\ Mrad/s \cdot V$$

(3) Charge Pump Current Icw

Rsc = 20KΩ

$$Icw_{18} = \frac{5.3}{20 \times 10^{3}} \left(1 + \frac{1}{8}\right) = 298.1\ \mu A \quad (NC=1)$$

$$Icw_{36} = \frac{5.3}{20 \times 10^{3}} \left(1 + \frac{5}{8}\right) = 430.6 \mu A \quad (NC=5)$$

(4) ω_n

$\omega_n \cdot T_{aq} = 2.25$

(ω_n = 22.5 Krad / s) (taq = 0.1 ms)

$$\omega_{nw\,18} = \sqrt{\frac{65.7 \times 10^{6} \times 298.1 \times 10^{-6}}{2\pi \cdot 96 \cdot C_{S1}}}$$

$$\omega_{nw\,36} = \sqrt{\frac{92.9 \times 10^{6} \times 430.6 \times 10^{-6}}{2\pi \cdot 192 \cdot C_{S1}}}$$

$C_{S1\,18}$ = 64137pF

$C_{S1\,36}$ = 65500pF

∴ C_{S1} = (64137 + 65500) / 2 =64819

≈ 68000pF

$$C_{S2} = \frac{1}{45} \cdot C_{S1} = 1440.4$$

∴ $C_{S2} \approx$ 1500pF

(5) Attenaton ζ_{nw}

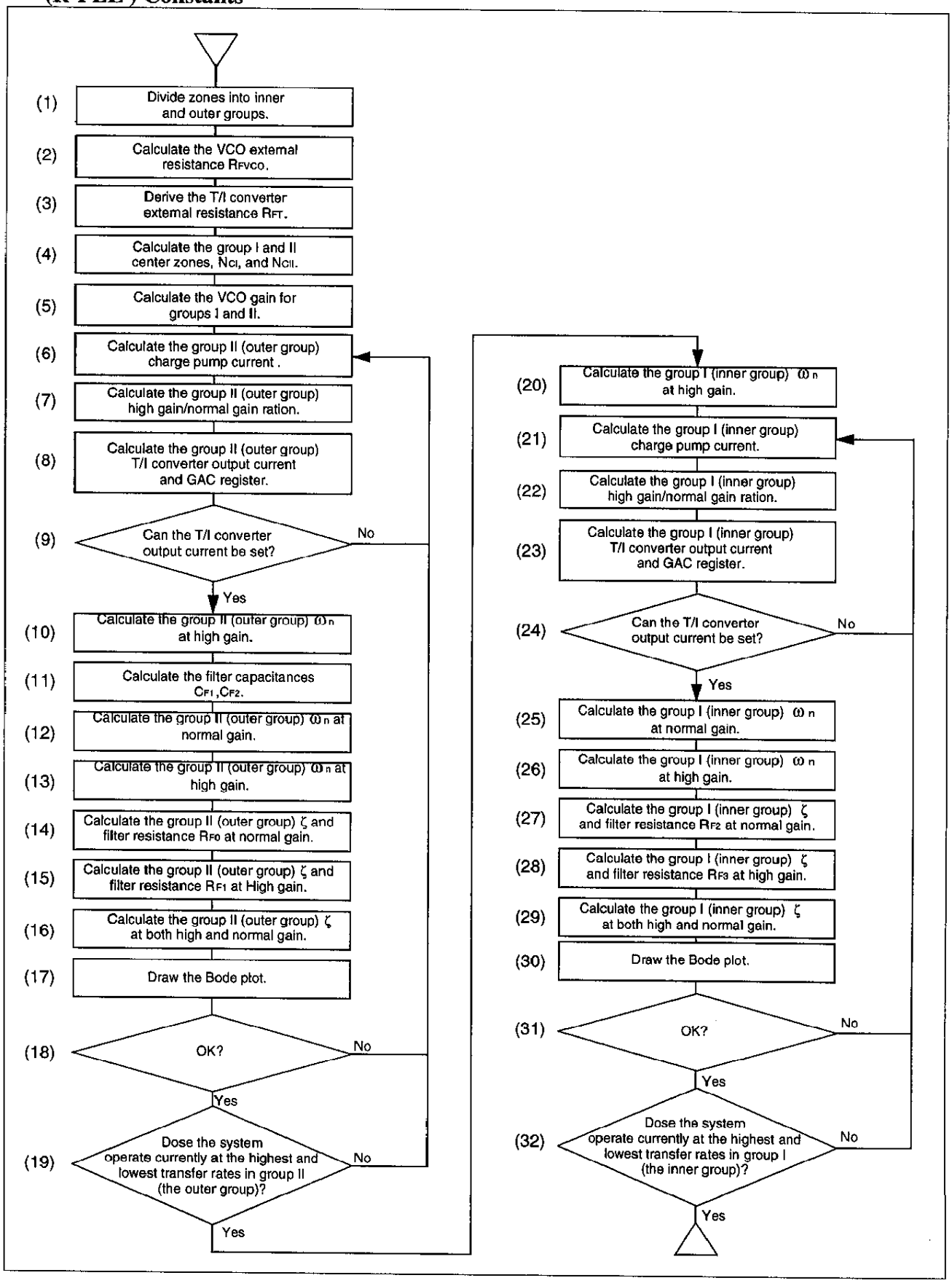
$$\zeta_{nw} = \frac{(68000+1500) \times 10^{-12}}{2} \cdot R_{S1} \cdot \omega_{nw}$$

$\omega_{nw\,18}$ = 21.86 Krad / s, $\zeta_{nw\,18}$ = 0.9875

$\omega_{nw\,36}$ = 22.09 Krad / s, $\zeta_{nw\,36}$ = 0.9979

∴ $R_{S1} \approx$ 1.3 kΩ

19. Flowchart of Procedure for Setting Decode Clock Generator VFO (R-PLL) Constants



20. Flowchart Explanation (R-PLL)

(1) Divide zones into groups

Divide the zones selected in synthesizer step (1) into two groups (I and II) having equal frequency ranges.

Divide the groups at the following transfer rate TRgr:

$$TRgr = \sqrt{TRmin \cdot TRmax}$$

(2) VCO external resistance R_{FVCO}

Use equation (II.1) to calulate the external resistance R_{FVCO} that makes the VCO oscillate at 1.5 times the minimum transfer rate (N=16)

(3) T/I converter external resistance R_{FT}

Find the R_{FT} values at the minimum transfer rate as shown in Fig1.(R_{FT} vs Data transfer rate).

(4) Center zones TR_{CI} and TR_{CII} of group I and II

Find N_{CI} and N_{CII} in groups I and II by the same method as in synthesizer step (3). See page 42.

(5) VCO gain K_{OR} in groups I and II

Use equation (II.2) to calculate the VCO gain K_{OR} at the center zones ($N=N_{CI}$ and $N=N_{CII}$) in groups I and II.

(6) Charge pump current I_{CR} in group II

Select the charge pump current level within the following range:

$I_{CR} \leq 5.0$ (mA)

Calculate the values for the external resistances R_{FC} and P from equation (II.3). So that the current has the desired value. See Table2 for the relationship between the value of P and GAC register.

(7) High gain/normal gain ratio in group II.

Set the current ratio g_G between high and normal gain.

$$g_G = 16$$

(8) Group II T/I conversion output current I

Determine the value of L($0 \leq L \leq 7$) using equation (II.4), so that the following equation is satisfied.

$$I_{TR} = \frac{I_{CR}}{6(g_G - 1)}$$

See Table3 for the relationship between the value of L and GAC register.

(9) Analysis

Determine if the T/I converter output current can be set.

(10) Group II High Gain ω_n

After determining the group II center zone N CII phase pull-in time Taq taking into consideration the high gain set time, and determine the high gain characteristic frequency ω_{nRH} using the following equation.

$$\omega_{nRH} \cdot T_{aq} = 2.7$$

(Adjust so that this value is in the range 2 to 4.)

(11) Filter Capacitances C_{F1} and C_{F2}

Calculate the filter capacitance C_{F1} by substituting the high gain characteristic frequency ω_{nRH} calculated in item (10) above in formula II.5.

Also, set the ratio between C_{F1} and C_{F2} taking into consideration high region jitter suppression and phase margin. We recommend deriving C_{F2} using the following equation.

$$C_{F2} = \frac{1}{45} \cdot C_{F1}$$

(Adjust so that this value is in the range 1/20 to 1/100.)

(12) Group II Normal Gain ω_n

Compute the normal gain characteristic frequency ω_{nRN} by substituting the derived value of C_{F1} into formula II.6.

(13) Group II High Gain ω_n

Compute the high gain characteristic frequency ω_{nRH} by substituting the derived value of C_{F1} into formula II.5.

(14) Group II Normal Gain ζ and Filter Resistance R_{F0}

Set the normal gain attenuation ratio ζ_{RN} with stability as the main criteria.
The equation below indicate the recommend value . $\zeta_{RN} \cong 1.0$
Calculate the filter resistance R_{F0} by substituting that value into formula II.8

(15) Group II High Gain ζ and Filter Resistance R_{F1}

Set the normal gain attenuation ratio ζ_{RH} with stability as the main criteria.
The equation below indicate the recommend value . $\zeta_{RN} \cong 0.8$
Calculate the filter resistance R_{F1} by substituting that value into formula II.7.

(16) Group II High Gain ζ and Normal Gain ζ

Calculate the attenuation ratios ζ_{RH} and ζ_{RN} by substituting the values of R_{F0} and R_{F1} into equations II.7 and II.8.

(17) Bode Plot Construction

Compute the open loop transfer function G(s) and construct the Bode plot.

(18) Analysis

Determine if the system is suitable from the open and closed loop characteristics.

(19) Analysis at TRmin and TRmax

Repeat the analysis of item (17) and (18) for group II TRmin and TRmax.

(20) Group I High Gain ω_n

After determining the group I center zone N ci pfase pull-in time Taq taking into consideration the high gain set time, and determine the high gain chracteristic frequency ω_{nRH} using the following equation

$$\omega_{nRH} \cdot Taq = 3.07$$

(Adjust so that this value is in the range 2 to 4.)

(21) Group I Charge Pump Current I_{CR}

Calculate the charge pump current I_{CR} by substituting the high gain characteristic frequency ω_{nRH} computed in item (20) above into formla II.5.

Here, set the charge pump current level within the following range:

$$I_{CR} \leq 5.0mA$$

Now , derive a value for P using equation II.3 so that the desired charge pump current is achieved.

See Table2 for the relationship between the value P and GAC register.

(22) Group I High gain / Normal Gain Ratio

Set the high gain to normal gain current ratio g_G.

$$g_G = 16$$

(23) Group I T/I Converter Output Current I_{TR}

Determine a value of L ($0 \leq L \leq 7$) using equation (II.4) so that the following equation

$$I_{TR} = \frac{I_{CR}}{6(g_G-1)}$$

See Table3 for the relationship between the value L and GAC register.

(24) Analysis

Determine if the T/I converter output current should be set .

(25) Group I Normal Gain ω_n

Calculate the normal gain characteristic frequeny ω_{nRN} by substituting the I_{TR} derived above into formuia II.6.

(26) Group I High Gain ω_n

Calculate the high gain characteristic frequeny ω_{nRH} by substituting the I_{CR} derived above into formuia II.5.

(27) Group I Normal Gain ζ and Filter Resistance R_{F2}

Set the normal gain attenuation ration ζ_{RN} with stability as the main criteria.
The equation below indicate the recommend value.
$\zeta_{RN} \cong 1.0$
Calculate the filter resistance R_{F2} by substituting that value into formula II.8.

(28) Group I High Gain ζ and Filter Resistance R_{F3}

Set the high gain attenuation ration ζ_{RH} with stability as the main criteria.
The equation below indicate the recommend value.
$\zeta_{RH} \cong 0.8$
Calculate the filter resistance R_{F3} by substituting that value into formula II.7.

(29) Group I High Gain ζ and Normal Gain ζ

Calculate the attenuation ratios ζ_{RH} and ζ_{RN} by substituting the values of R_{F2} and R_{F3} into equations II.7 and II.8.

(30) Bode Plot Construction

Compute the open loop transfer function G(S) and construct the Bode plot.

(31) Analysis

Determine if the system is suitable from the open and closed loop characteristics.

(32) Analysis to determine TRmin and TRmax

Repeat the analysis of items (30) and (31) for group I TRmin and TRmax.

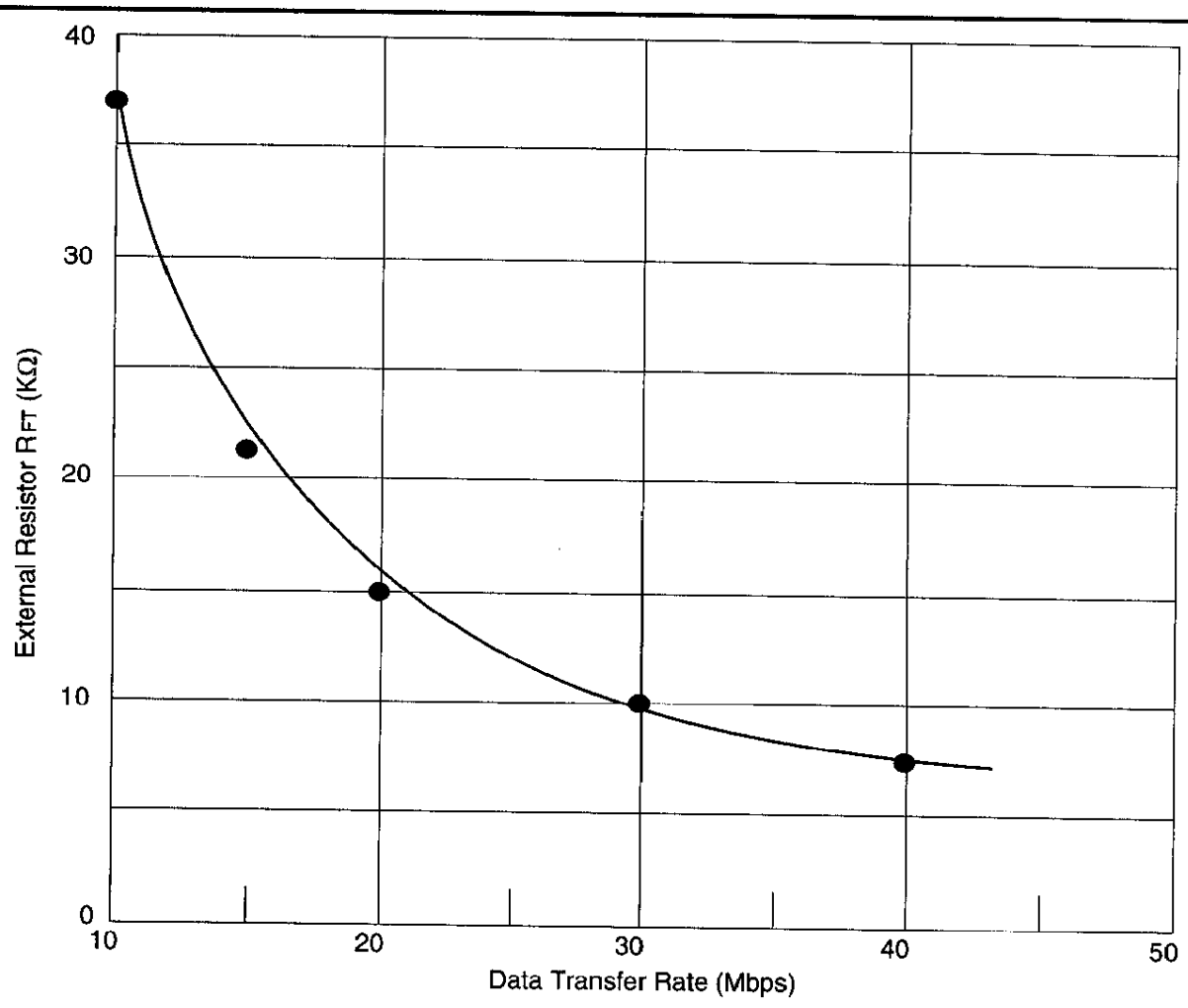


Fig 19. 1 T/I Converter Circuit External Resistor RFT vs Data Transfer Rate

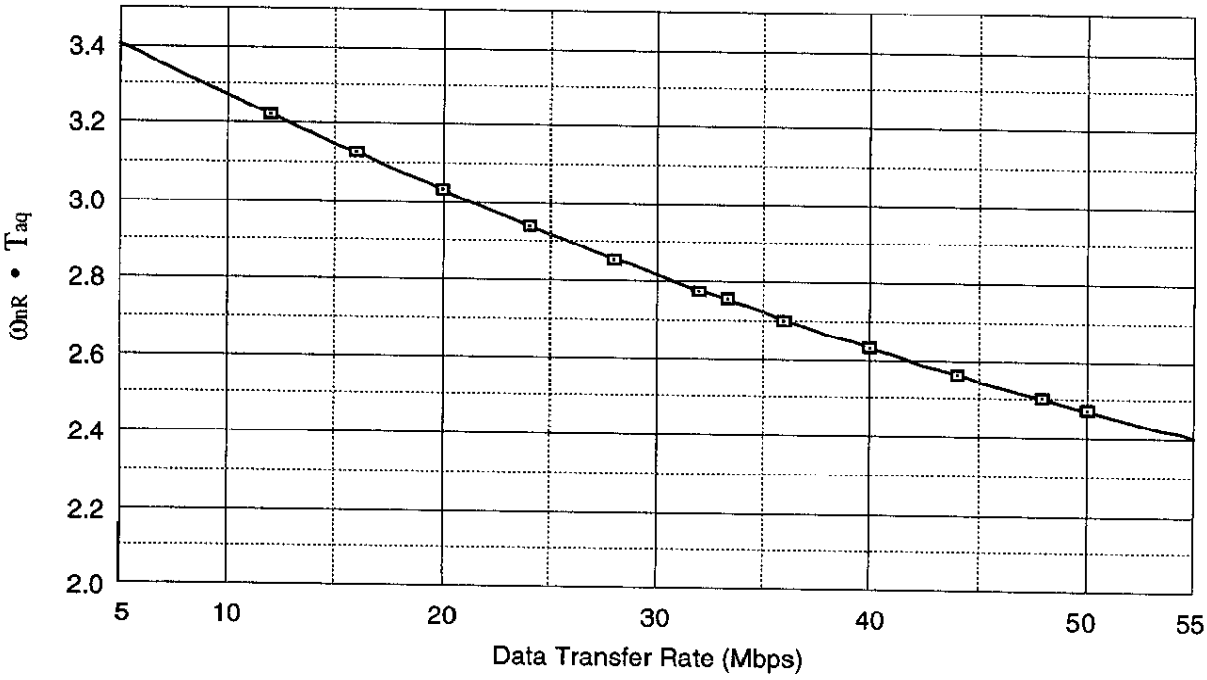


Fig 19. 2 ω_{nR} • T_{aq} vs Data Transfer Rate (R-PLL)

20. Caluculation example of HD153031RF R-PLL Constants

Transfer rate ; 18Mbps , 36Mbps 2 zone

(1) $R_{FVCO} = 3.0K\Omega$ Oscillation frequency = 36MHz

(2) $R_{FT} = 16K\Omega$

(3) VCO Gain K_{OR}

$$K_{OR\,18} = 1.536 \times 10^{9}\sqrt{\frac{24}{3.0 \times 10^{3}}} = 137.4\ \text{Mrad/s} \bullet \text{V}$$

$$K_{OR\,36} = 1.536 \times 10^{9}\sqrt{\frac{48}{3.0 \times 10^{3}}} = 194.3\ \text{Mrad/s} \bullet \text{V}$$

(4) Charge Pump Current I_{CR}

$R_{FC} = 5.1\ K\Omega$

$$I_{CR\,36} = \frac{2.5 \times 10^{4}}{5.1 \times 10^{3}} \bullet \frac{P}{8}$$

$I_{CR\,36} = 4.9\ mA\ (P=8)$

(5) T/I Current I_{TR}

$$I_{TR\,36} = \frac{4.9}{6 \bullet (16 - 1)} = 54.4\ \mu A$$

$R_{FT} = 16\ K\Omega$

$$I_{TR\,36} = 3.52 \times 10^{3} \bullet \frac{N \bullet L}{500 + R_{FT}}$$

$\therefore I_{TR\,36} = 51.2\mu A\ (N=48, L=5)$

(6) $\omega_n \bullet T_{aq\,36} = 2.7$

$T_{aq\,36} = 0.89\mu\ s$ (6 bytes x 2/3)

$\omega_{nRH} = 3.03\ \text{Mrad/s}$

$C_{F1}=5600P$, $C_{F2}=130P$

$\omega_{nRH\,36} = 3.10\ \text{Mrad/s}$ $\omega_{nRN\,36} = 0.75\text{Mrad/s}$

(7) $\zeta_N = 1.0$, $\zeta_H = 0.8$

$R_{F2} = 470\ \Omega$, $R_{F3} = 110\Omega$

$\zeta_N = 1.01$, $\zeta_H = 0.79$

(8) $\omega_n \bullet T_{aq\,18} = 3.07$

$T_{aq\,18} = 1.78\ \mu s$ (6 bytes x 2/3)

$\omega_{nRH\,18} = 1.72\ \text{Mrad/s}$

(9) Charge Pump Current I_{CR}

$$I_{CR\,18} = \frac{6\pi C_{F1} \bullet \omega_{nRH\,18}^{2}}{K_{OR\,18}} - 6I_{TR} = 1.96\ mA$$

$\therefore I_{CR\,18} = 1.84\ mA\ (P=3)$

(10) T/I Current I_{TR}

$I_{T\,18}$ = 20.48 μA (N=24, L=4)

$\omega_{nRH\,18}$ = 1.60 Mrad / s

$\omega_{nRN\,18}$ = 0.40 Mrad / s

(11) ζ_N = 1.0 , ζ_H = 0.8

R_{F0} = 910 Ω R_{F1} = 220 Ω

ζ_N = 1.04 ζ_H = 0.81

21. Example of HD153031RF PLL's external parts (18/36Mbps)

(A) W-PLL

R_{SVCO} = 6.2KΩ

R_{SC} = 20KΩ

C_{S1} = 68000pF

C_{S2} = 1500pF

R_{S1} = 1.3 kΩ

Register Value

18Mbps	36Mbps
VFC = 0110 0000	1100 0000
SGC = 0100 0001	0100 0101

(B) R-PLL

R_{FVCO} = 3.0 kΩ

R_{FC} = 5.1 kΩ

R_{FT} = 16 kΩ

C_{F1} = 5600pF

C_{F2} = 130pF

R_{F3} = 110 Ω

R_{F2} = 470 Ω

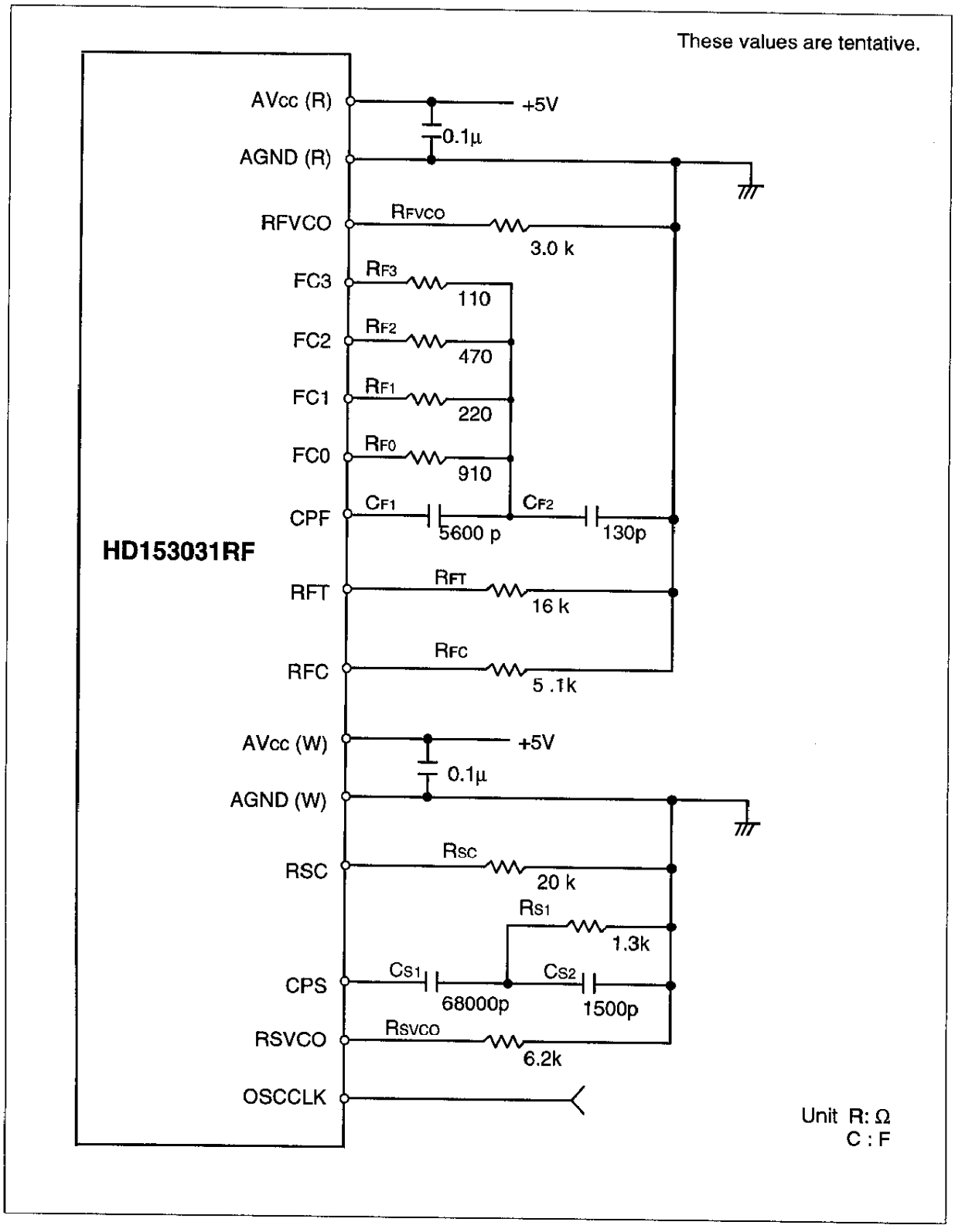
R_{F1} = 220 Ω

R_{F0} = 910 Ω

Register Value

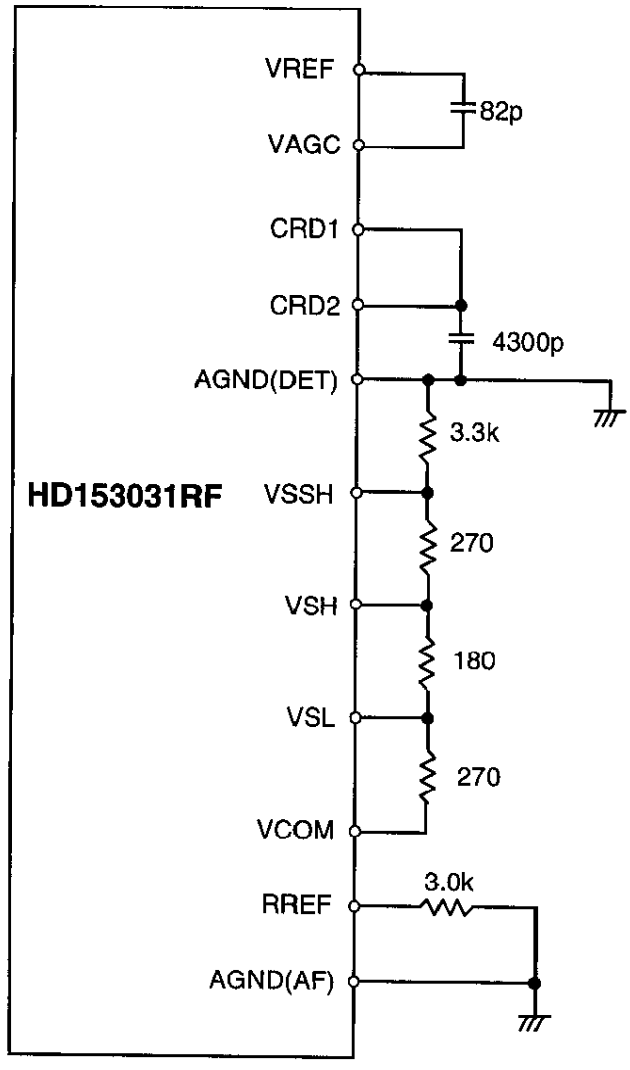
18Mbps	36Mbps
VFC =0110 0000	1100 0000
GAC= 0001 0100	0111 1101

22. Example of External Components Connected to the Read PLL and Write PLL



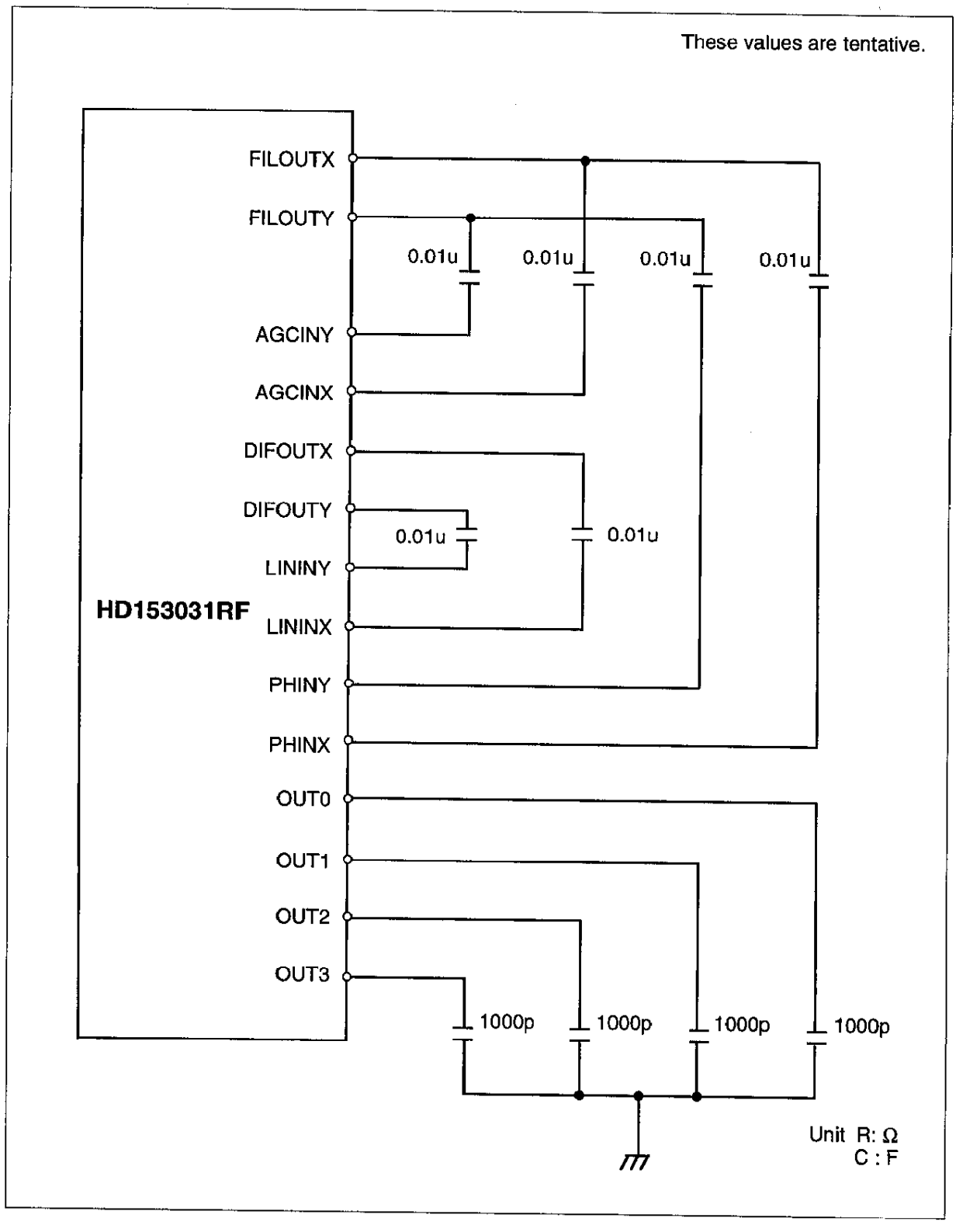
23. Example of External Components Connected to the RPD

These values are tentative.



Unit R: Ω
C : F

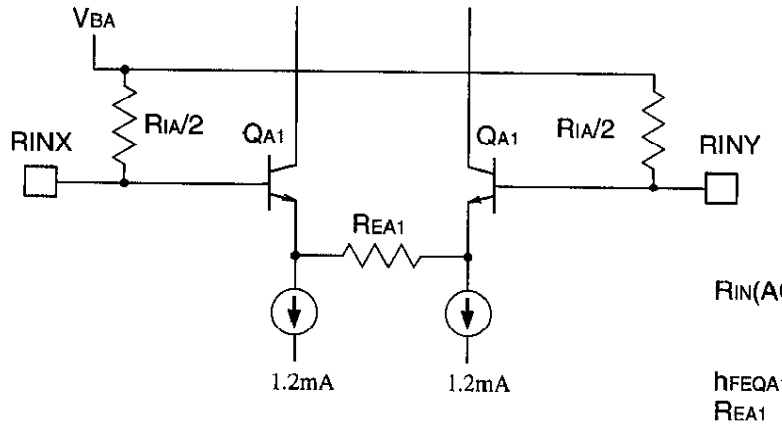
24. Example of External Components Connected to the RPD



25. Input/Output impedance of the Read Pulse Detector's amplifiers

■ AGC amplifier

Input impedance



$R_{IA}/2$	1.5kΩ
R_{EA1}	167Ω
R_{EAQ1}	21.4Ω
h_{FEQA1}	100

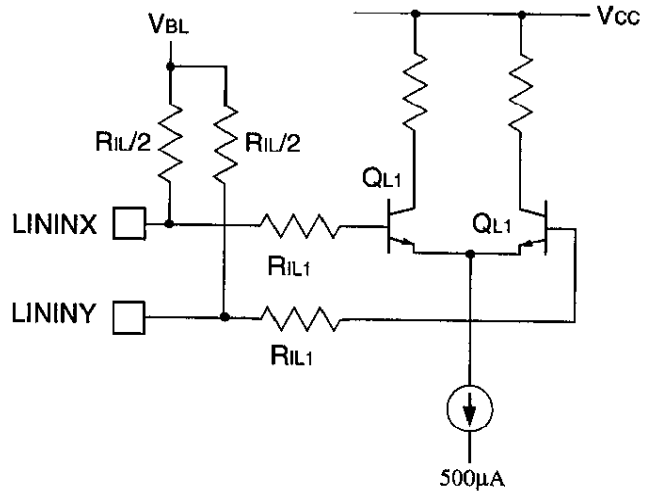
$R_{IN(AGC)} = R_{IA}/2 \;//\; h_{FEQA1} \times (R_{EQA1} + R_{EA1}/2)$
$= 1.5k\Omega \;//\; 10.49k\Omega$
$= 1.31k\Omega$

h_{FEQA1} : h_{FE} of Q_{A1}

R_{EA1} : Emitter resistance of Q_{A1}

■ LIN amplifier

Input impedance



$R_{IL}/2$	4.5kΩ
R_{IL1}	100Ω
R_{EQL1}	103Ω
h_{FEQL1}	100

$R_{IN(LIN)} \cong R_{IL}/2 \;//\; \{ R_{IL1} + h_{FEQL1} \times R_{EQL1} \}$
$\cong 3.14k\Omega$

h_{FEQL1} : h_{FE} of Q_{L1}

R_{EQL1} : Emitter resistance of Q_{L1}

26. AGC(Automatic Gain Control) amplifier circuit

The AGC amplifier is a three-stage differential amplifier. The first stage has variable gain and the second and third satges have fixed gain. The AGC block consists of the first and second gain stages. The output of the active filter (FILOUT and DIFOUT) stage is the third gain stage of the AGC block.

Active Filter Block Diagram

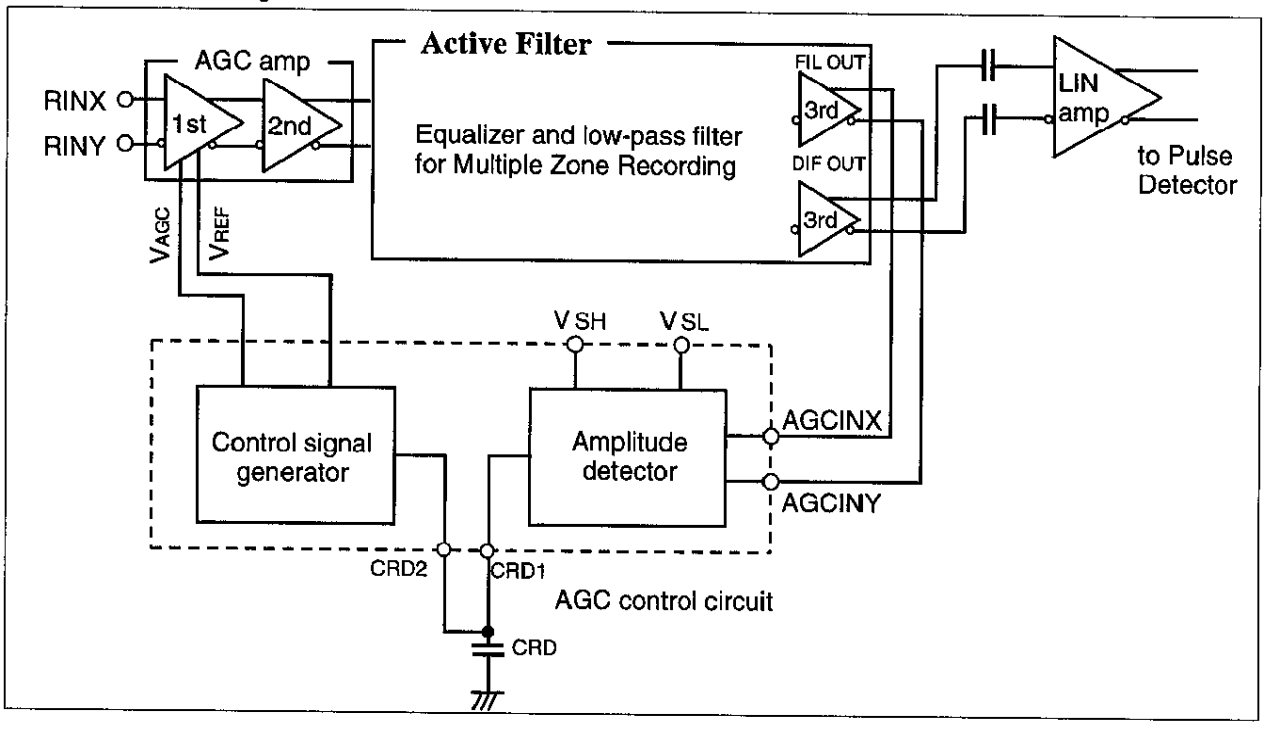


Fig.2 Active Filter Block Diagram

The first-stage gain can be controlled in the range from - ∞ to approximately 15 dB by an amplitude control signal (VAGC) from the AGC control circuit. The first-stage gain is given by the following formula.

$$Av = K_1 \cdot \left(\frac{1}{1 + \exp\left(qV_C / kT\right)} \right)$$

$K_1 = 5.62$
$V_C = V_{AGC} - V_{REF}$
q: unit electrical charge
k: Bolzmann constant
T: absolute temperature

The second-stage amplifier has fixcd gains of 6dB.

The third-stage amplifier within the Active filter has fixed gains of 20dB (at the outputs of FILOUT).

The AGC full gain is 112V/V (= 41 dB).

The AGC amplifier gain control system is shown in figure 2. The AGC amplifier output is amplified by the post-amplifier and buffer amplifier, then passed through a low-pass filter. The low-pass filter output is connected to the differentiating amplifier, and is also feedback to the AGC control circuit. Here it is compared with reference voltages (V_{SH} and V_{SL}) that are set externally, then the external capacitor (C_{RD}) is charged or discharged. The charging/discharging of the external capacitor varies the control signal V_{AGC} which directly affects the gain of the AGC amplifier. The final amplitude V_P (of the AGCINX and AGCINY waveforms) in this control system can be calculated from the following equations, assuming sine waveforms:

$$T_1 \times I_{ch} = T_2 \times I_{dis} \qquad (26\text{-}1)$$

$$T_1 = \left(1 - \frac{2}{\pi}\sin^{-1}\frac{V_{COM} - V_{SH}}{V_P}\right) \times T \qquad (26\text{-}2)$$

$$T_2 = \left(1 - \frac{2}{\pi}\sin^{-1}\frac{V_{COM} - V_{SL}}{V_P}\right) \times T \qquad (26\text{-}3)$$

From equations (26-1), (26-2), and (26-3):

$$\sin^{-1}\frac{V_{COM} - V_{SH}}{V_P} - \frac{I_{dis}}{I_{ch}}\sin^{-1}\frac{V_{COM} - V_{SL}}{V_P} = \frac{\pi}{2}\left(1 - \frac{I_{dis}}{I_{ch}}\right) \qquad (26\text{-}4)$$

The final amplitude of the AGC amplifier loop is determined mainly by V_{SH} bias level. If appropriate values are set for V_{SL}, Ich and Idis, then from the preceding equations the final differential peak voltage V_{PDF} is:

$$V_{PDF} = 4\,(V_{COM} - V_{SH}) \times m \qquad (26\text{-}5)$$

where m = 1.02 to 1.04

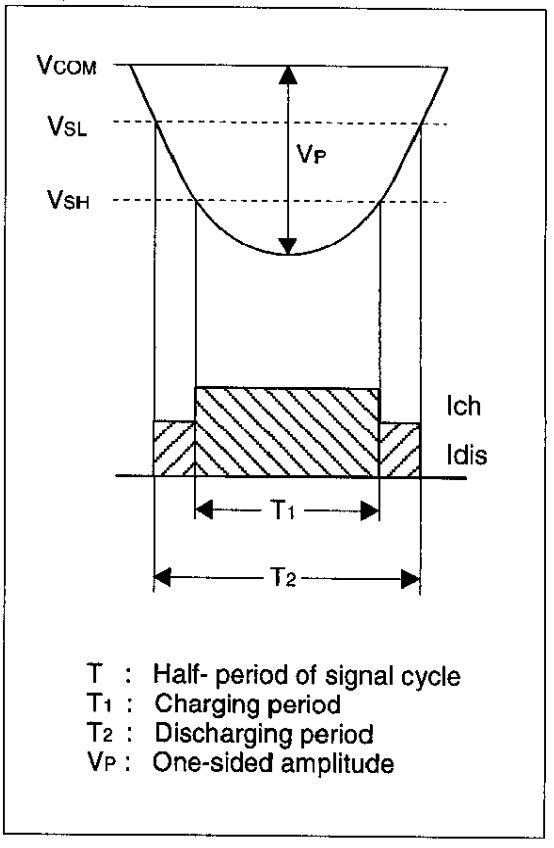
$$V_{COM} = \frac{4}{5} V_{CC}$$

The preceding V_{PDF} is determined by the signal waveform, the output dynamic range of the amplifiers, and other factors. An appropriate value is V_{PDF} = 1.7V ± 0.1V. Accordingly, (V_{COM} - V_{SH}) should be from 0.2V to 0.3V. V_{SL} should normally be about:

$$V_{COM} - V_{SL} = 0.67\,(V_{COM} - V_{SH}) \qquad (26\text{-}6)$$

The value must be determined from the resolution specifications, however. The procedure is to determine V_{SH} and V_P from equation (26-4), then

Amplitude



set Ich = 1.0mA and Idis = 0.2mA to determine VSL. Attenuation of signal amplitudes internal to the disk drive with respect to signal amplitudes external to the disk drive must be considered. For example, from equation (26-5), (V_{COM} - V_{SH}) = 0.239V and m = 1.03 gives V_{PDF} = 0.985 V, and from equation (26-4), (V_{COM} - V_{SL}) = 0.10 V, but if the input amplitude is instantaneously attenuated from its previous value to a new value that is not larger than (V_{COM} - V_{SL}), the amplitude recovery time might be excessively long. Next, it is necessary to consider the relationship of the recovery time to the charge-discharge capacitor C_{RD}. The C_{RD} capacitance should be close to the following value:

$$C_{RD} = \frac{200000}{\text{Transfer rate (Mbps)}}\ (\text{pF}) \qquad (26.7)$$

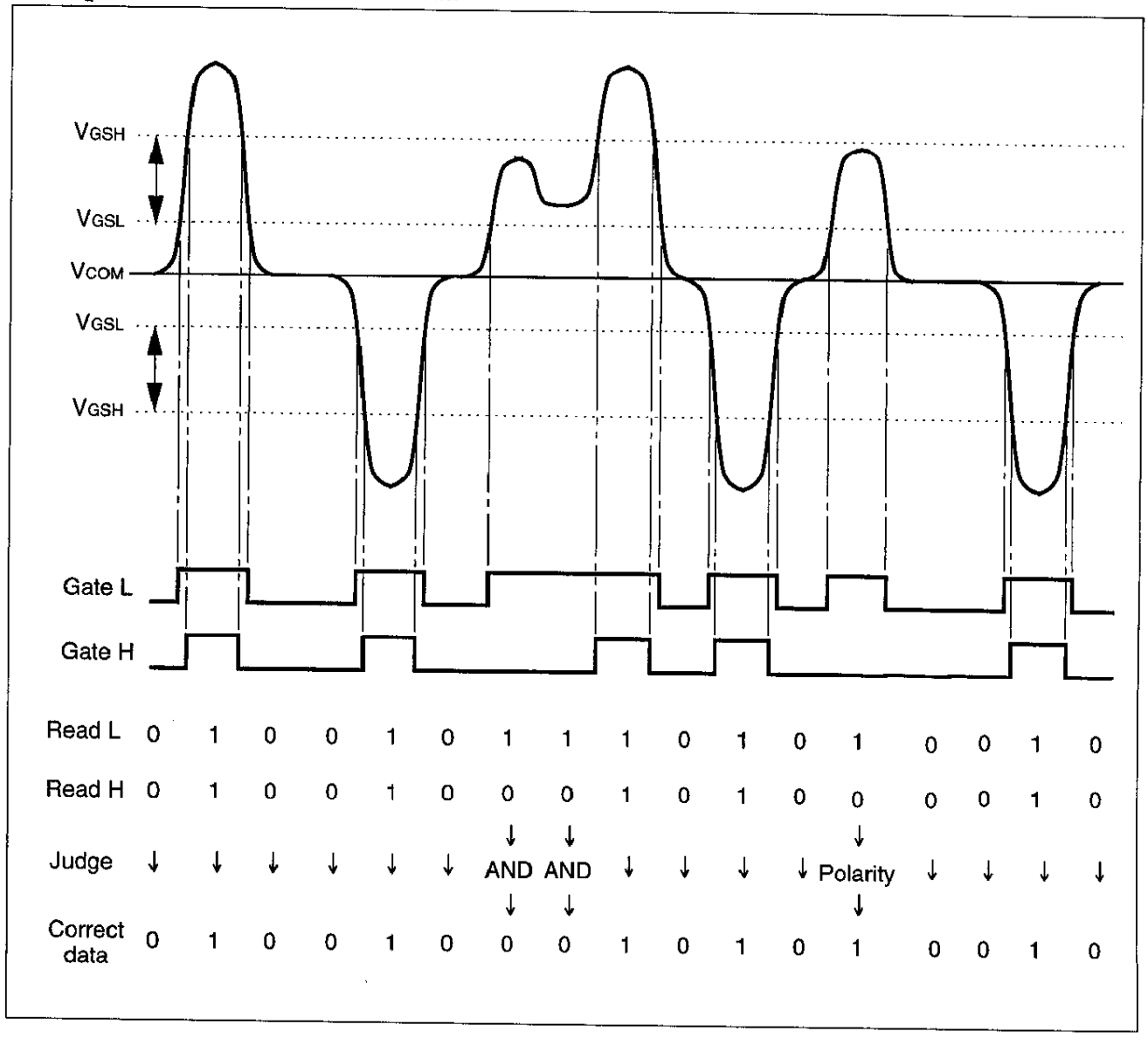
The write-to-read recovery time t_R is then :

$$t_R = 200 \times C_{RD}\ (\text{seconds}) \qquad (26.8)$$

27. Gate Generator Circuit

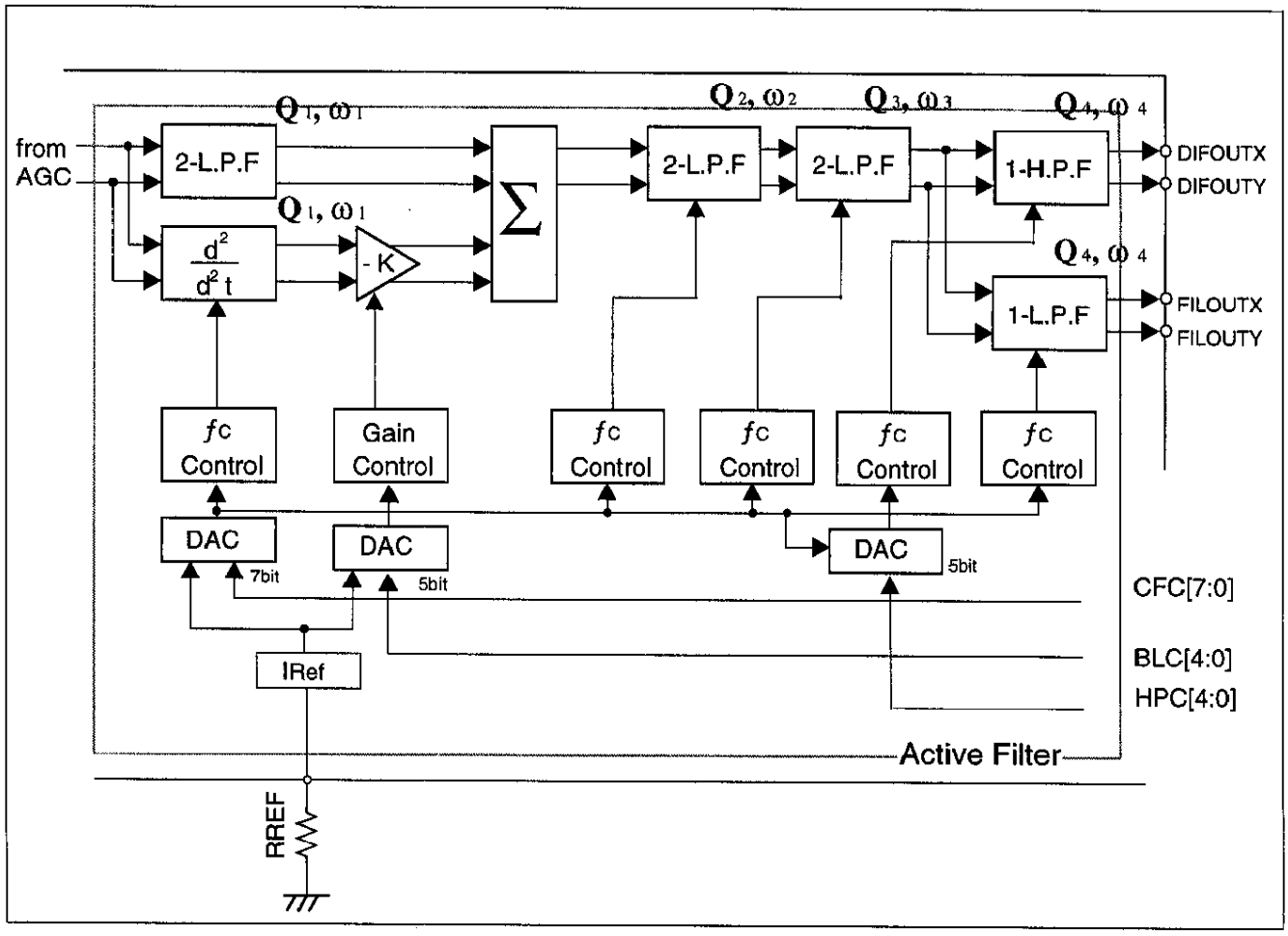
A gate signal is used to gate the read signal near its peak value to remove incorrect read pulse. This gate signal is created by the gate generator circuit. The principle is to ensure that the read pulse crosses two programmable slice levels before being gated out as PDRD signal. For normal read mode, shifter and logic are used to qualify pulses that crosses only the low slice level or multiple peaks that would require polarity checking. The two slice levels VGSL and VGSH are set by writing to the VGSH and VGSL 4-bit registers. The High slice level is programmed to covered 0% to 100% of the VSH level and the Low slice level would covered 0 % to 100% of the VSH. In servo mode, if one pulse is missing because it is not meeting the Low slice level, the next qualifying pulse will be disqualified as well.

Principal of Gate Generation Circuit.

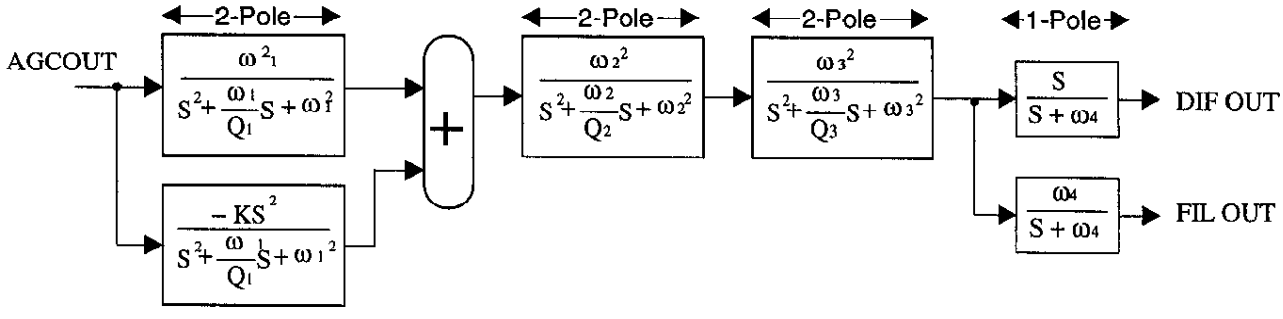


28. Active Filter

Active Filter consists of equalizer and electronic filter. Electronic filter is 7-pole, Bessel-type, low-pass filter and can be used in multiple zone recording (MZR) design. Cut-off frequency of filter is set by writing to register CFC. Writing to the HPC register will set the high-pass cut-off frequency of the differential amplifier. The equalizer is double differentiation pulse sliming equalization. The Boost level is set by writing to register BLC.



Transfer function



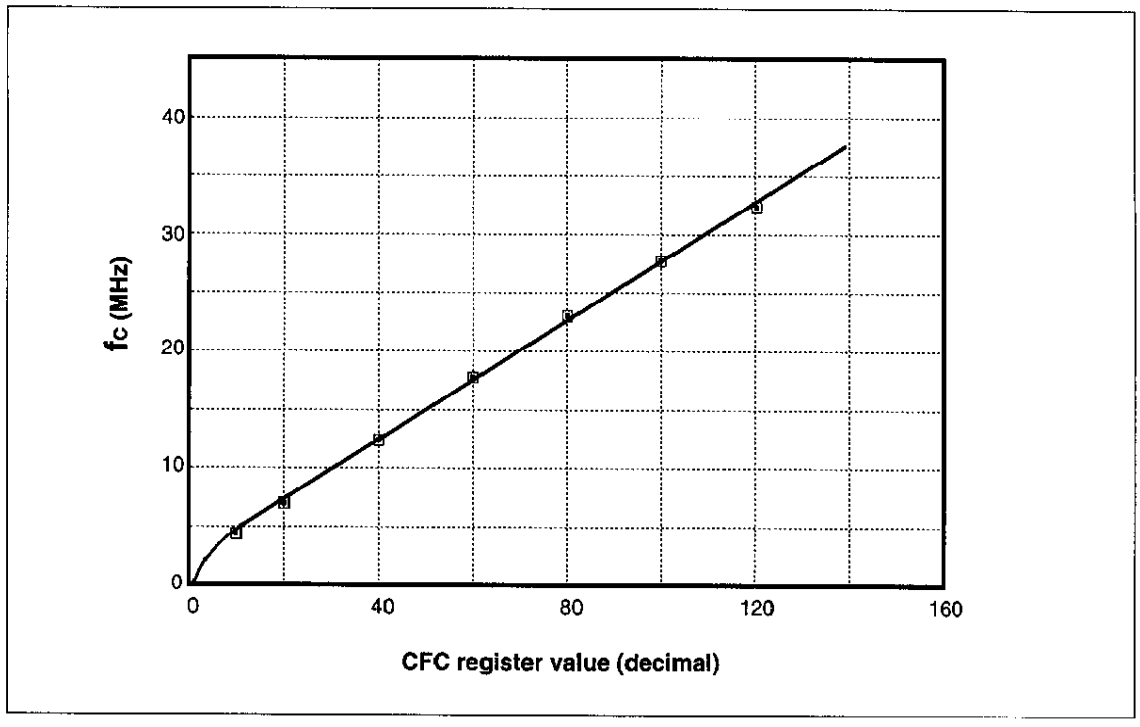


Fig 28. 1 fc vs CFC register

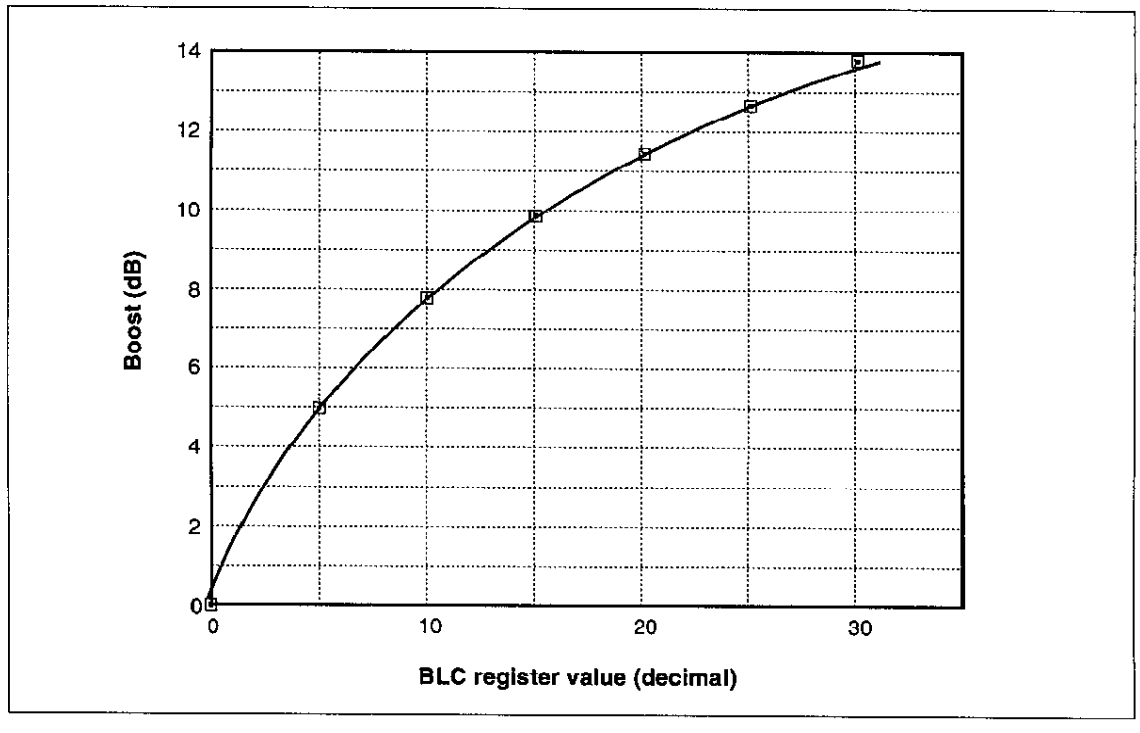


Fig 28. 2 Boost vs BLC register

Normalized Constant of 7-pole Bessel filter

Parameter	Normalized constant ($\omega_c = 1$)
ω_{1}	2.94930
ω_1 / Q_1	3.22597
ω_{2}	3.32507
ω_2 / Q_2	2.75939
ω_{3}	4.20534
ω_3 / Q_3	1.82031
ω_4	1.68536

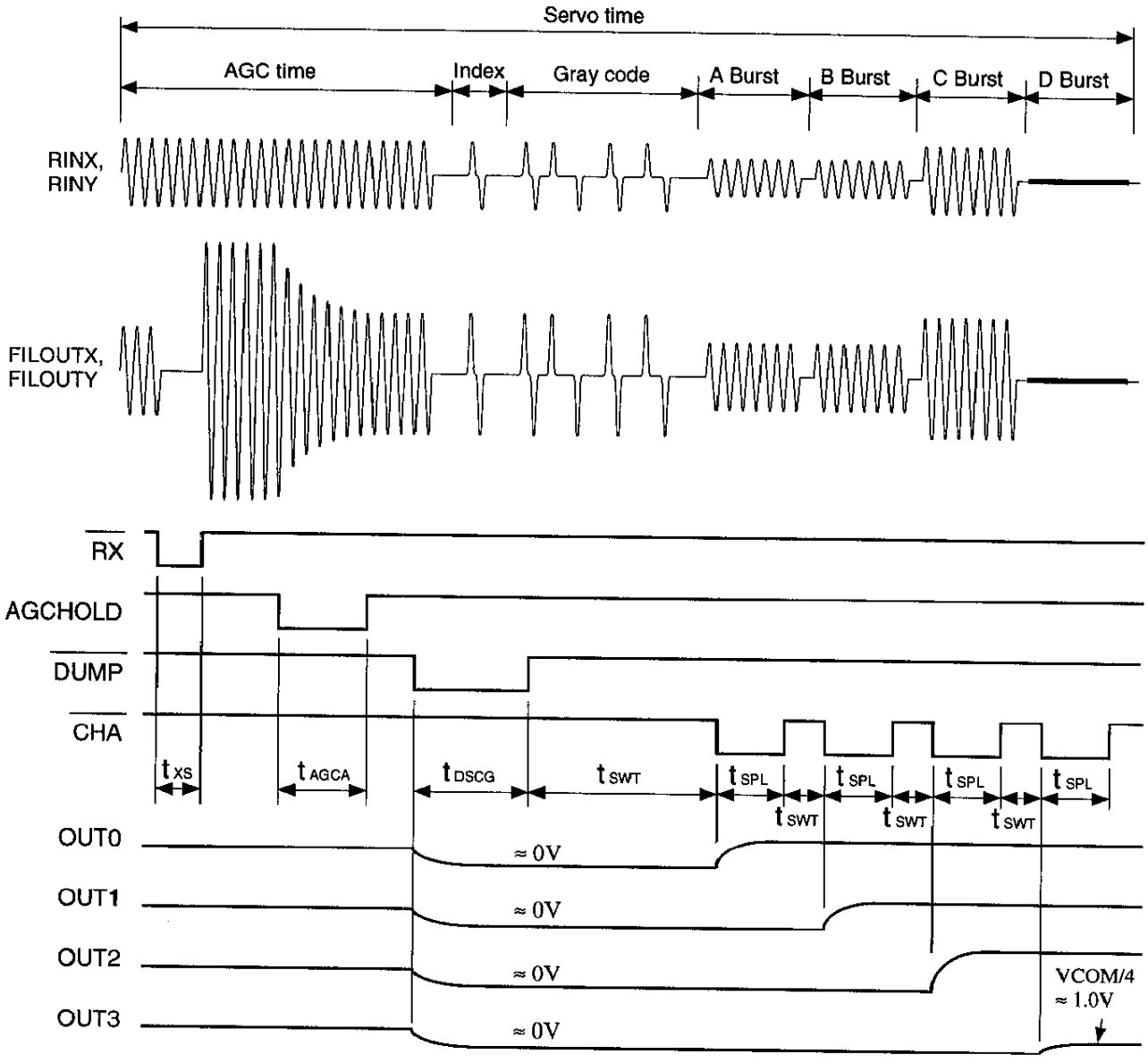
29. Idle input pin for power saving:

With the mode control register(PCN), there are four different modes of operation as shown: 11 = Sleep, 10 = Power Save, 00 = Normal (full power).The modes are defined as followed:

a) When bit5,4 = 00 : **Normal** mode. All circuitries should be powered.
b) When bit5,4 = 11 : **Sleep** mode. Everythings powered down except the I/O and the logic section of the chip.
c) When bit5,4 = 10 : **Power Save** mode. In this mode, the Idle/Servo pin will select which of the two power save modes to be used. If Idle = 1 then Idle mode is selected and all modules will be powered down except for the I/O, logic, and the bias circuitries.. If Idle/Servo = 0 then Servo mode will be selected and all blocks will be kept on except the clock syncthesizer (WR PLL) and the synchronizer (RD PLL).

	Mode	PCN Reg. Bit5, 4	I/$\overline{S}$ pin	I/O	Logic	Bias	RD PLL	WR PLL	AGC	AF	RPD	PH
	Normal	00	X	ON	ON	ON	ON	ON	ON	ON	ON	ON
Power Save	Servo	10	0	ON	ON	ON			ON	ON	ON	ON
Power Save	Idle	10	1	ON	ON	ON						
	Sleep	11	X	ON	ON							

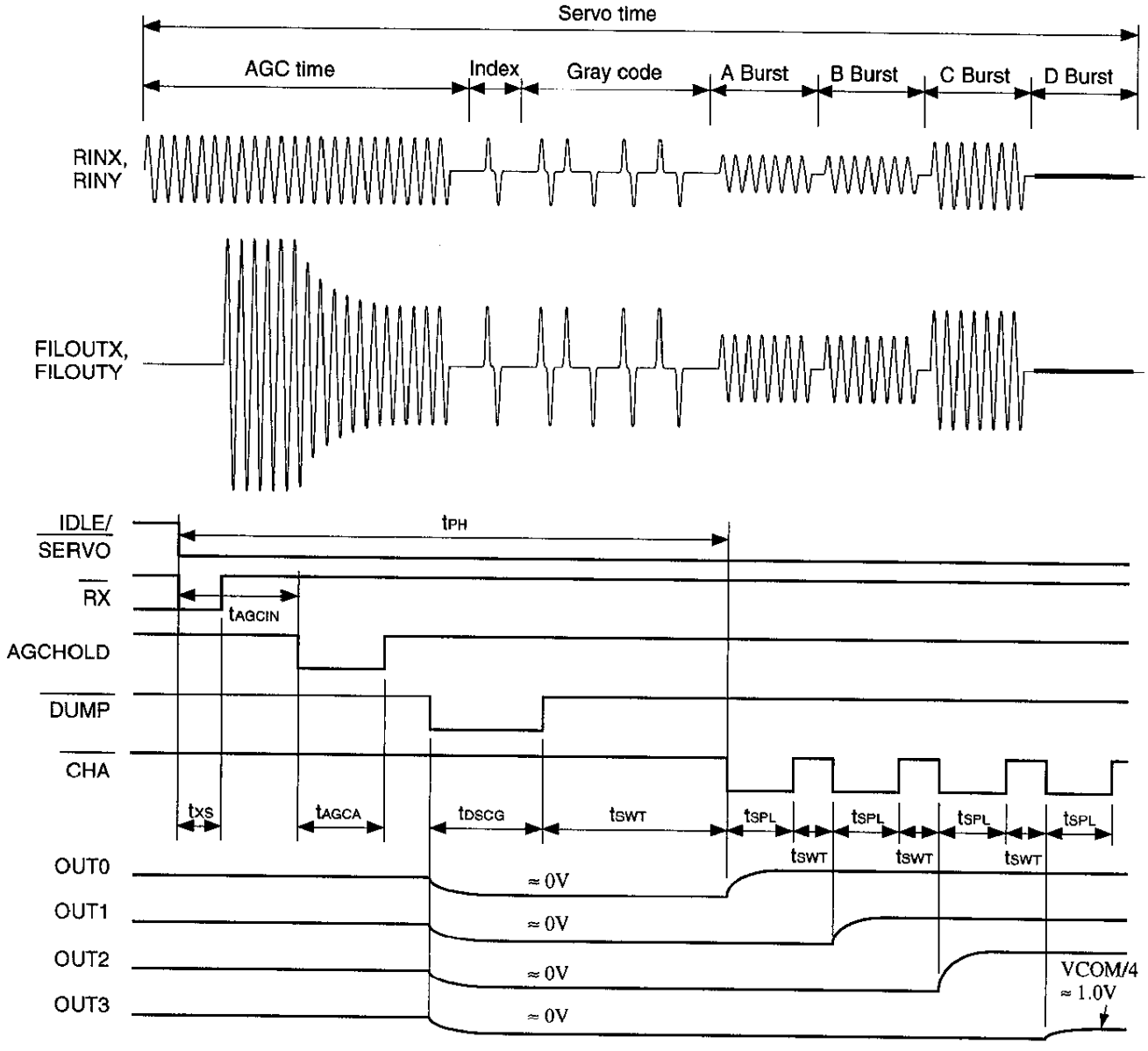
30. Example of the Normal to Servo mode waveform



When D Burst is no signal coming out.

Symbol	min	typ	max	unit	Conditions
t_{XS}	150			ns	
t_{AGCA}			2	µs	CRD=3300pF
t_{DSCG}			2	µs	C_{OUT0}~C_{OUT3}=1000pF
t_{SWT}	200			ns	
t_{SPL}	2			µs	

31. Example of the Idle to Servo mode waveform

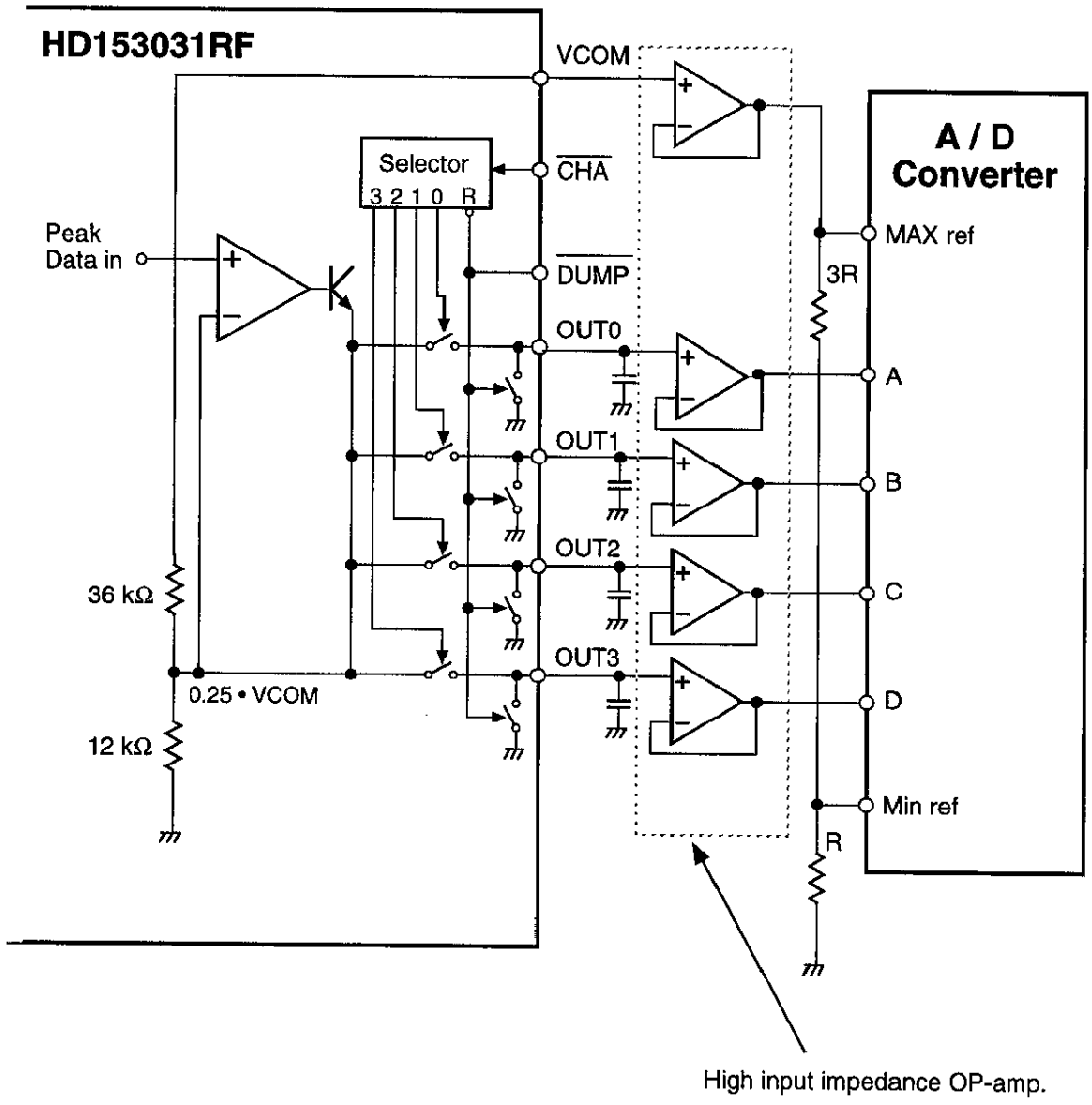


When D Burst is no signal coming out.

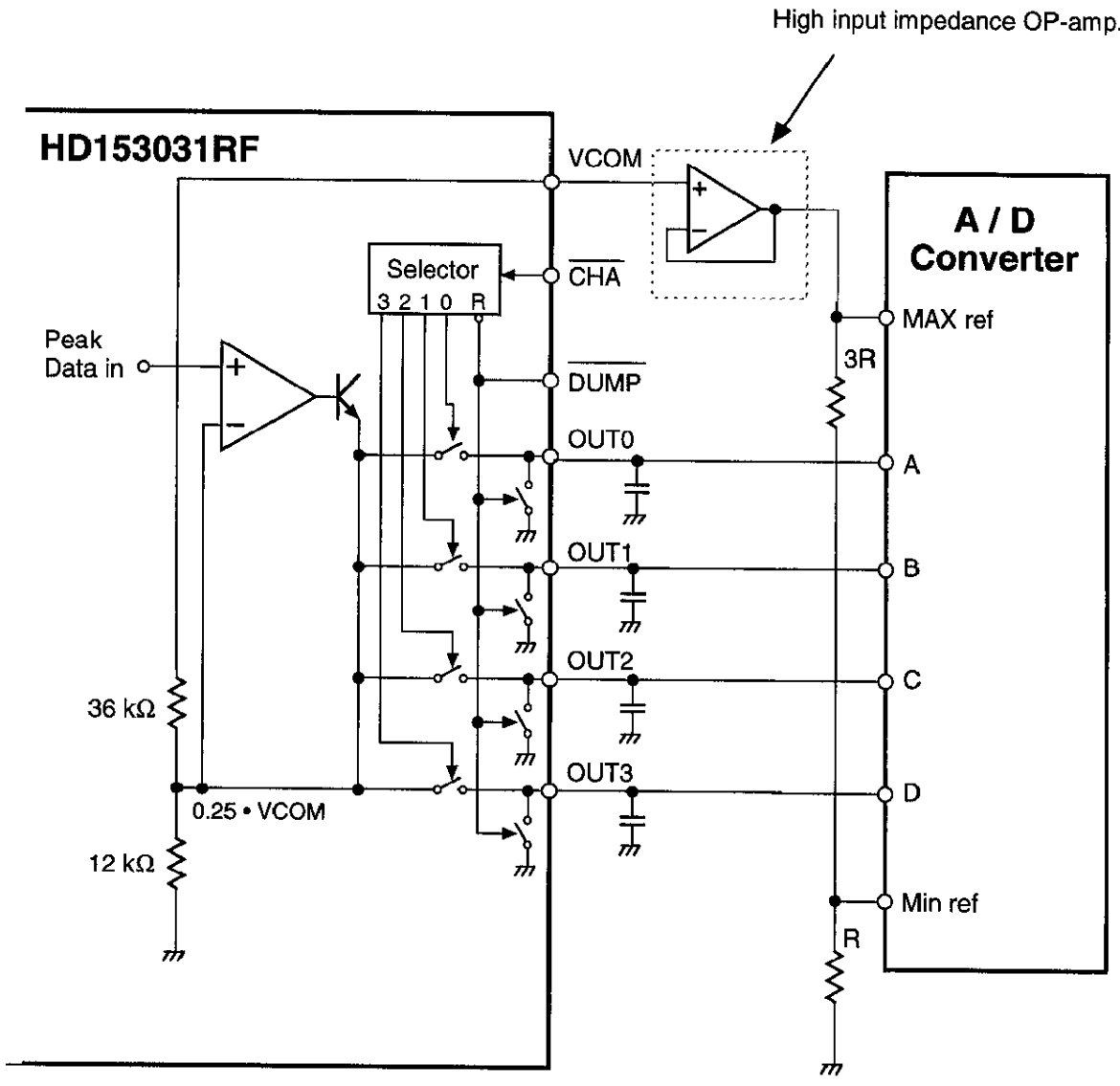
Symbol	min	typ	max	unit	Conditions
t_{XS}	4			µs	C_{AGCIN}=2200pF
t_{AGCA}			5	µs	CRD=3300pF
t_{DSCG}			2	µs	C_{OUT0}~C_{OUT3}=1000pF
t_{SWT}	200			ns	
t_{SPL}	2			µs	
t_{PH}	60			µs	C_{PHIN}=2200pF
t_{AGCIN}	10			µs	C_{AGCIN}=2200pF

32. Servo application example (external compornents)

(1) Low input impedance Digital to Analog Converter application



(2) High input impedance Digital to Analog Converter application



33. Absolute Maximum Ratings (Ta=25 °C)

Description	Symbol	Ratings	Unit	Applicable pins
Supply voltage	Vcc	7	V	DVcc,AVcc(PH),AVcc(W),AVcc(R) AVcc(AF),AVcc(AGC),AVcc(RPD)
Input voltage	VI	- 0.3 to 5.5	V	Note1
Output voltage	Vo	5.5	V	Note2
Operating temperature	Topr	0 to 70	°C	
Storage temperature	Tstg	- 55 to + 125	°C	

Note1: OSCCLK,$\overline{\text{RESET}}$,IDLE/$\overline{\text{SERVO}}$,$\overline{\text{RSENA}}$,SCLK,SDATA,$\overline{\text{DUMP}}$,$\overline{\text{CHA}}$,$\overline{\text{SHORT}}$,$\overline{\text{RX}}$,AGCHOLD,RG, SRV/$\overline{\text{RD}}$,NRZRD/WD0(Write mode),NRZRD/WD1(Write mode),WG,$\overline{\text{AME}}$

Note2: SDATA,AMF,$\overline{\text{ULD}}$,PDRD,$\overline{\text{DLYCLK}}$,$\overline{\text{DLYRD}}$,$\overline{\text{SYNCRD}}$,RRCLK,CLKOUT1-7WDOUT,$\overline{\text{1-7WDOUT}}$, NRZRD/WD0(Read mode),NRZRD/WD1(Read mode)

34. Electrical Characteristics (Ta=0 to + 70℃, unless otherwise specifiedVcc = 5.0V ± 10%)

Item	Symbol	min.	typ.	max	Unit	Conditions	Applicable Pins	Note
Supply Voltage	Vcc	4.5	5	5.5	V		*4	
Operating Temperature	Ta	0	25	70	℃			
Transfer Rate		10		36	Mbps			
Current Consumption	Icc(read)			240	mA	5.5V 36Mbps	*4	
				200	mA	5.5V 24Mbps	*4	
	Icc(write)			240	mA	5.5V 36Mbps	*4	
				200	mA	5.5V 24Mbps	*4	
	Icc(servo)			170	mA	5.5V 36Mbps	*4	
	Icc(idle)			15	mA	5.5V	*4	
	Icc(sleep)			13	mA	5.5V	*4	
TTL High Level Input Voltage	VIH	2.2			V	Vcc=4.5V	*1	
TTL Low Level Input Voltage	VIL			0.80	V	Vcc=4.5V	*1	
TTL High Level Output Voltage	VOHT	2.4			V	IOH=-400 μA, Vcc=4.5V	*2	
TTL Low Level Output Voltage	VOLT			0.5	V	IOL=4mA, Vcc=4.5V	*2	
ECL High Level Output Voltage	VOHE	Vcc -0.95	Vcc -0.8		V	Ta=25℃, RL=510Ω	*3	
ECL Low Level Output Voltage	VOLE		Vcc -1.8	Vcc -1.6	V	Ta=25℃, RL=510Ω	*3	
Input Current	IIH			20	μA	Vcc=5.5V, Vi=2.7V	*1	
	IIL			-400	μA	Vcc=5.5V, Vi=0.4V	*1	
Output Short Current	Ios	-20		-120	mA	Vcc=5.5V	*2	
Input Clamp Voltage	VIK			-1.5V	V	Vcc=5.5V	*1	

* 1: OSCCLK,RESET,IDLE/SERVO,RSENA,SCLK,SDATA,DUMP,CHA,SHORT,RX,AGCHOLD,RG, SRV/RD,NRZRD/WD0(Write mode),NRZRD/WD1(Write mode),WG,AME
* 2: SDATA,AMF,ULD,PDRD,DLYCLK,DLYRD,SYNCRD,RRCLK,CLKOUT,1-7WDOUT(TTL), 1-7WDOUT(TTL), NRZRD/WD0(Read mode),NRZRD/WD1(Read mode)
* 3: 1-7WDOUT(ECL),1-7WDOUT(ECL)
* 4: DVcc,AVcc(PH),AVcc(W),AVcc(R),AVcc(AF),AVcc(AGC),AVcc(RPD)

35. Encoder/Decoder(Ta=25°C, Vcc=5V, 36Mbps)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
NRZRD set-up time(serial)	t_{SNRS}	9.0			ns		NRZRD/WD0
NRZRD set-up time(parallel)	t_{SNRP}	15.0			ns		NRZRD/WD0,1
NRZRD hold time(serial)	t_{HNRS}	8.0			ns		NRZRD/WD0
NRZRD hold time(parallel)	t_{HNRP}	18.0			ns		NRZRD/WD0,1
NRZWD set-up time(serial)	t_{SNWS}	8.0			ns		NRZRD/WD0
NRZWD set-up time(parallel)	t_{SNWP}	21.0			ns		NRZRD/WD0,1
NRZWD hold time(serial)	t_{HNWS}	0			ns		NRZRD/WD0
NRZWD hold time(parallel)	t_{HNWP}	0			ns		NRZRD/WD0,1
Decode time	t_{DD}		14	16	RRCLK		NRZRD/WD0
Encode time	t_{ED}		12	14	RRCLK		$\overline{\text{1-7WDOUT}}$, 1-7WDOUT
Write Precomp time step		0.28	0.55	0.82	ns	Not tested	
Write Precomp time width		± 2.0	± 3.85	± 5.7	ns	± 7steps	

36. Register (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
RSENA "L" time	t_{EL}	1650			ns		RSENA
RSENA "H" time	t_{EH}	50			ns		RSENA
RSENA falling edge to the first SCLK falling edge	t_{EFSF}	50			ns		SCLK
SDATA set up time	t_{CDS}	10			ns		SDATA
SDATA hold time	t_{CDH}	10			ns		SDATA
The last SCLK rising edge to RSENA rising edge	t_{SRER}	50			ns		RSENA
SCLK cycle time	t_{CC}	100			ns		SCLK
SCLK "H" time	t_{CH}	40			ns		SCLK
SCLK "L" time	t_{CL}	40			ns		SCLK
SDATA output delay	t_{CDD}			20	ns		SDATA
SDATA output hold time	t_{EDH}	5			ns		SDATA

37. Synchronizer (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Read VCO center frequency 1	fvco1	34.2	36	37.8	MHz	RFVCO=3k, Register VFC=80 Hex
Phase lock acquisition time 1		—	—	6	Byte	6 NRZ bytes period at 24Mbps
Capture range 1		±15	—	—	%	at 24Mbps
Lock range 1		±15	—	—	%	at 24Mbps
Read VCO gain 1		126	160	194	Mrad / sec •V	RFVCO=3k, Register VFC=80 Hex
Read VCO upper limit clamping frequency 1		—	48	—	MHz	RFVCO=3k, Register VFC=80 Hex
Read VCO lower limit clamping frequency 1		—	27	—	MHz	RFVCO=3k, Register VFC=80 Hex
Read VCO center frequency 2	fvco2	67.5	71.5	75.5	MHz	RFVCO=3k, Register VFC=FF Hex
Phase lock acquisition time 2		—	—	6	Byte	6 NRZ bytes period at 36Mbps
Capture range 2		±15	—	—	%	at 36Mbps
Lock range 2		±15	—	—	%	at 36Mbps
Read VCO gain 2		174	220	266	Mrad / sec •V	RFVCO=3k, Register VFC=FF Hex
Read VCO upper limit clamping frequency 2		—	95	—	MHz	RFVCO=3k, Register VFC=FF Hex
Read VCO lower limit clamping frequency 2		—	53	—	MHz	RFVCO=3k, Register VFC=FF Hex
Window margin loss		0		3	ns	at any data rate
Window adjust tap		0.34	0.67	1.0	ns	Not tested
Window adjust width		+5.5 −5.9	+10.0 −10.7	+14.5 −15.5	ns	+15step, −16step
Window fine adjust tap		0.12	0.25	0.5	ns	Not tested
Read VCO maximum oscillate frequency		90	108	—	MHz	RFVCO=1k, Register VFC=80 Hex
Decode window center accuracy		-4.2		0.6	ns	at 24Mbps
T/I offset accuracy		-1.8		5.0	μA	at 24Mbps
C/P offset accuracy		-15		+15	%	at GAC=20Hex
Oscillation Start Voltage				4.0	V	Ta=25℃, fosc≧100KHz

38. Synthesizer (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Write VCO center frequency	fwvco	67.5	71.5	75.5	MHz	RSVCO=6.2k, Register VFC=FF Hex
Write VCO upper limit clamping frequency		—	86	—	MHz	RSVCO=6.2k, Register VFC=FF Hex
Write VCO lower limit clamping frequency		—	56.8	—	MHz	RSVCO=6.2k, Register VFC=FF Hex
Phase lock acquisition time		—	—	1	ms	tested at 24Mbps,36Mbps
Capture range		±10	—	—	%	tested at 24Mbps,36Mbps
Lock range		±10	—	—	%	tested at 24Mbps,36Mbps
VCO frequency step		—	1.0	—	%	at f_{MAX} / f_{LOW} = 2.55
VCO gain		84	106	128	Mrad / sec • V	RSVCO=6.2k, Register VFC=FF Hex
Max frequency		80	—	—	MHz	RSVCO=2.3k, Register VFC=80 Hex

39. RPD & PH (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions	Applicable pins
Max peak-peak Input signal				2.0	Vpp	differential inputs	PHINX/Y
PDRD pulse width		4.5	9	13.5	ns	at 36Mbps, PW[1:0]=00	
PDRD pulse rise time	tr	0.5	2	4	ns	CL=15pF,20%-80%	Not tested
PDRD pulse fall time	tf	0.5	2	4	ns	CL=15pF,80%-20%	Not tested
P/H output voltage swing		2.0	2.3	2.6	V	fin=6.5MHz, Vin=2Vpp **	
P/H output leakage current		-0.2	0	+0.2	µA		OUT0 ~ OUT3
P/H Channel Offset		-50	0	+50	mV		OUT0 ~ OUT3
P/H Reference Voltage			VCOM x 25%		V	PHINX/Y=0Vpp	OUT0 ~ OUT3
P/H Discharge time	t_{DSCG}			2.0	µS	C_{OUT0} ~ C_{OUT3} =1000pF	OUT0 ~ OUT3 $\overline{DUMP}$
P/H Sampling time ($\overline{CHA}$ = "L" time)	t_{SPL}	2.0			µS		$\overline{CHA}$
$\overline{CHA}$ Switching time	t_{SWT}	200			ns		$\overline{CHA}$

** : differential input for PHINX and PHINY.

40. Active Filter (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
Filter cutoff frequency	fc	5		25	MHz	
fc Accuracy	fca	- 15		+15	%	
Filter boost level	Fb	0		10	dB	
Filter boost Accuracy	Fba	- 1		1	dB	Fb = 10dB
Output dynamic range		1.5	1.8	2.0	Vpp	diff. outputs, THD < 1% Not tested
Output noise(normal)			3	5.5	mVRms	Not tested
Output noise(differential)			6	10	mVRms	Not tested
Group delay variation (0)		0		5	ns	fc=9MHz f=0.2fc to fc Boost=0dB, Not tested
		0		5	ns	fc=9MHz f=0.2fc to fc Boost=6dB, Not tested
Group delay variation (1)		0		5	%	fc=5MHz to 9MHz (f=0.2fc to fc Boost=0dB) Not tested
Power noise rejection	PSRR	45			dB	AGC+Active Filter Not tested
Common mode rejection	CMRR	40			dB	AGC+Active Filter f_{IN}=1MHz

Condition 1: fc =18MHz, range = 0.2fc to fc, measured from AGCOUTX/Y to FILOUTX/Y.

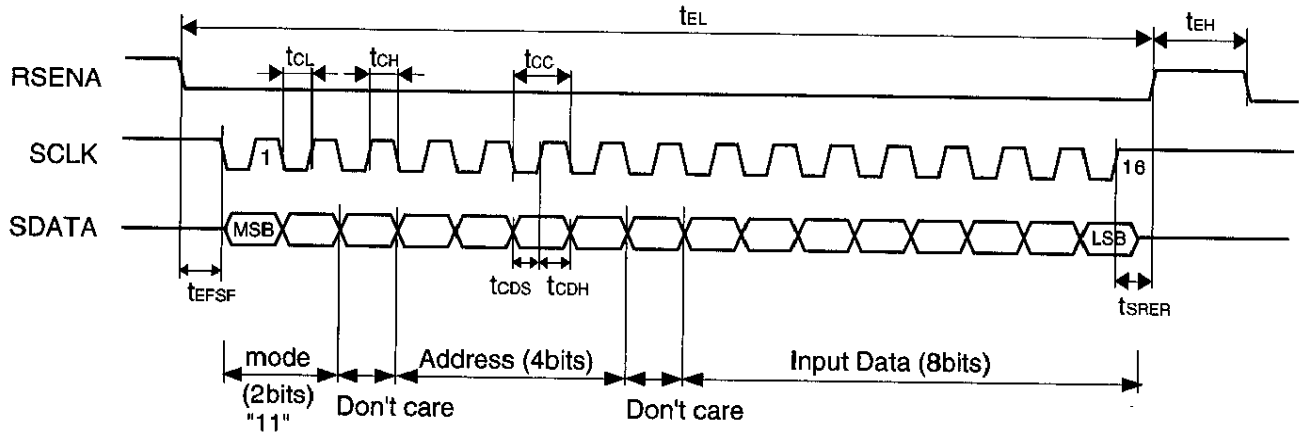
41. AGC (Ta=25°C, Vcc=5V)

Item	Symbol	min	typ	max	unit	conditions
AGC max gain		39	41		dB	RINX/Y to FILOUTX/Y
AGC min gain				0	V/V	$\overline{RX}$=Low
Input dynamic range		20		100	mV	Distortion <1% Not tested
Band width(-3dB)	Bw	50			MHz	Not tested
Output DC offset	Voff		100	200	mV	AGCOUTX/Y
Input noise(max gain)			5	15	nV/$\sqrt{Hz}$	Not tested
Write to read recovery time	twrr		1	2	µs	write($\overline{RX}$=L) to read cycle CRD=3300pF
Read recovery time	trr			5	µs	recovery from max gain
Idle to Servo AGC Recovery time	t_{AGC}		7	10	µs	C_{AGCIN}=2200pF
Idle to Servo P/H Recovery time	t_{PH}		40	60	µs	C_{PHIN}=2200pF
Sleep to Servo Recovery time				1	ms	

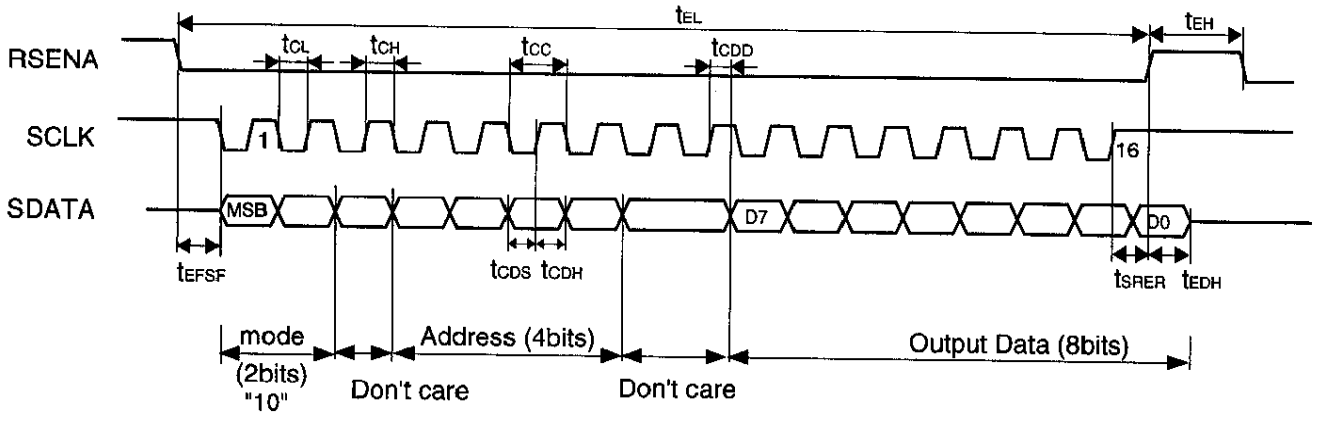
42. AC Timing Chart

(1) Register read / write

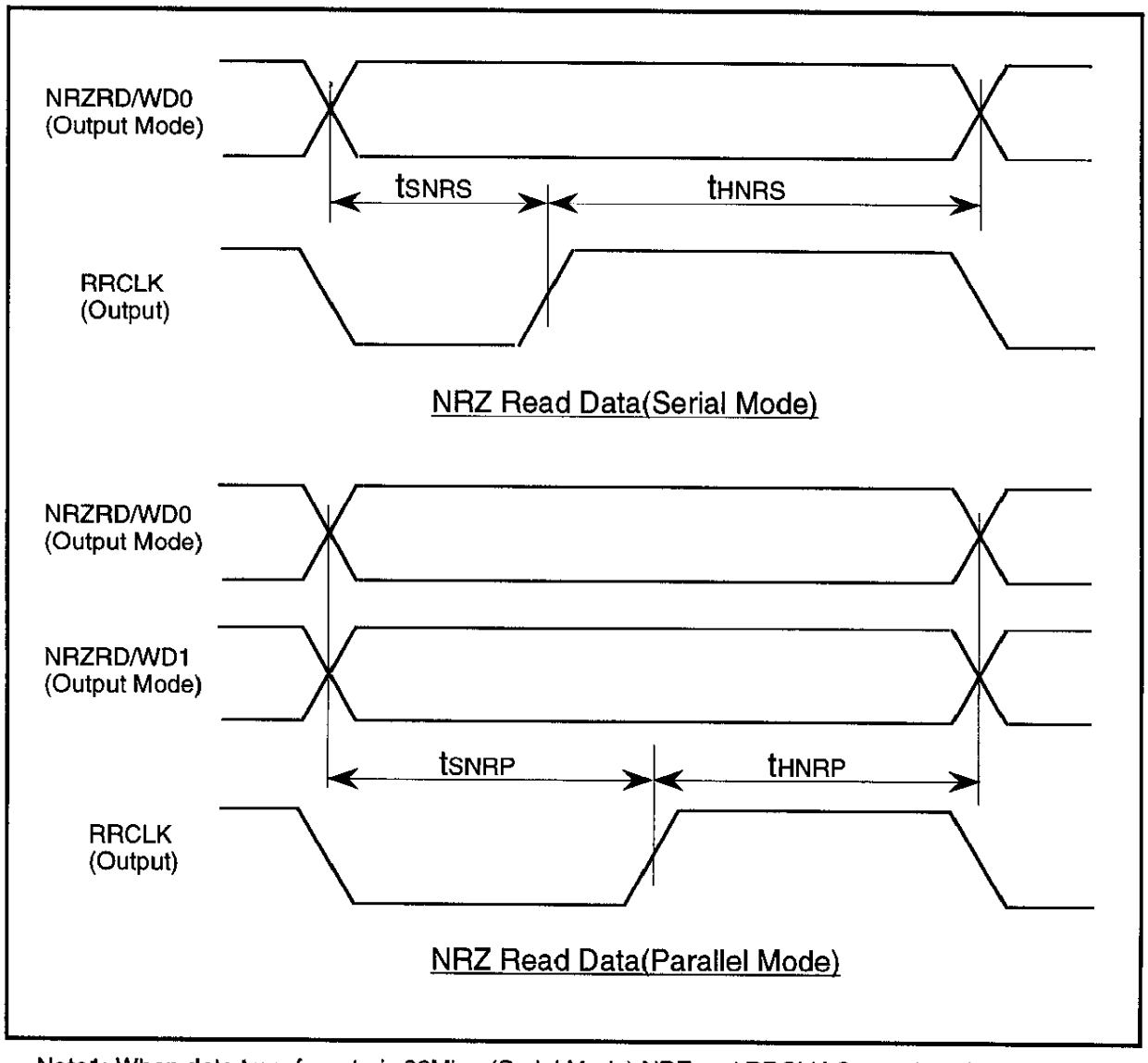
< Write >



< Read >

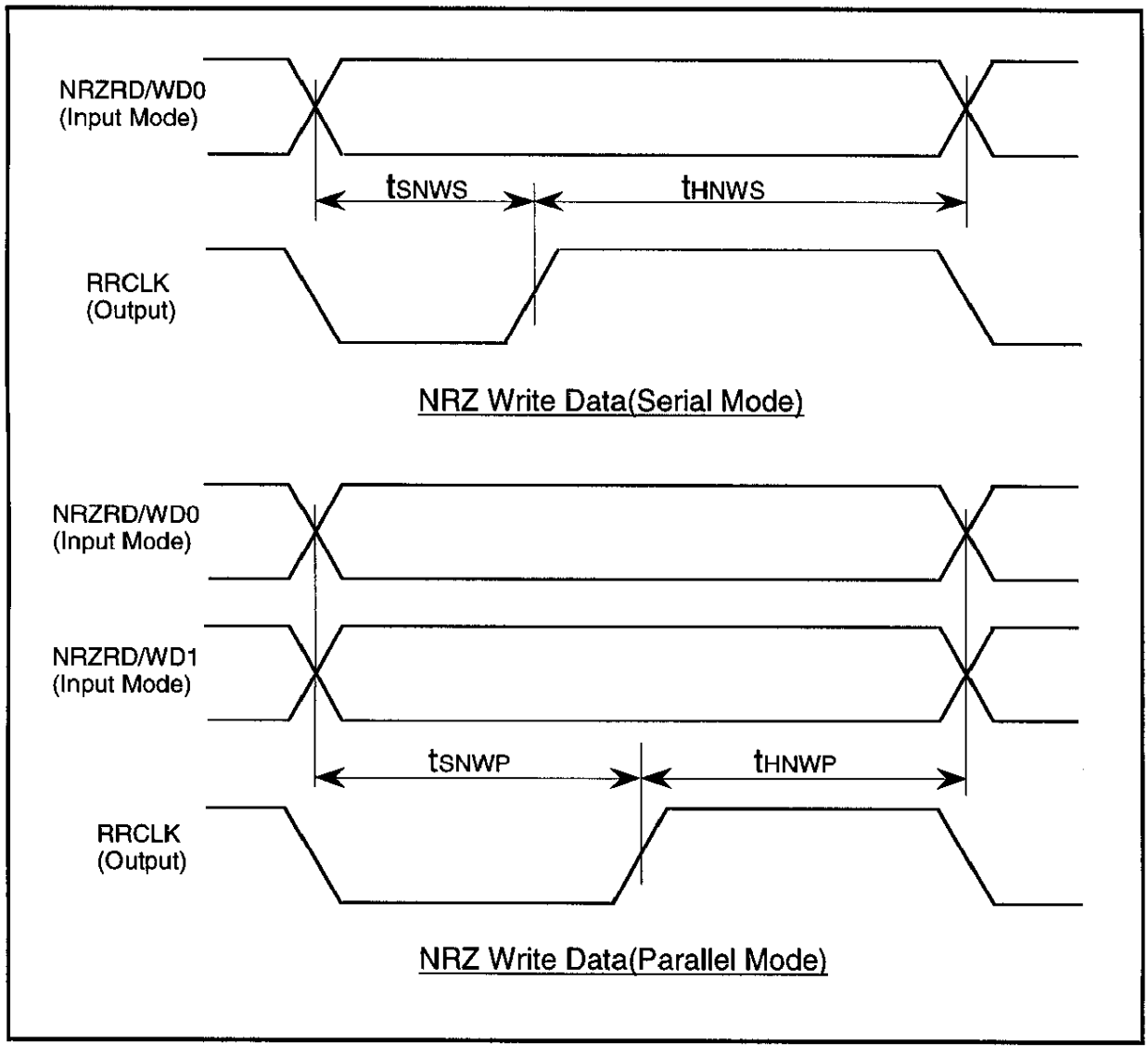


(2) Read for NRZ data



Note1: When data transfer rate is 36Mbps(Serial Mode),NRZ and RRCLK Output is 36MHz .
RRCLK clock duty "L":"H" =1:2.
When data transfer rate is 36Mbps(Parallel Mode),NRZ and RRCLK Output is 18MHz .
RRCLK clock duty "L":"H" =1:1

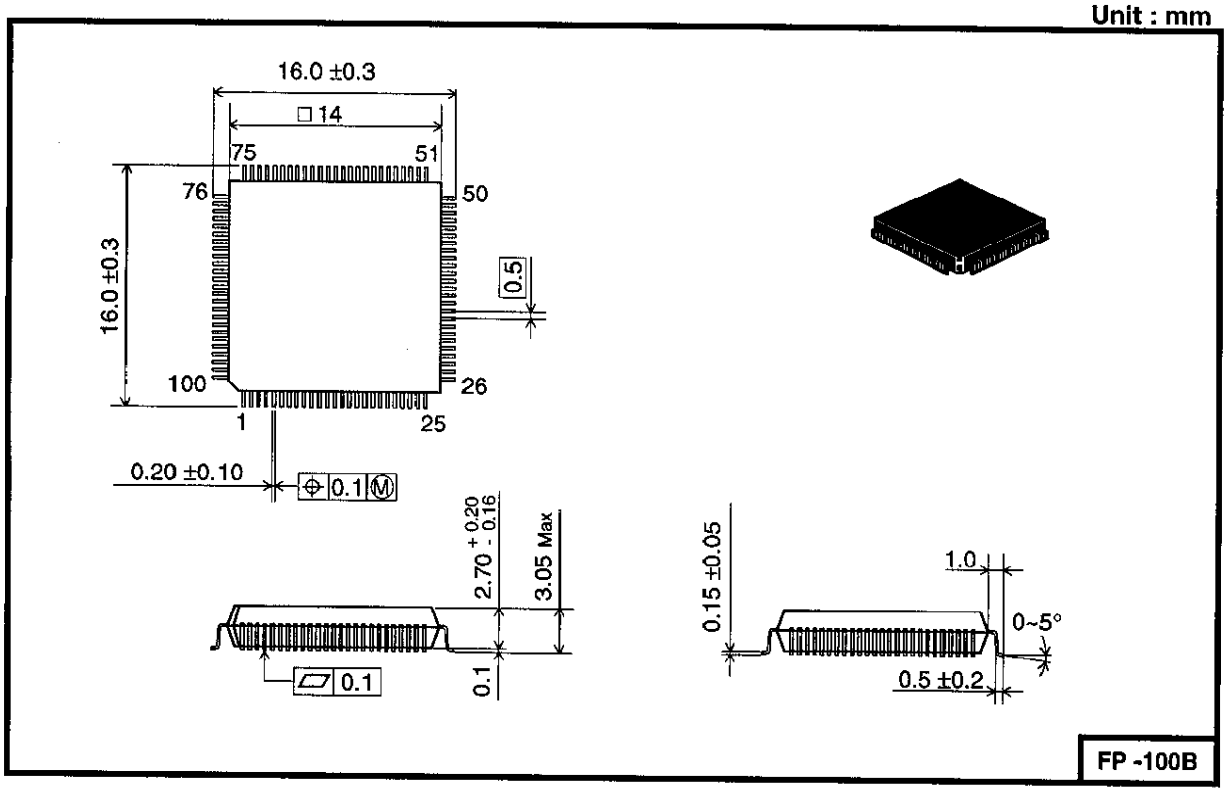
(3) Write for NRZ data



Note2: When data transfer rate is 36Mbps(Serial Mode), RRCLK Output is 36MHz .
RRCLK clock duty "L":"H" =1:2.
When data transfer rate is 36Mbps(Parallel Mode), RRCLK Output is 18MHz .
RRCLK clock duty "L":"H" =1:1

43. PACKAGE DIMENSIONS

Unit : mm



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