Single Chip Codec/Filter Circuit

GENERAL INFORMATION

The XR-T3052/3053/3054/3057 are monolithic PCM CODER and DECODER integrated circuits, designed in CMOS technology, and intended to implement the transmit and receive functions in digital telecommunication circuits. The XR-T3052/3053/3054 have a companded μ-law PCM format as opposed to the XR-T3057 which uses the A-law PCM format. Each device contains separate D/A and A/D circuitry, all necessary sample and hold switched capacitor filters, precision voltage reference and internal auto zero circuitry.

On the transmit side, the analog signal is first amplified and then prefiltered by a distributed RC network to eliminate high frequency noise before entering a switched capacitor bandpass filter. The coder then samples the filtered signal and encodes this in the companded μ or A law. On the receive side, the decoder reconstructs the analog signal from the incoming digital PCM code. The analog signal goes through a low pass filter with sinx/x correction and a driver to handle low impedance loads. Included also is a timing and control section, which is upward compatible with 3052/3053/3054/3057 industry standard devices.

APPLICATIONS

Digital Telephone
Digital PABX'S
Digital PBX
ISDN Networks

FEATURES

Fully Differential Data Paths
Transmit High Pass, Low Pass Filtering
Receive Low Pass Filter with Sin x/x Correction
U-Law or A-Law COding and DECoding
Internal Auto-zero Circuitry
Dual Supply +/- 5 Volts
Serial I/O Interface
Low Operating Power (typ. 60 mW)
Power Down Stand by Mode (typ. 3 mW)
16 Pin Dual in Line Package (3054/3057)
TTL and CMOS Compatible Digital Interface
Automatic Power Down
Meets or Exceeds BELL/CCITT Specifications
Compatible with TP3052/3053/3054/3057
Precision Voltage Reference

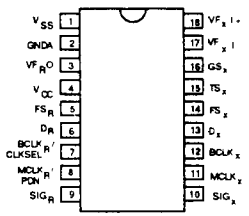
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{SS}/V_{DD}	+/- 7 Volts
Storage Temperature Range	-65° C to 150° C
Voltage at any pin	V_{SS}-.3 < V_{IN} < V_{DD} +.3

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T3052/53/54/57CP	Plastic DIP	0° C to +70° C
XR-T3052/53/54/57IP	Plastic DIP	-40°C to +85°C
XR-T3052/57CJ	PLCC	0° C to +70° C
XR-T3052/57IJ	PLCC	-40°C to +85°C
XR-T3052/53/54/57CN	Ceramic DIP	0°C to +70°C
XR-T3052/53/54/57IN	Ceramic DIP	-40°C to +85°C

PIN ASSIGNMENT



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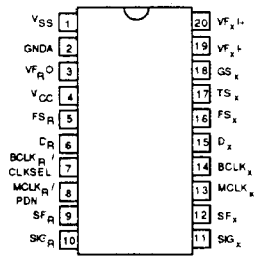

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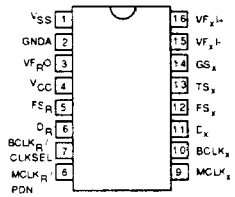

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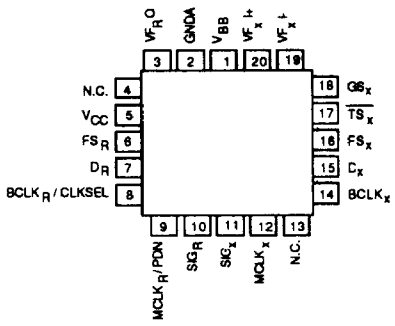

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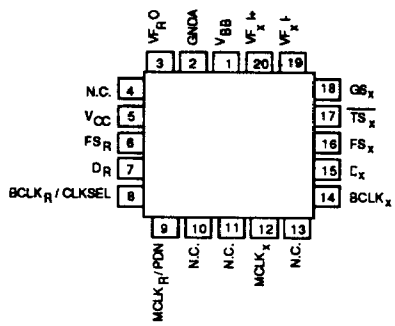

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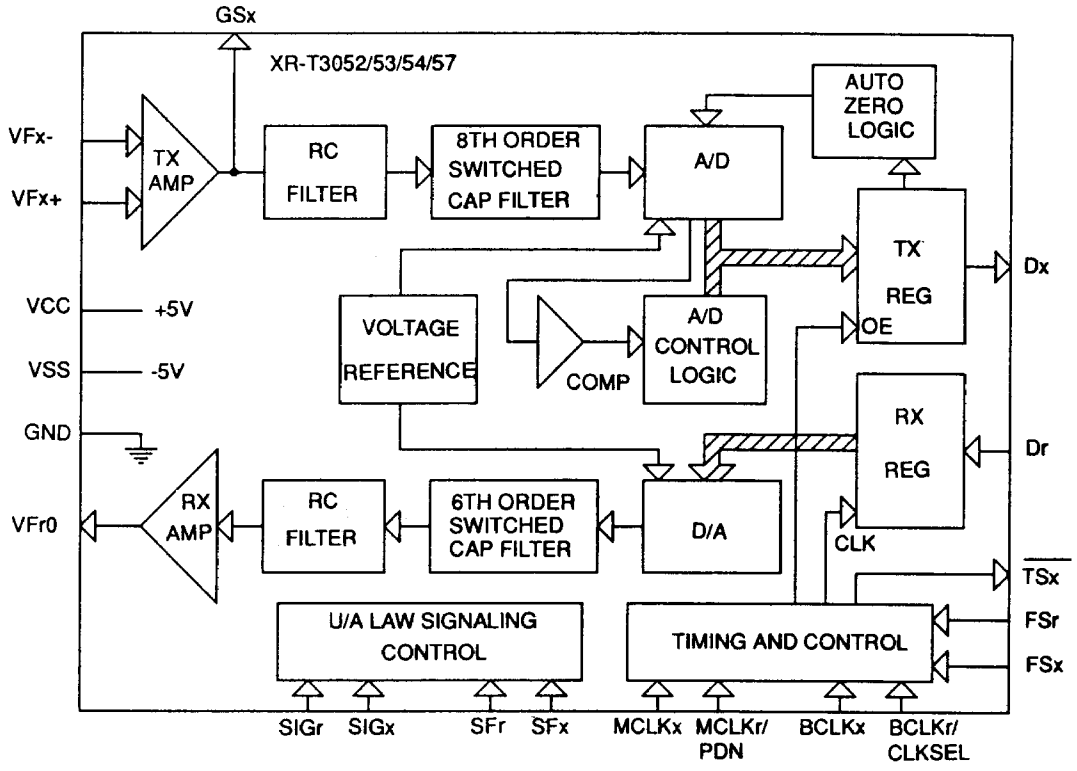

PIN DESCRIPTION

	DESCRIPTION
VSS	**Negative Power Supply** pin. V_{SS} = -5V +/-5%.
GNDA	**Analog Ground**, all signals are referenced to this pin.
VFrO	**Analog Output** of the receive power amplifier.
VDD	**Positive Power Supply** pin. V_{DD} = +5V +/-5%
FSr	**Receive Frame Sync Pulse** which triggers extraction of PCM data into Dr. FSr is an 8KHz pulse train.
Dr	**Receive PCM Data Input** shifted into Dr following the FSr leading edge.
BCLKr/ CLKSEL	**Receive bit clock** which shifts data into Dr after the FSr leading edge. May vary from 64 KHz to 2.048 MHz. This pin can be selected as a master clock input for 1.536 MHz/1.544 MHz or 2.048 MHz. In the synchronous mode BCLKx is used for both receive and transmit directions.(See Table 1)
MCLKr/ PDN	**Receive Masterclock/ Powerdown.** This input must be a 1.536 MHz, 1.544 or 2.048 MHz clock which may be asynchronous with MCLKx but offers best performance when in the synchronous mode. If MCLKr is connected low, MCLKx is selected for all internal timing. If MCLKr is connected high the device is powered down.
SFr	**Receive Signaling Frame** When high during FSr, this input indicates a receive signal frame.

SYMBOL	DESCRIPTION
SIGr	**Receive Signaling Output** The eighth bit of the PCM data appears at this output after each receive signaling frame.
SIGx	**Transmit Signaling Input.** Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SFx	**Transmit Signaling Frame** When high during FSx, this input indicates a transmit signaling frame.
MCLKx	**Transmit Masterclock** Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with MCLKr but offers best performance when in the synchronous mode.
BCLKx	**Transmit Bit Clock** which shifts out the PCM data on Dx. May vary from 64 KHz to 2.048 MHz.
Dx	**Transmit PCM Data Output** The three state PCM data output which is enabled by FSx.
FSx	**Transmit Frame Sync Pulse** input which enables BCLKx to shift out the PCM data on Dx. FSx is an 8 KHz pulse train. (See Figure 1 and 2)
TSx~	**Time Slot Output.** Open drain which pulses low during the encoded time slot.
GSx	**Transmit Amplifier Output** Used to set the gain of the transmit input amplifier.
VFxI-	**Inverting Input** of the transmit input amplifier.
VFxI+	**Non Inverting Input** of the transmit input amplifier.

DC ELECTRICAL CHARACTERISTICS:

Unless specified otherwise the following characteristics are guaranteed from T_A = -40°C to +85°C, V_{CC} = +5V ± 5%, V_{SS} = -5V ± 5%.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	Dx,IL = 3.2mA
				0.4	V	SIGr,IL = 3.2mA
				0.4	V	TSx,IL = 3.2mA (open drain)
V_{OH}	Output High Voltage	2.4			V	Dx,IH = -3.2mA
		2.4			V	SIGr,IH = -3.2mA
I_{IL}	Input Low Current	-10		+10	µA	GNDA≤VIN≤VIL
I_{IH}	Input High Current	-10		+10	µA	VIH≤VIN≤VCC
I_{OZ}	Output Current (High Z State)	-10		+10	µA	Dx,GNDA≤VO≤ VCC
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_{IXA}	Input Leakage Current	-200		+200	nA	-2.5V≤V≤+2.5V VFx+ or VFx-
R_{IXA}	Input Resistance	10			MΩ	-2.5V≤V≤+2.5V VFx+ or VFx-
R_{oXA}	Output Resistance		1	3	Ω	Closed loop
R_{lXA}	Load Resistance	10			KΩ	GSx
C_{lXA}	Load Capacitance			50	pF	GSx
V_{oXA}	Dynamic Range out	-2.8		+2.8	V	GSx,R_L≥10K
A_{vXA}	Voltage Gain	5000			V/V	VFx+ to GSx
F_{uXA}	Bandwidth (unity)	1	2		MHz	
V_{osXA}	Offset Voltage	-20		+20	mV	
V_{cmXA}	Common Mode Voltage	-2.5		+2.5	V	CMRRXA > 60db
CMRRXA	Rejection Ratio CM	60			dB	DC Test
PSRRXA	Rejection Ratio PS	60			dB	DC Test
ANALOG INTERFACE WITH RECEIVE FILTER						
R_{lRF}	Output Resistance		1	3	Ω	Pin VFrO
R_{lRF}	Load Resistance	600			Ω	VFrO = +/-2.5V
C_{lRF}	Load Capacitance			500	pF	
V_{OSrO}	Output DC Offset	-200		+200	mV	
POWER DISSIPATION						
I_{CC0}	Power Down Current		0.5	1.5	mA	No Load
I_{BB0}	Power Down Current		0.05	0.3	mA	No Load
I_{CC1}	Power Active Current		6.0	9.0	mA	No Load
I_{BB1}	Power Active Current		6.0	9.0	mA	No Load

TRANSMISSION CHARACTERISTICS

Unless specified otherwise the following characteristics are guaranteed from TA = -40°C to +85°C, V_{DD} = +5V ± 5%, V_{SS} = -5V ± 5%.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
	Absolute Levels		1.227		Vrms	0 dbm 0 = 4dbm
t_{MAX}	Max Overload Level		2.501		Vpk	XR-T3052/53/54
G_{XA}	Transmit Gain Absolute	-0.15		+0.15	db	XR-T3052/53/54/57 GSx = 0 dbm0 @ 1020Hz
G_{XR}	Transmit Gain Relative to GXA			-40	db	f = 16Hz
				-30	db	f = 50Hz
				-22	db	f = 60Hz
		-1.8		+0.15	db	f = 200Hz
		-0.15		+0.15	db	f = 300Hz to 3000Hz
		-0.35		+0.05	db	f = 3300Hz
		-0.7		0	db	f = 3400Hz
				-14	db	f = 4000Hz
				-32	db	f = 4600Hz and up
G_{XAT}	Transmit Gain Variations with Temperature	-0.1		+0.1	db	Relative to GXA
G_{XAV}	Absolute Gain Variations with Supply Voltage	-0.05		+0.05	db	Relative to GXA
G_{XRL}	Transmit Gain Variation with Level	-0.2		+0.2	db	VFx+ = -40 to +3dbm0
		-0.4		+0.4	db	VFx+ = -50 to -40dbm0
		-1.2		+1.2	db	VFx+ = -55 to -50dbm0 Sinusoidal Test
G_{RA}	Receive Gain, Absolute	-0.15		+0.15	db	Digital Code Input at 1020Hz @ 0dbm0
G_{RR}	Receive Gain, Relative to GRA	-0.15		+0.15	db	f = 0 to 3000Hz
		-0.35		+0.05	db	f = 3300Hz
		-0.7		0	db	f = 3400Hz
				-14	db	f = 4000Hz
G_{RAT}	Absolute Gain Variation (Receiver) over Temperature	-0.1		+0.1	db	Relative to GRA
G_{RAV}	Absolute Gain Variation (Receiver) over Supply Voltage	-0.05		+0.05	db	Relative to GRA
G_{RRL}	Receive Gain Variation with Level	-0.2		+0.2	db	-40 to 3dbm0
		-0.4		0.4	db	-50 to 3dbm0
		-1.2		1.2		-55 to -50dbm0 Sinusodial test method
V_{RO}	Receive Output Drive	-2.5		+2.5	V	Rl = 600Ω
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay (Abs)		290	315	µsec	f = 1600Hz
D_{XR}	Transmit Delay (Relative to DXA)		195	220	µsec	f = 500 to 600Hz
			120	145	µsec	f = 600 to 800Hz
			50	75	µsec	f = 800 to 1000Hz
			20	40	µsec	f = 1000 to 1600Hz
			55	75	µsec	f = 1600 to 2600Hz
			80	105	µsec	f = 2600 to 2800Hz
			130	155	µsec	f = 2800 to 3000Hz
D_{RA}	Receive Delay (Abs)		180	200	µsec	f = 1600Hz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DRR	Receive Delay Relative to DRA	-40 -30	-25 -20		µsec µsec	f = 500 to 1000Hz f = 1000 to 1600Hz
			70	90	µsec	f = 1600 to 2600Hz
			100	125	µsec	f = 2600 to 2600Hz
			145	175	µsec	f = 2800 to 3000 Hz
NOISE						
N_{XC}	Transmit Noise C Message Weighted		12	15	dbmCO	XR-T3052/53/54
N_{XP}	Transmit Noise P Message Weighted		-74	-67	dbmCO	XR-T3057
N_{RC}	Receive Noise C Message Weighted		8	11	dbmOP	XR-T3052/53/54 PCM Code
N_{RP}	Receive Noise P Message Weighted		-82	-79	dbmOP	XR-T3057
N_{RS}	Noise, Single Frequency			-53	dbmO	f = 0 to 100KHz VFx+ = 0Vrms
PPSRx	Positive Power Supply Rejection, Transmit	40			dbC	VFx+ = -50dbm0 V_{CC} = 5Vdc+ 100mVrms, f = 0 to 50KHz
NPSRx	Negative Power Supply Rejection Transmit	40			dbC	VFx+ = -50dbm0, Vee = -5Vdc+100mV, f = 0 to 50KHz
PPSRr	Positive Power Supply Rejection,	40			dbC	f = 0 to 4000Hz
	Receive	40			db	f = 4KHz to 25KHz
		36			db	f = 25KHz to 50KHz
NPSRr	Negative Power Supply Rejection	40			dbC	f = 0 to 4000Hz
	Receive	40			db	f = 4KHz to 25KHz
		36			db	f = 25KHz to 50KHz
SOS	Spurious Out-of-band Signals at the Channel Output			-30	db	0 dbm0, 300Hz to 3400Hz, Input = Dr, Loop Around Measurement
				-30	db	f = 4600 to 7600Hz
				-40	db	f = 7600 to 8400Hz
				-30	db	f = 8.4 to 100KHz
DISTORTION						
STDx	Signal/Distortion	33			dbC	3 db level
STDr	Transmit or Receive Half Channel	36			dbC	0 to -30db level
		29			dbC	-40dbm0 (XMT)
		20			dbC	-40dbm0 (RCV)
		14			dbC	-55dbm0 (XMT)
		15			dbC	-55dbm0 (RCV)
SFDx	Single Frequency Distortion, Transmit			-46	db	
SFDr	Single Frequency Distortion, Receive			-46	db	
IMD	Intermodulation Distortion			-41	db	VFx+ = -4 to 21dbm0, 300Hz< f<3400Hz

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CROSSTALK						
CTx-r	Transmit To Receive Crosstalk, Level = 0dbm		-90	-75	db	f=300 to 3400Hz Dr = Quiet dbm Code
CTr-x	Receive to Transmit Crosstalk, Level = 0dbm		-90	-70	db	f=300 to 3400Hz VFx = Multitone

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AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25° C, V_{SS} =-5V+/-5%, V_{DD} = 5V+/-5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
$1/t_{PM}$	Master Clock Frequency		1.536		MHz	See Table 1
			1.544		MHz	
			2.048		MHz	
t_{WMH}	Width (MCLK High)	160			ns	MCLKx, MCLKr
t_{WML}	Width (MCLK Low)	160			ns	MCLKx, MCLKr
(t_{SBFM})	Set-Up Time BCLK high to MCLK low	100			ns	Bit after FSx edge
t_{WBH}	Bit Clock Width	160			ns	VIH = 2.2V
t_{WBL}	Bit Clock Low	160			ns	VIL = 0.6V
t_{HBFL}	Hold Time (Bit Clock Low to FS)	0			ns	Long Frame Only
t_{HBFS}	Hold Time (Bit Clock High to FS)	0			ns	Short Frame Only
t_{SFB}	Set Up Time (FS to Bit Clock Low)	80			ns	Long Frame Only
t_{DBD}	Delay (BCLK high to Data Valid)	0	140		ns	Load = 150pF
t_{DBTS}	Delay (to TSx low)	140			ns	Load = 150pF
t_{DZC}	Delay (BCLKx low- Data Out Disabled)	50		165	ns	C = 0 to 150pF
					ns	
t_{DZF}	Delay (Data Valid from FSx or BCLKx	20		165	ns	C = 0 to 150pF
t_{SSFF}	Set-Up (SFx/r to high to FSx/r)	60			ns	XR-T3053
t_{SSFB}	Set-Up (SF Sync to high to BCLKx/r	60			ns	XR-T3053
t_{SSGB}	Set-Up (SIGx to BCLKx)	100			ns	XR-T3052 & XR-T3053
t_{HBSG}	Hold Time (BCLK high to SIGx)	50			ns	XR-T3052 & XR-T3053
t_{SDB}	Set-Up (Dr valid to BCLKr/x low)	50			ns	
t_{HBD}	Hold Time (BCLKr/x low to Dr valid)	50			ns	
t_{HBSF}	Hold Time (BCLKx/r low to SF Sync)	100			ns	XR-T3053
t_{SF}	Set-Up Time (FSx/r to BCLKx/r low)	50			ns	Short Frame Sync Pulse
t_{HF}	Hold Time (BCLKx/r low to FSx/r low)	100			ns	Short Frame Sync Pulse
t_{HBFI}	Hold Time (Bit CLK 3rd Period to FSr or FSx)	100			ns	Long Frame Sync Pulse
t_{WFL}	Minimum Width of Frame Sync Pulse	160			ns	64Bit/sec
t_{RM}	Rise Time of MCLK	50			ns	MCLKr,MCLKx
t_{FM}	Fall Time of MCLK	50			ns	MCLKr,MCLKx
t_{PB}	Bit Clock Period	485	488	15725	ns	

ENCODING FORMAT		
	T3052/3053/3054	XR-T3057
V IN (at GSX) = +Full Scale	10000000	10101010
V IN (at GSX) = 0V	11111111	11010101
	01111111	01010101
V IN (at GSX) = -Full Scale	00000000	00101010

SYSTEM DESCRIPTION

The XR-T3052/53/54/57 consist of two major blocks; the COder or the transmit section and the DECoder or the receive section plus timing and control sections.

TRANSMITTER/RECEIVER SECTION

The encoder portion of each device consists of an input gain adjust amplifier with provisions for gain adjustment using two external resistors to set the required gain. This amplifier stage allows amplification of the audio signals in excess of 20 db across the audio passband with satisfactory low noise and wide bandwidth. The output of the amplifier drives a distributed RC network, followed by an eighth order switched capacitor band pass filter. The resulting band-pass characteristics meet the G.712 specifications. The sample and hold circuit follows this band pass filter and passes the sampled information to the analog to digital encoder. The circuitry used for coding and encoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and resistors to define steps. These steps are predefined according to U-law (XR-T3052/53/54) or A-law (XR-T3057) coding conventions. The frame sync pulse (FSx) is needed to control the sampling of the filter output, and start each encoding cycle. The 8-bit codes are then loaded into a buffer and shifted out through Dx at the next FSx pulse. The DC offset cancellation is achieved with an autozero logic circuitry which operates by integrating the sign bit of the PCM data and feeding it back to the noninverting input of the comparator.

The decode portion of each device consist of an expanding decoder, which reconstructs the analog signal from the companded U-law (XR-T3052/53/54) or A-law (XR-T3057) code. The output of this section drives a sixth order low pass filter, and is used to correct for the sinx/x response of the decoder output. The outputpower amplifier is capable of driving a 600 ohm load to a level of 7.2 dbm. Upon the occurrence of FSr, the data at the Dr input is clocked in on the falling edge of the next eight BCLKr periods. At the end of the decoder time slot, the decoding cycle begins, and the decoder digital to analog circuit output is updated.

SYNCHRONOUS/ASYNCHRONOUS OPERATION

In a synchronous operation, the same bit clock should be used for both transmitter and receiver. A bit clock must be applied to BCLKx and BCLKr/CLKSEL can be used to select the proper internal divider for a masterclock of 1.536 MHz, 1.544 MHz or 2.048 MHz as shown in table 1. If 1.544 MHz clock is supplied, the device automatically compensates for the 193rd framing bit pulse. BCLKx may vary from 64 KHz to 2.048 MHz. The FSx pulse starts the encoding cycle and it also enables the Dx output to shift out the previously encoded PCM bits on the positive edge of BCLKx. The tri-state Dx output then returns to a high impedance state. On the receive side PCM data from Dr is latched on the negative edge of BCLKx with an FSr pulse.

For asynchronous operation, separate transmit and receive clocks may be applied. Applying only static logic levels to the MCLKr/PDN pin will automatically connect MCLKx to all internal MCLKr functions. FSx starts each encoding cycle and must be synchronous with BCLKx. In the asynchronous mode the logic levels shown in table 1 do not apply anymore, but the bit clocks (BCLKr and BCLKx) may still operate from 64 KHz to 2.048 MHz. The FSr pulse starts each decoding cycle and must be synchronous with BCLKr.

	Master Clock Frequency Selected	
BCLKR/CLKSEL	TP3057	TP3052 TP3053 TP3054
Clocked	2.048MHz	1.536MHz or 1.544 MHz
0	1.536MHz or 1.544MHz	2.048MHz
1 (or Open Circuit)	2.048MHz	1.536MHz or 1.544MHz

Table 1. Selection of Master Clock Frequencies

FRAME SYNCHRONIZATION

The XR-T3052/53/54/57 can utilize either a short or long frame sync pulse. Upon power initialization, the device will be set to short frame mode. In this mode both FSx and FSr must be one bit clock period long. With FSx high during a falling edge of BCLKx, the next rising edge of BCLKx enables the Dx output. With FSr high during a falling edge of BCLKr, the next falling edge of BCLKr latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

To use long sync frame mode, FSx or FSr, must be three or more bit clock periods long. Based on the transmit frame sync pulse (FSx), the XR-T3052/53/54/57 will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx three state output buffer is enabled with the rising edge of FSx or the rising edge of BCLKx, whichever comes later, and the first bit clocked out is the sign bit. The following seven bits will be clocked out on next rising edge of the BCLKx. The Dx output is disabled by the falling BCLKx edge following the eight rising edges, or by FSx going low, whichever comes later. A rising edge on the receive frame sync pulse, FSr will cause the PCM data at Dr to be latched in on the next eight falling edges of BCLKr (BCLKx in the synchronous mode. The long frame sync pulse may be utilized in both, the synchronous and asynchronous mode.

SIGNALING

The XR-T3052 is a U-law CODEC intended to be used for short frame sync applications and be able to insert and extract signaling from the PCM data stream.

The XR-T3053 has the same characteristics as the XR-T3052 except it can be used for short and long frame sync pulses.

The XR-T3054 is also U-law but has no provisions for signaling.

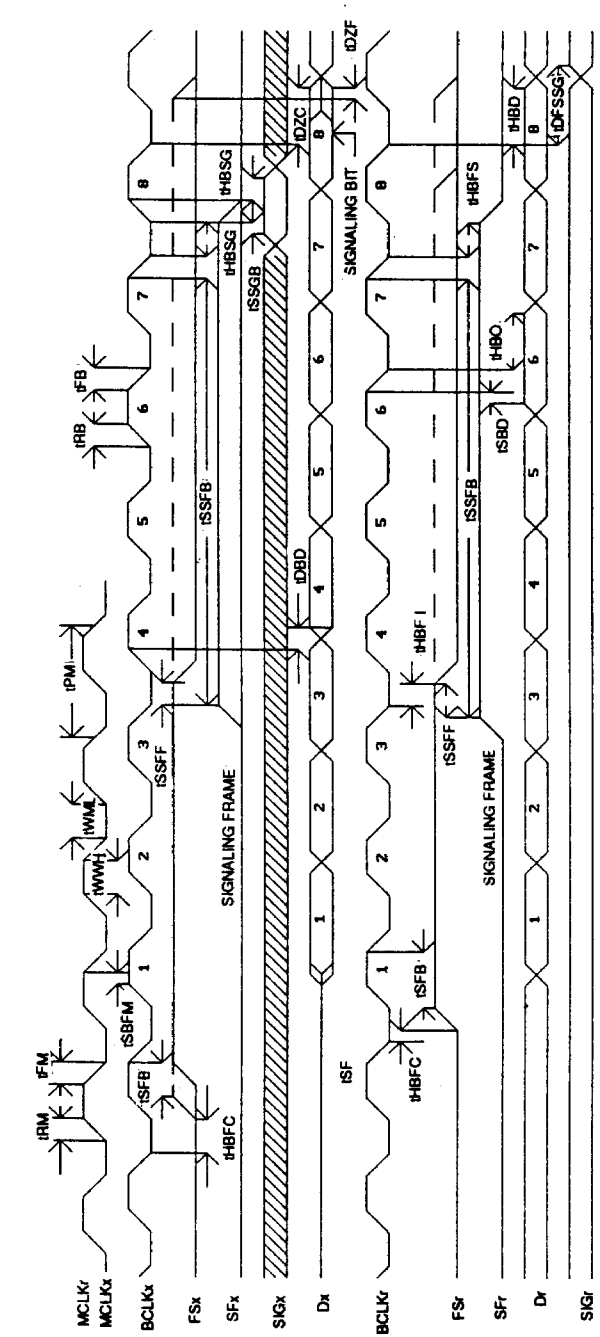
The XR-T3057 uses A-law companding technique and has no provisions for signaling.

Signaling is accomplished by insertion of the data present on the SIGx input, whenever a frame sync pulse (two bits long) is present. The signaling data is inserted LSB in the PCM data transmitted during that frame. Similar, with a FSr two bit clock periods long, the LSB of the PCM data read into the Dr input will be latched and appear on the SIGr output pin until updated following the next signaling frame.

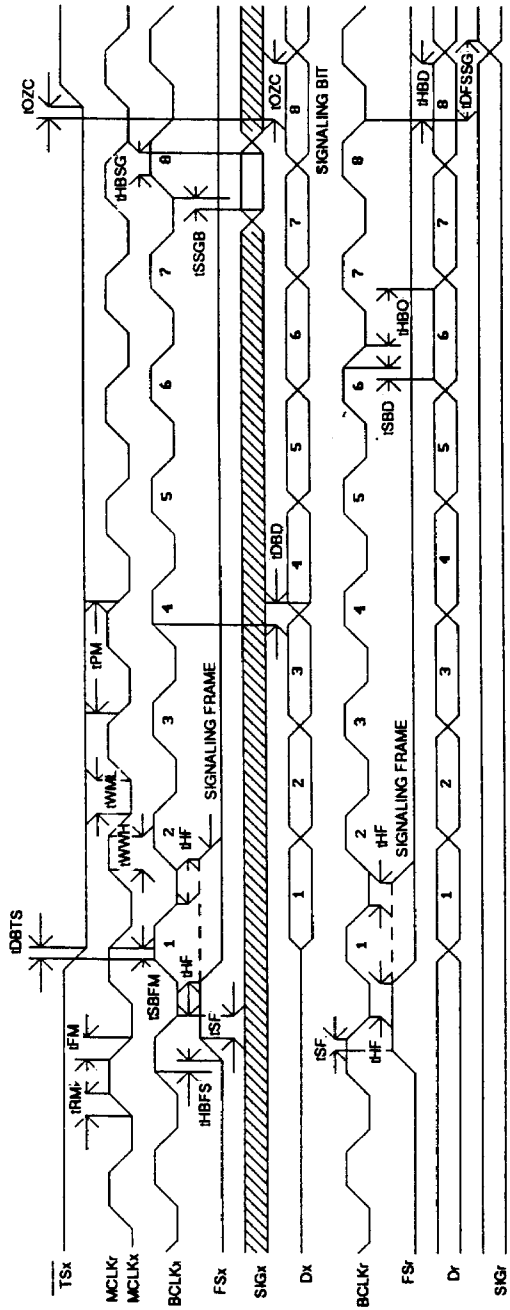
The short frame signaling may also be implemented using the XR-T3053, providing SFr and SFx are left open circuit or tied to ground. As mentioned prior, the XR-T3052 can not insert or extract signaling information in the long frame mode, while the XR-T3053 can in both modes. In the long framing mode, two additional frame sync pulses are required (SFx and SFr), which indicate the respective transmit and receive signaling frames. Operation is such, that the data present at the SIGx input will be inserted as the LSB into the PCM data transmitted during that frame. Similar, with a signaling frame sync (SFr), the LSB of the PCM data is latched at Dr and will appear on the SIGr output pin until the next signaling frame.

POWER UP

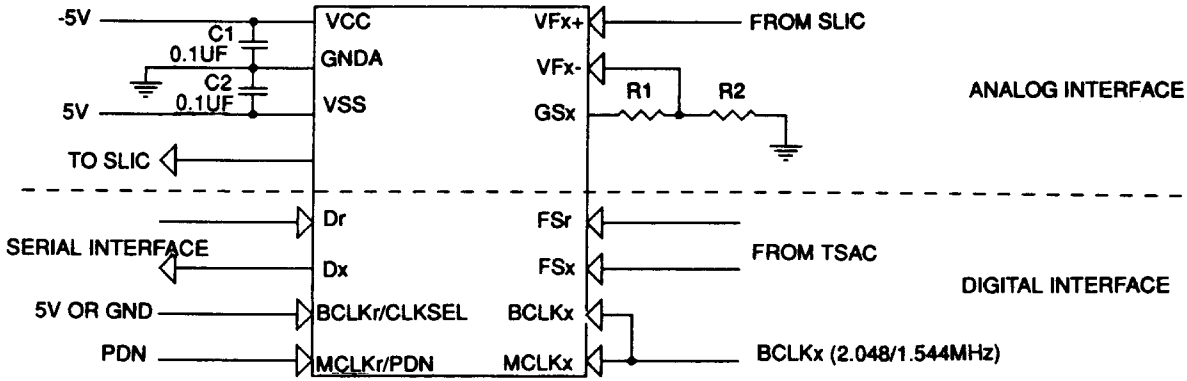
Initially, at power-up the COMBO is put into a power down state.This way all essential circuits are deactivated and the Dx and VFro outputs are put into a high impedance state. To activate the device [a logical low level or clock (MCLKr/PDN)] and [FSx or FSr pulses] need to be present. Note now that two different power-down control modes are available. One, to put MCLKr/PDN pin into a high state, and second, to keep both (FSr and FSx) continuously low. The approximate power-down delay after the last FSx or FSr pulse is 2msec. The first FSx or FSr pulse powers the device up but keeps the Dx output drive in a high impedance state until the next FSx pulse.



LONG FRAME SYNC TIMING



SHORT FRAME SYNC TIMING



Note: 1) Xmit Gain = 20 Log (R1 + R2) / R2 where (R1 + R2) > 10Kohm
2) C1 & C2 need to be connected as close as possible to the device for proper operation.

TYPICAL SYNCHRONOUS APPLICATION CIRCUIT FOR THE XR-T3052/53/54/57