1.1 Scope.

This specification covers the detail requirements for a complete monolithic 12-bit, 1.25 Msps A/D converter with an on-chip, high performance sample-and-hold amplifier (SHA) and voltage reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD1671SQ/883B

1.2.3 Case Outline.

See outline dimension drawing for package outline:

Package	Description
Q-28	28-Pin Cerdip

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to ACOM ..... −0.5 V to +6.5 V
V_{EE} to ACOM ..... −6.5 V to +0.5 V
V_{LOGIC} to DCOM ..... −0.5 V to +6.5 V
ACOM to DCOM ..... −1 V to +1 V
V_{CC} to V_{LOGIC} ..... −6.5 V to +6.5 V
ENCODE to DCOM ..... −0.5 V to V_{LOGIC} + 0.5 V
REF IN, BPO/UPO to ACOM ..... −0.5 V to V_{CC} + 0.5 V
AIN to ACOM ..... −11 V to +11 V
Power Dissipation ..... 1000 mW
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

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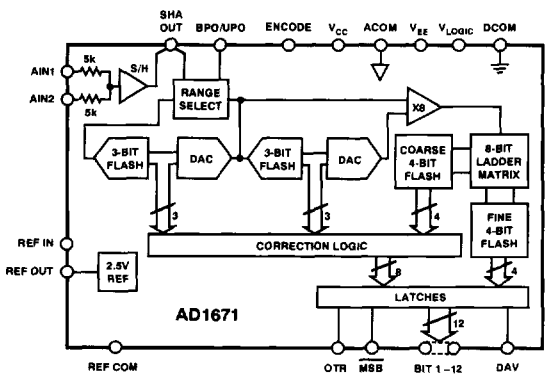
Table 1.

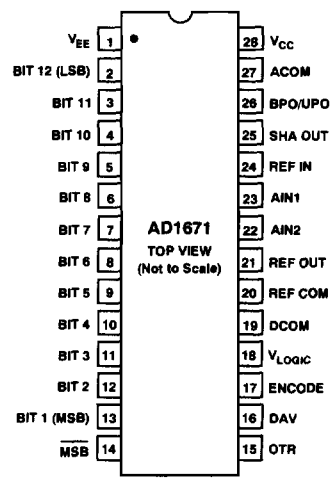
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition	Units
Resolution	RES	1	12	12	12		Bits
Integral Nonlinearity	INL	1	2.5	2.5	3	All Codes Histogram	±LSB
Differential Nonlinearity	DNL	1	11	11	11	All Codes Histogram	Bits
Unipolar Offset Error	V_{OSE}	1	9	9		2.5 V, 5 V Span	±LSB
Unipolar Offset Drift	TC_{VOS}	1			25	2.5 V, 5 V Span	±ppm/°C
Gain Error	A_E	1	0.37	0.37		Unipolar & Bipolar	% FSR
Gain Drift	TC_A	1			40	Unipolar & Bipolar	±ppm/°C
Bipolar Zero Error	B_{POE}	1	10	10		2.5 V, 5 V Span	±LSB
Bipolar Zero Drift	TC_{BPO}	1			30	2.5 V, 5 V Span	±ppm/°C
Analog Input Ranges	V_{IN}	1	2.5	2.5	2.5	Unipolar Mode	Volts
			5	5	5		
			2.5	2.5	2.5	Bipolar Mode	±Volts
			5	5	5		
Input Resistance	$R_{IN2.5}$	1	10			2.5 V Range	MΩ
	R_{IN5}		10			5 V Range	kΩ
Input Capacitance	C_{IN}	1	10				pF
Reference Voltage	V_{RO}	1	2.5			Unipolar & Bipolar	V
Reference Error	V_{ROE}	1		25		Unipolar & Bipolar	±mV
Reference Drift	TC_{VRO}	1			30	Unipolar & Bipolar	±ppm/°C
Reference Current	I_{REF}	1	2.5			Unipolar Mode	mA
			1			Bipolar Mode	mA
Power Dissipation	P_D	1	750	750	750	V_{CC}, V_{EE} = ±5.25 V	mW
Power Supply Current	I_{CC}	1	68	68	68	Tested Under Static Conditions	+mA max
	I_{EE}	1	68	68	68		−mA max
	I_{DD}	1	5	5	5		+mA max
Operating Voltage Range	V_{CC}	1	4.75				V min
			5.25				V max
	V_{EE}	1	4.75				−V max
			5.25				−V min
	V_{DD}	1	4.5				V min
			5.5				V max
PSRR	V_{CC}	1	5	5	5	Full-Scale Change Measured	±LSB
	V_{EE}		5	5	5		
	V_{DD}		5	5	5		
Input Logic Levels	V_{IH}	1	2	2	2	Encode Input	V min
	V_{IL}		0.8	0.8	0.8		V max
Input Logic Currents	I_{IH}	1	10	10	10		±μA
	I_{IL}		10	10	10		
Logic Outputs	V_{OH}	1	2.4	2.4	2.4	I_{OH} = 500 μA	V min
	V_{OL}		0.4	0.4	0.4	I_{OL} = 1.6 mA	V max
	I_{OH}		500	500	500		μA
	I_{OL}		1.6	1.6	1.6		−mA

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition	Units
Signal-to-Noise Plus Distortion	SINAD	1	68	68	68	f_{IN} = 100 kHz f_S = 1 MHz −0.5 dB Input	dB min
Effective Number of Bits	ENOB	1	11.0				Bits min
Total Harmonic Distortion	THD	1	75	75	75		−dB max
Peak Spurious of Peak Harmonic Component	PS	1	77	77	77		−dB max
Small Signal Bandwidth	bW	1	12				MHz
Full Power Bandwidth	BW	1	2				MHz
Intermodulation Distortion	Σ 2nd	1	75	75	75	2nd Order Products	−dB max
	Σ 3rd	1	75	75	75	3rd Order Products	−dB max

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 9	Sub Group 10, 11	Test Condition	Units
Conversion Time	T_{CONV}	1	800	800	800		ns
Sample Rate		1	1.25	1.25	1.25		MSPS max
Encode Width High (Short Encode)	t_{ENC}	1	20	20	20		ns min
			50	50	50		ns max
Encode Width Low (Long Encode)	t_{ENCL}	1	20	20	20		ns min
DAV Pulse Width	t_{DAV}	1	150	150	150		ns min
			300	300	300		ns max
Encode Falling Edge Delay	t_F	1	0				ns min
Start New Conversion Delay	t_R	1	0				ns min
Data and OTR Delay from DAV Falling Edge	t_{DD}	1	20				ns min
Data and OTR Delay from DAV Rising Edge	t_{SS}	1	20				ns min

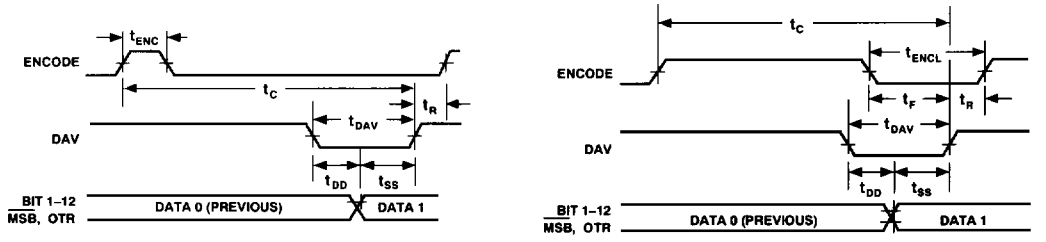
3.2.1 Functional Block Diagram and Terminal Assignments.





3.2.4 Microcircuit Technology Group.

This circuit is covered by technology group (93).



a. Encode Pulse HIGH *b. Encode Pulse LOW*

Figure 1. Timing Diagram

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).