

TERMINAL ASSIGNMENT

CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

High-Voltage Types (20-Volt Rating)

Features:

- Independence of power-supply sequence considerations— V_{CC} can exceed V_{DD} ; input signals can exceed both V_{CC} and V_{DD}
- Up and down level-shifting capability
- Shiftable input threshold for either CMOS or TTL compatibility
- Standardized symmetrical output characteristics
- 100% tested for quiescent current @ 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25° C
- 5 V, 10 V, and 15 V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4504B hex voltage level-shifter consists of six circuits which shift input signals from the V_{CC} logic level to the V_{DD} logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V_{CC} HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504B device is supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead dual-in-line surface-mount plastic packages (M suffix), and in chip form (H suffix).

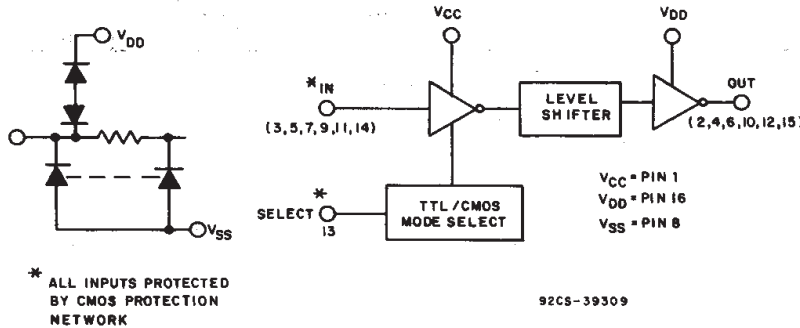


Fig. 1 - Functional diagram for CD4504B.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$: Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR -

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -85°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max $+265^\circ\text{C}$

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CD4504B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{CC} (V)	V _D (V)	-55	-40	+85	+125	+25				
									MIN	TYP	MAX		
Quiescent Device Current, I _{DD} Max and I _{CC} in CMOS-CMOS Mode	—	0,5	5	5	1	1	30	30	—	0.02	1	μA	
	—	0,10	5	10	2	2	60	60	—	0.02	2		
	—	0,15	5	15	4	4	120	120	—	0.02	4		
	—	0,20	5	20	20	20	600	600	—	0.04	20		
Quiescent Device Current, I _{CC} Max TTL-CMOS Mode	—	0,5	5	5	5	5	6	6	—	2.5	5	mA	
	—	0,10	5	10	5	5	6	6	—	2.5	5		
	—	0,15	5	15	5	5	6	6	—	2.5	5		
Output Low (Sink) Current, I _{OL} Min	0.4	0.5	—	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0,10	—	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0,15	—	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I _{OH} Min	4.6	0,5	—	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
	2.5	0,5	—	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0,10	—	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0,15	—	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V _{OL} Max	—	0,5	—	5	0.05				—	0	0.05	V	
	—	0,10	—	10	0.05				—	0	0.05		
	—	0,15	—	15	0.05				—	0	0.05		
Output Voltage: High-Level, V _{OH} Min	—	0,5	—	5	4.95				4.95	5	—	V	
	—	0,10	—	10	9.95				9.95	10	—		
	—	0,15	—	15	14.95				14.95	15	—		
Input Low Voltage, V _{IL} Max Note 1	TTL-CMOS	1	—	5	10	0.8				—	—	0.8	V
	TTL-CMOS	1	—	5	15	0.8				—	—	0.8	
	CMOS-CMOS	1	—	5	10	1.5				—	—	1.5	
	CMOS-CMOS	1.5	—	5	15	1.5				—	—	1.5	
	CMOS-CMOS	1.5	—	10	15	3				—	—	3	
Input High Voltage, V _{IH} Min Note 1	TTL-CMOS	9	—	5	10	2				2	—	—	V
	TTL-CMOS	13.5	—	5	15	2				2	—	—	
	CMOS-CMOS	9	—	5	10	3.5				3.5	—	—	
	CMOS-CMOS	13.5	—	5	15	3.5				3.5	—	—	
	CMOS-CMOS	13.5	—	10	15	7				7	—	—	
Input Current, I _{IN} Max	—	0,18	—	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA	

Note 1: Applies to the 6 input signals. For mode control (P13), only the CMOS-CMOS ratings apply.

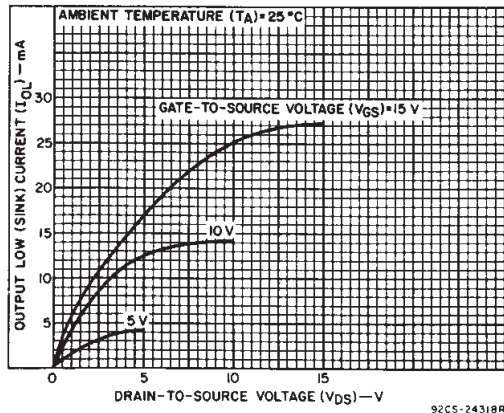


Fig. 2 - Typical output low (sink) current characteristics.

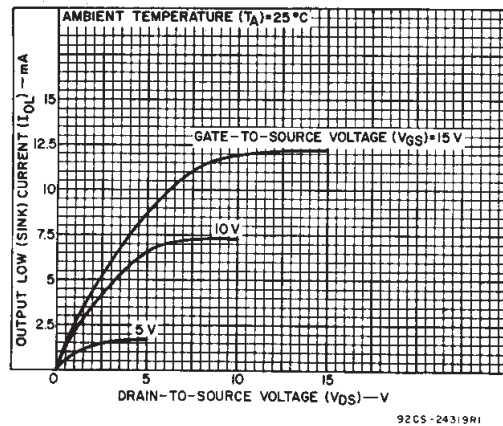


Fig. 3 - Minimum output low (sink) current characteristics.

CD4504B Types

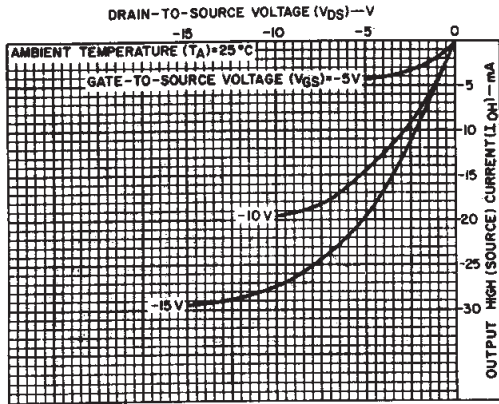


Fig. 4 - Typical output high (source) current characteristics.

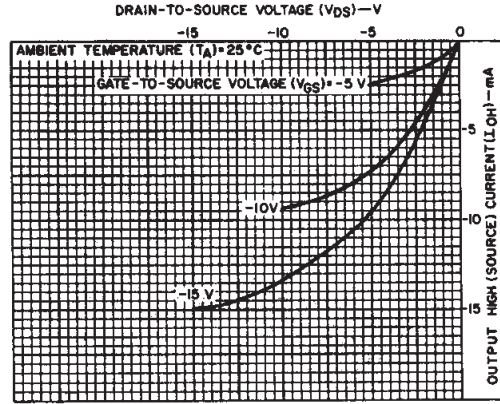


Fig. 5 - Minimum output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)	—	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 Ω

CHARACTERISTIC	SHIFTING MODE	V _{CC} (V)	V _{DD} (V)	LIMITS		UNITS
				TYP.	MAX.	
Propagation Delay: High-to-Low, t _{PHL}	TTL to CMOS V _{DD} > V _{CC}	5	10	140	280	ns
	CMOS to CMOS V _{DD} > V _{CC}	5	10	120	240	
		5	15	120	240	
		10	15	70	140	
	CMOS to CMOS V _{CC} > V _{DD}	10	5	275	550	
		15	5	275	550	
		15	10	70	140	
Low-to-High, t _{PLH}	TTL to CMOS V _{DD} > V _{CC}	5	10	140	280	ns
	CMOS to CMOS V _{DD} > V _{CC}	5	10	120	240	
		5	15	120	240	
		10	15	70	140	
	CMOS to CMOS V _{CC} > V _{DD}	10	5	200	400	
		15	5	200	400	
		15	10	60	120	
Transition Time, t _{THL} , t _{TLH}	All Modes		5	100	200	ns
			10	50	100	
			15	40	80	
Input Capacitance, C _{IN}	Any Input			5	7.5	pF

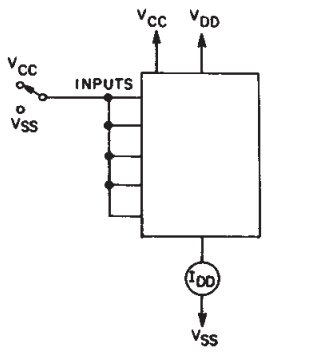


Fig. 6 - Quiescent device current.

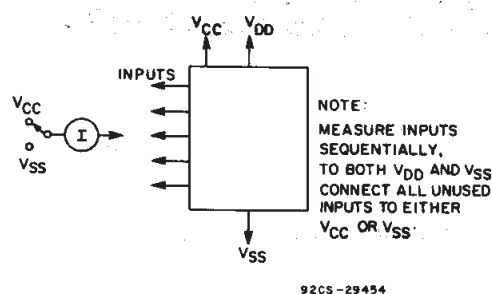


Fig. 7 - Input current.

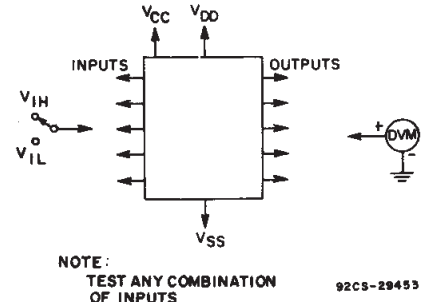


Fig. 8 - Input voltage.

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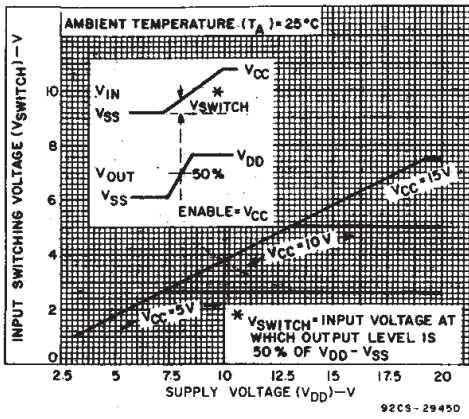


Fig. 9 - Typical input switching as a function of high-level supply voltage. (SELECT at V_{CC} -CMOS mode).

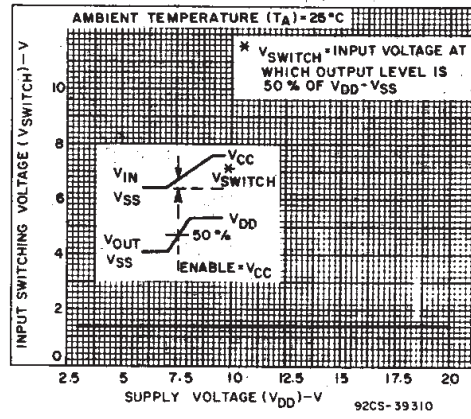


Fig. 10 - Typical input switching as a function of high-level supply voltage (SELECT at V_{SS} -TTL mode).

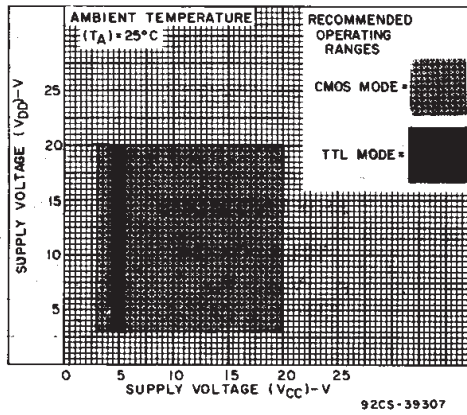
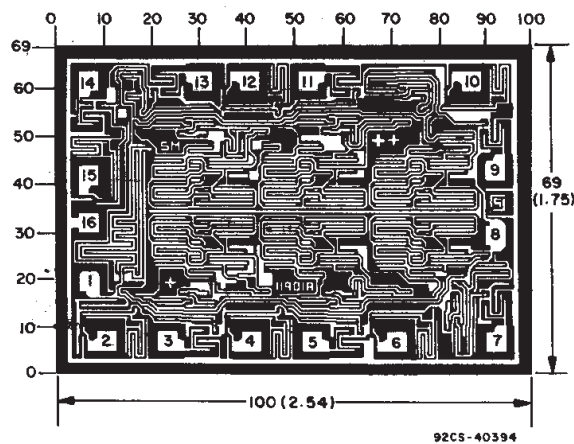


Fig. 11 - High-level supply voltage vs. low-level supply voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4504BH.

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| [APPLICATION NOTES](#) | [USER GUIDES](#) | [MORE LITERATURE](#)

CD4504B, CMOS Hex Voltage-Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

DEVICE STATUS: **ACTIVE**

PARAMETER NAME CD4504B

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [cd4504b.pdf](#) (219 KB) (Updated: 11/20/1998)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics](#) (SCHA004 - Updated: 12/03/2001)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)

- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4504BE	PDIP (N)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4504BM96	SOIC (D)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4504BPWR	TSSOP (PW)	16	-55 TO 125	ACTIVE		View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION Updated Daily								TI INVENTORY STATUS As Of 08:00 AM GMT, 17 Apr 2003			REPORTED DISTRIBUTOR INVENTORY As Of 08:00 AM GMT, 17 Apr 2003		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
CD4504BE	ACTIVE	PDIP (N) 16	-55 TO 125		View Contents	1KU 0.44	25	<u>8000*</u>	>10k 10 Jun	4 WKS	Avnet Americas	>1k	BUY NOW
											DigiKey Americas	>1k	BUY NOW
											Newark Electronics Americas	552	BUY NOW
											Avnet-SILICA Europe	54	BUY NOW
CD4504BF3A	ACTIVE	CDIP (J) 16	-55 TO 125		View Contents	1KU 3.53	1	<u>1788*</u>	3971 20 May	8 WKS	EBV Electronik Europe	50	BUY NOW
											Avnet-SILICA Europe	19	BUY NOW
CD4504BM	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.88	40	<u>0*</u>	31 28 Apr	4 WKS	Insight Americas	80	BUY NOW
									>10k 13 May				
CD4504BM96	ACTIVE	SOIC (D) 16	-55 TO 125		View Contents	1KU 0.88	2500	<u>0*</u>	>10k 13 May	4 WKS	DigiKey Americas	>1k	BUY NOW
CD4504BNSR	OBSOLETE	SOP (NS) 16	-55 TO 125		View Contents	1KU		<u>0*</u>		Call**	None Reported View Distributors		
CD4504BPW	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.56	90	<u>0*</u>	1620 16 Apr	4 WKS	None Reported View Distributors		
									>10k 08 May				
CD4504BPWR	ACTIVE	TSSOP (PW) 16	-55 TO 125		View Contents	1KU 0.28	2000	<u>0*</u>	>10k 08 May	4 WKS	DigiKey Americas	>1k	BUY NOW

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