

DM74AS645 TRI-STATE® Octal Bus Transceiver

General Description

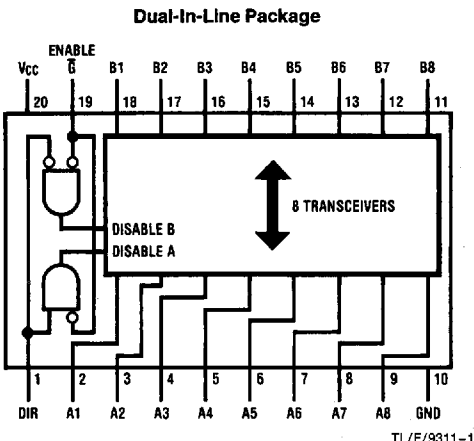
This advanced Schottky device contains 8 pairs of TRI-STATE logic elements configured as an octal bus transceiver. This circuit is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. This device transmits data from the A bus to the B bus, or vice versa, depending upon the logic level of the direction control input (DIR). The enable input (\bar{G}) can be used to disable the devices, effecting isolation of buses A and B.

The TRI-STATE circuitry also contains a protection feature that prevents these transceivers from glitching the bus during power-up or power-down.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance drive to drive terminated transmission lines to 133Ω
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

Connection Diagram



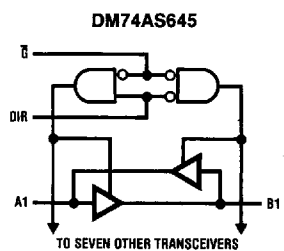
Top View

Order Number DM74AS645WM or DM74AS645N
See NS Package Number M20B or N20A

Function Table

Control Inputs		Operation
\bar{G}	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

Logic Diagram



TL/F/9311-2

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Typical θ_{JA}	
N Package	51.5°C/W
M Package	69.0°C/W

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			-15	mA
I_{OL}	Low Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74AS645 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5\text{V to } 5.5\text{V}, I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$			V
		$V_{CC} = 4.5\text{V}, I_{OH} = -3 \text{ mA}$	2.4			V
		$V_{CC} = 4.5\text{V}, I_{OH} = \text{Max}$	2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$		0.35	0.55	V
I_I	Input Current at Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7\text{V},$ $(V_I = 5.5\text{V for A or B Ports})$			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V (Note 2)}$	Control Inputs		20	μA
			A or B Ports		70	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max},$ $V_I = 0.4\text{V (Note 2)}$	Control Inputs		-0.5	mA
			A or B Ports		-0.75	
I_O	Output Drive Current	$V_{CC} = \text{Max}, V_O = 2.25\text{V}$	-50		-150	mA
I_{CCH}	Supply Current with Outputs High	$V_{CC} = \text{Max}$		62	97	mA
I_{CCL}	Supply Current with Outputs Low			95	149	mA
I_{CC}	Supply Current with Outputs in TRI-STATE			79	123	mA

Note 1: All typicals are at $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$.

Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current, I_{OZH} and I_{OZL} .

Switching Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Note 1)

Symbol	Parameter	From (Input)	To (Output)	V _{CC} = Min to Max, C _L = 50 pF, R ₁ = R ₂ = 500Ω		Units
				Min	Max	
t _{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	2	9.5	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A	2	9	ns
t _{PZH}	Output Enable Time to High Level Output	\bar{G}	A or B	2	11	ns
t _{PZL}	Output Enable Time to Low Level Output	\bar{G}	A or B	2	10	ns
t _{PHZ}	Output Disable Time from High Level Output	\bar{G}	A or B	2	7	ns
t _{PLZ}	Output Disable Time from Low Level Output	\bar{G}	A or B	2	12	ns

Note 1: See Section 5 for test waveforms and output load.