# MP8831

## Single 10-Bit ADC with Digitally Controlled References

EXAR ...the analog plus company™

July 1997–1

### FEATURES

- 1.67 MSPS Sampling Rate
- 10 bit ADC with < ± 0.75 LSB DNL
- Independent, Digitally Controlled ADC Offset & Full Scale Adjustments
- ADC Full Scale Range: 0V to 2.82V, with 10-Bit Resolution
- ADC Offset Range: 0.175V to 0.345V, with 6-Bit Resolution
- Update Rate: Pixel-by-pixel
- Single 5V Supply
- Low Power CMOS: 175mW (typ.)
- Power Down Mode: 1.0mW (typ.)
- Latch-up Free
- ESD Protection to over 2000V

### APPLICATIONS

- Precision B/W & Color CCD Scanners
- Digital Copiers
- Digital Cameras
- Infra-Red Image Digitizers

### BENEFITS

- Improved Pixel-to-Pixel Calibration Accuracy Compared to Software Corrections
- Reduced Part Count & System Cost
- Lower Power Consumption & Power Down for Battery Applications

### GENERAL DESCRIPTION

The MP8831 is a 1.67MSPS image digitizing chip that includes a 10-bit A/D Converter with digitally controlled references. This allows imaging systems to calibrate for individual pixel offset and gain errors. The offset can be adjusted from 0.175V to 0.345V in 64 steps (6 bit resolution), while the full scale range (i.e. peak to peak input range) is adjustable up to 2.82V in 1024 steps (10 bit resolution).

The A/D converter uses a subranging architecture to achieve high sample rates and low power consumption. Our patented comparator design performs an on chip track & hold function with a low input capacitance. Our proprietary high speed DAC design is used to drive and update the ADC reference ladder at a 1.67MHz rate.

The MP8831 operates from a single +5V supply and an external 1V reference. Power consumption is typically only 180mW during conversion operation, and less than 1.0mW in power down mode. Specified for operation between -40°C to +85°C, the MP8831 is available in 28 lead SOIC (JEDEC) and PDIP packages.

### ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|---|---|---|
| MP8831AN | 28 Lead 300 Mil PDIP | -40°C to +85°C |
| MP8831AS | 28 Lead 300 Mil JEDEC SOIC | -40°C to +85°C |



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## BLOCK DIAGRAM

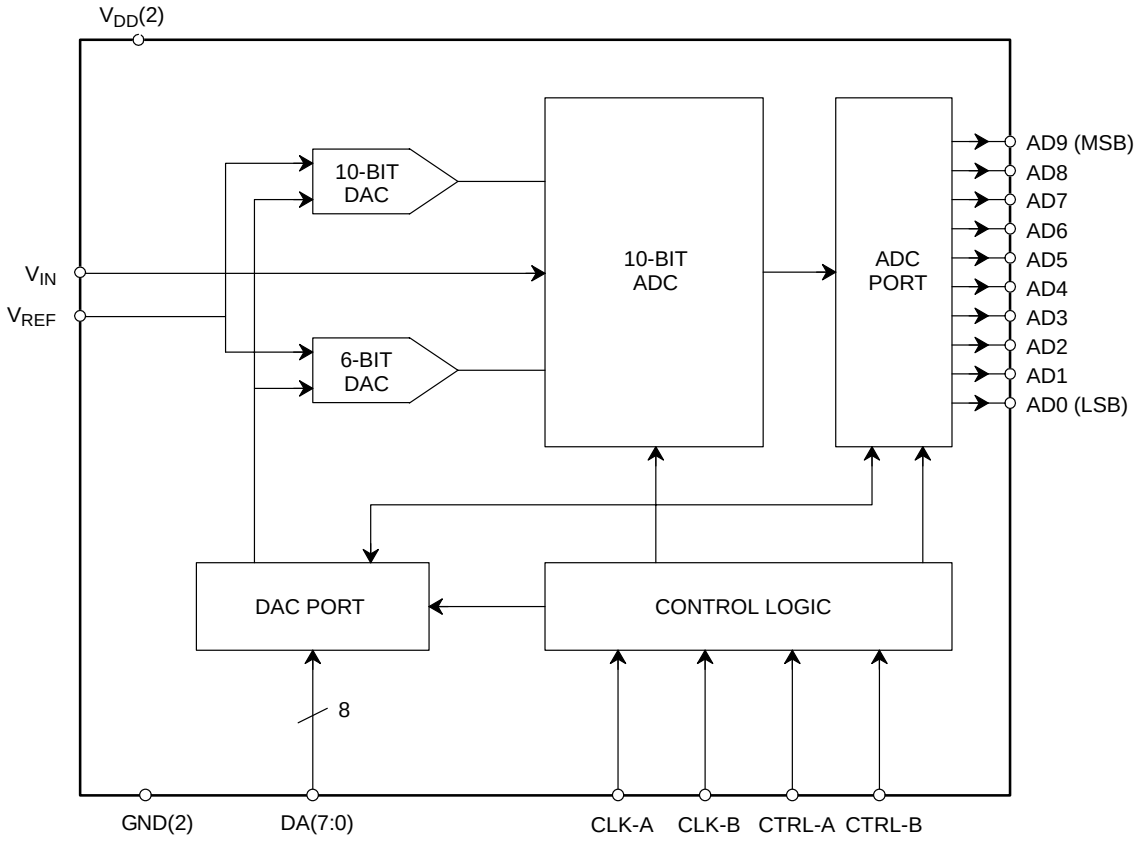
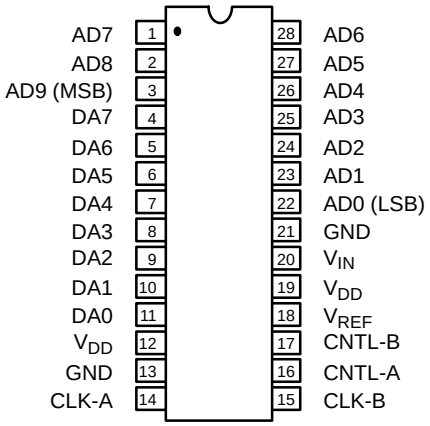
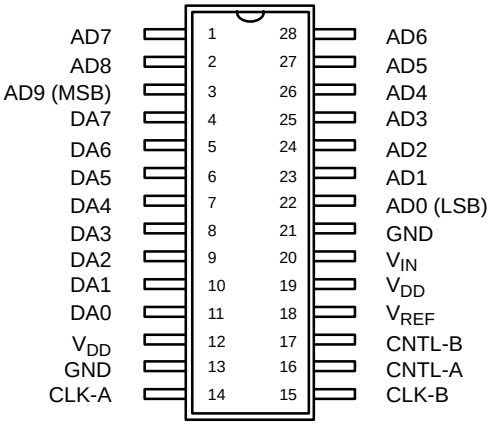



**Figure 1. Block Diagram**

## PIN CONFIGURATION




**28 Lead PDIP (0.300”)**




**28 Lead SOIC (Jedec, 0.300”)**

## PIN DESCRIPTION

| Pin # | Symbol | Description |
|---|---|---|
| 1 | AD7 | ADC Bus Bit 7. |
| 2 | AD8 | ADC Bus Bit 8. |
| 3 | AD9 | ADC Bus Bit 9 (MSB). |
| 4 | DA7 | DAC Bus Bit 7 (MSB). |
| 5 | DA6 | DAC Bus Bit 6. |
| 6 | DA5 | DAC Bus Bit 5. |
| 7 | DA4 | DAC Bus Bit 4. |
| 8 | DA3 | DAC Bus Bit 3. |
| 9 | DA2 | DAC Bus Bit 2. |
| 10 | DA1 | DAC Bus Bit 1. |
| 11 | DA0 | DAC Bus Bit 0 (LSB). |
| 12 | $V_{DD}$ | Power Supply. |
| 13 | GND | Ground. |
| 14 | CLK-A | Controls Timing of ADC & DAC. |
| 15 | CLK-B | Controls Timing of ADC & DAC. |
| 16 | CNTL-A | Control The Operating Mode Of The Chip (*See Table 1.)* |
| 17 | CNTL-B | Control The Operating Mode Of The Chip (*See Table 1.)* |
| 18 | $V_{REF}$ | Reference Input (1V) Sets Range of DACs. |
| 19 | $V_{DD}$ | Power Supply. |
| 20 | $V_{IN}$ | Analog Input. |
| 21 | GND | Ground. |
| 22 | AD0 | ADC Bus Bit 0 (LSB). |
| 23 | AD1 | ADC Bus Bit 1. |
| 24 | AD2 | ADC Bus Bit 2. |
| 25 | AD3 | ADC Bus Bit 3. |
| 26 | AD4 | ADC Bus Bit 4. |
| 27 | AD5 | ADC Bus Bit 5. |
| 28 | AD6 | ADC Bus Bit 6. |

## DC ELECTRICAL CHARACTERISTICS

**Test Conditions: $V_{DD}$ = 5V, GND = 0V and $T_A$ = 25°C Unless Otherwise Specified**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **ADC** | | | | | | |
| n | Number of Bits | 10 | | | Bits | |
| FS | Max Effective Sample Rate | 1.67 | | | MSPS | |
| DNL | Differential Non-Linearity | -1.0 | ±0.75 | 2.0 | LSB | Gain DAC=1/2 scale, offset DAC=ZS |
| DNL | Differential Non-Linearity | -1.0 | | 2.0 | LSB | Gain DAC=FS, offset DAC=ZS |
| INL | Integral Non-Linearity | -3 | | 3 | LSB | Gain DAC=1/2 scale, offset DAC=ZS, best fit straight line |
| INL | Integral Non-Linearity | -2 | | 2 | LSB | Gain DAC=FS, offset DAC=ZS, best fit straight line |
| EZS | Zero Scale Error | | –30 | | mV | |
| EFS | Full Scale Error | | 20 | | mV | |
| $A_{INPP}$ | DC input Range | GND | | $V_{DD}$ | V | $A_{IN}$ can swing from GND to $V_{DD}$. Digitizing range is set by DAC codes. |
| $C_{IN}$ | Input Capacitance | | 10 | 20 | pF | |
| **Offset DAC** | | | | | | |
| n | Number of Bits | 6 | | | Bits | |
| DNL | Differential Non-Linearity | -0.5 | | 0.5 | LSB | Measured at bottom of ADC reference ladder through a switch. |
| INL | Integral Non-Linearity | -1 | | 1 | LSB | Measured at bottom of ADC reference ladder through a switch. |
| $VO_{ZS}$ | Effective Zero Scale Voltage | | 0.178 | | V | Measured at bottom of ADC reference ladder through a switch. |
| $VO_{FS}$ | Effective Full Scale Voltage | | 0.348 | | V | Measured at bottom of ADC reference ladder through a switch. |
| MOC | Maximum Change per Conversion | | | 100 | % FS | After specified change in DAC setting, the ADC should output the same code ± 2LSB, assuming analog input is constant. |
| ts-od | Settling Time | | 300 | | ns | Not tested. Guaranteed by design. |
| **Gain DAC** | | | | | | |
| n | Number of Bits | 10 | | | Bits | |
| DNL | Differential Non-Linearity | -1 | | 1 | LSB | Measured at top of ADC reference ladder through a switch. |
| INL | Integral Non-Linearity | -2 | | 2 | LSB | Measured at top of ADC reference ladder through a switch, (BFSL). |
| $VG_{ZS}$ | Effective Zero Scale Voltage | | $VO_{FS}$ 0.00 | | V | Measured at top of ADC reference ladder through a switch. Offset DAC = ZS |

## DC ELECTRICAL CHARACTERISTICS (CONT'D)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Gain DAC (Cont'd)** | | | | | | |
| $VG_{FS}$ | Effective Full Scale Voltage | | $VO_{FS}$ 2.82 | | V | Measured at top of ADC reference ladder through a switch. Offset DAC = ZS |
| MGC | Maximum Change per Conversion | | | 20 | % FS | After specified change in DAC setting, the ADC should output the same code ± 1 LSB, assuming analog input is constant. |
| ts-od | Settling Time | | 300 | | ns | Not Tested. Guaranteed by design. |
| **Digital Characteristics** | | | | | | |
| $V_{IH}$ | Digital Input High Voltage | 3.5 | | | V | |
| $V_{IL}$ | Digital Input Low Voltage | | | 1.5 | V | |
| $V_{OH}$ | Digital Output High Voltage | 4.5 | | | V | While sourcing 2mA. |
| $V_{OL}$ | Digital Output Low Voltage | | | 0.5 | V | While sinking 2mA. |
| $I_{OZ}$ | High-Z Leakage | | | 10 | µA | When inputs are idle or reading DAC data. |
| **Digital Timing Specifications (Convert Mode)** | | | | | | |
| $t_{DV}$ | Data Valid Delay (Rising Edge CLK-A to AD[9:0] New Data Valid | | 30 | 50 | ns | With 30 pF load on each pin. AD[9:0] |
| $t_{SET1}$ | DAbus Setup Time 1 | 40 | | | ns | DA[7:0] to rising edge CLK-B. |
| $t_{SET2}$ | DAbus Setup Time 2 | 40 | | | ns | DA[7:0] to rising edge CLK-A. |
| $t_{HOLD1}$ | DAbus Hold Time 1 | | | 0 | ns | Rising edge CLK-B to DA[7:0]. |
| $t_{HOLD2}$ | DAbus Hold Time 2 | | | 0 | ns | Rising edge CLK-A to DA[7:0]. |
| $t_1$ | Clock Timing | 100 | 200 | | ns | Rising edge CLK-B to falling edge CLK-A. |
| $t_2$ | Clock Timing | 200 | 200 | 25,000 | ns | Negative pulse width CLK-A. |
| $t_3$ | Clock Timing | 100 | 200 | 25,000 | ns | Rising edge CLK-A to falling edge CLK-B. |
| $t_4$ | Clock Timing | 200 | 200 | 25,000 | ns | Negative pulse width CLK-B. |

## DC ELECTRICAL CHARACTERISTICS (CONT'D)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| **Pass-Through Mode AD=>DA** | | | | | | |
| $t_{10}$ | DAbus Release to CNTL-A Falling Edge | 0 | | | ns | External ckts must stop driving DA-bus by the time CNTL-A falls. |
| $t_{11}$ | CNTL-A Falling Edge to ADbus Release | | 20 | 40 | ns | Delay from falling edge CNTL-A until chip stops driving ADC data on ADbus. External ckts may not drive data onto ADbus before this time. |
| $t_{12}$ | Pass-Through Mode Propagation Delay From ADbus to DAbus | | 17 | 30 | ns | CNTL-A=low, CNTL-B=high; 30 pF load. |
| $t_{13}$ | ADbus Release to CNTL-A Rising Edge | 0 | | | ns | External ckts must stop driving AD-bus by the time CNTL-A rises. |
| $t_{14}$ | CNTL-A Rising Edge to ADbus Enable | | 30 | 50 | ns | After this time ADbus will output previous ADC data again. |
| $t_{15}$ | CNTL-A Rising Edge to DAbus Release | | 20 | 40 | ns | Delay from rising edge CNTL-A until chip stops driving data on DAbus. External ckts may not drive data onto DAbus before this time. |
| **Pass-Through Mode DA=>AD** | | | | | | |
| $t_{16}$ | CNTL-B Falling Edge to ADbus Pass-through Data Valid | | 30 | 50 | ns | Time required for ADbus change from ADC data to DAbus pass-through data. |
| $t_{17}$ | Pass-Through Mode Propagation Delay From DAbus to ADbus | | 19 | 35 | ns | CNTL-A=high, CNTL-B=low; 30 pF load. |
| $t_{18}$ | CNTL-B Rising Edge to ADbus ADC Data Valid | | 30 | 50 | ns | Time required for ADbus change from DAbus pass-through data to ADC data. |
| **Power Supply** | | | | | | |
| $V_{DD}$ | Operating Voltage | 4.5 | 5 | 5.5 | V | |
| $I_{DD}$ | Operating Current | 30 | 35 | 40 | mA | |
| | Power Down $I_{DD}$ | | 0.2 | 0.5 | mA | |

**Specifications are subject to change without notice**

### ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND ..... -0.3 to 6 V
All Inputs ..... $V_{DD}$ +0.5 to GND -0.5
All Inputs ..... $V_{DD}$ +0.5 to GND -0.5
Storage Temperature ..... -65°C to +150°C

Lead Temperature (soldering, 10 sec) ..... +300°C
ESD Rating/Latch-up ..... 2000V/100mA
Package Power Dissipation ..... 850mW
Derate above 75°C ..... 12mW/°C

***Notes:***

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

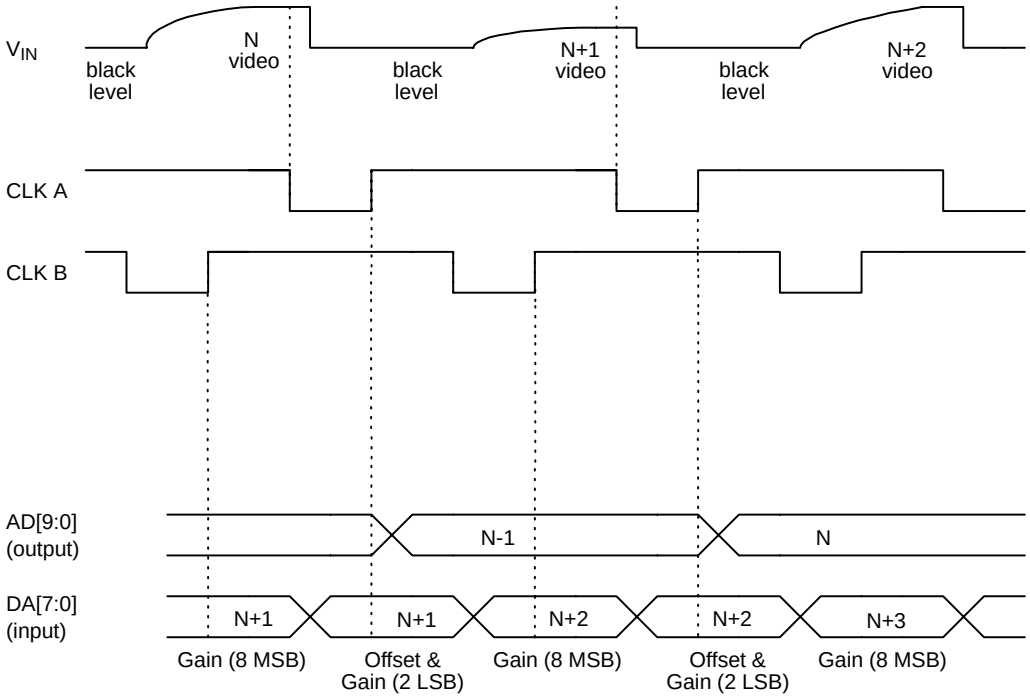



**Figure 2. Convert Mode Operation**

| Cntl A | Cntl B | Operation Mode |
|---|---|---|
| 0 | 0 | Test mode ($V_{RT} \Rightarrow$ AD[9]; $V_{RB} \Rightarrow$ AD[8] |
| 0 | 1 | Pass-through mode AD[7:0] $\Rightarrow$ DA[7:0] |
| 1 | 0 | Pass-through mode DA[7:0] $\Rightarrow$ AD[7:0] |
| 1 | 1 | Convert mode |

**Table 1. Truth Table**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Rising Edge of CLK B | GD9 | GD8 | GD7 | GD6 | GD5 | GD4 | GD3 | GD2 |
| | (DA7) | | | | | | | (DA0) |
| Rising Edge of CLK A | OS5 | OS4 | OS3 | OS2 | OS1 | OS0 | GD1 | GD0 |
| | (DA7) | | | | | | | (DA0) |

***Notes***
– *(GD9-GD0 is the gain DAC data,OS5-OS0 is the offset DAC data)*
– *Forcing GD1 & GD0 to 0 gives an 8 bit resolution gain DAC, but will simplify the I/O.*

**Table 2. DAC Data Format**

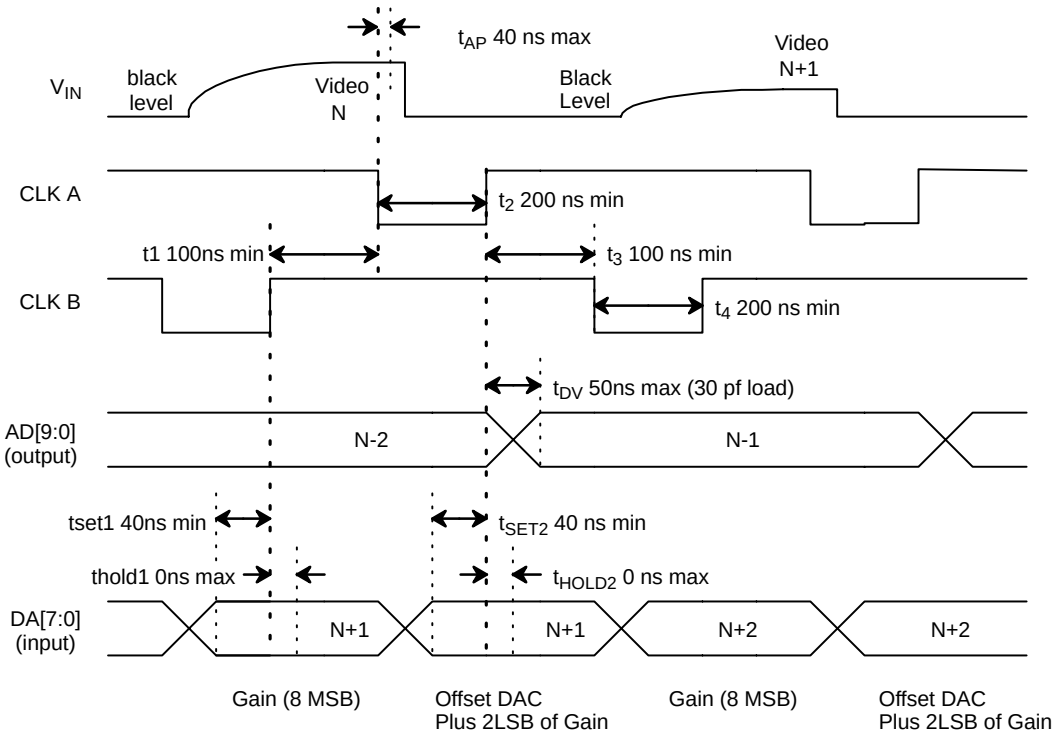



**Figure 3. Convert Mode Timing Diagram**

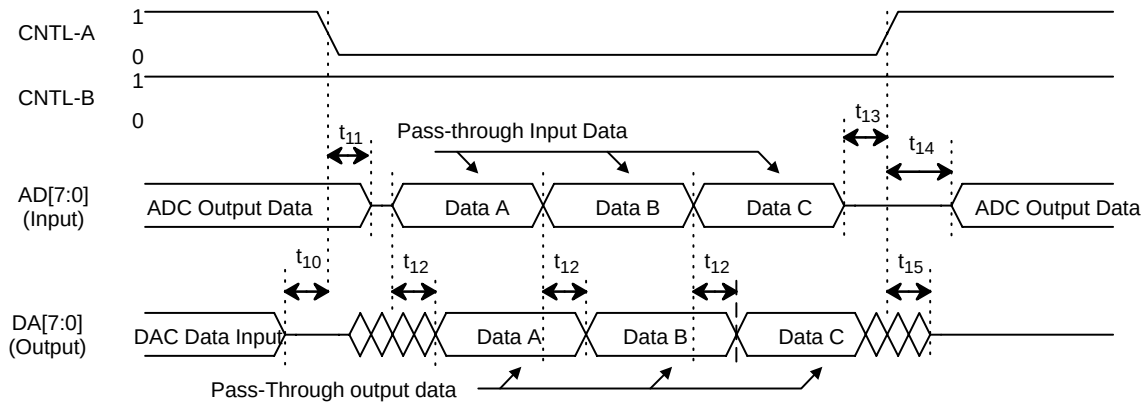



**Figure 4. Pass-Through Mode (AD=>DA) Timing Diagram**

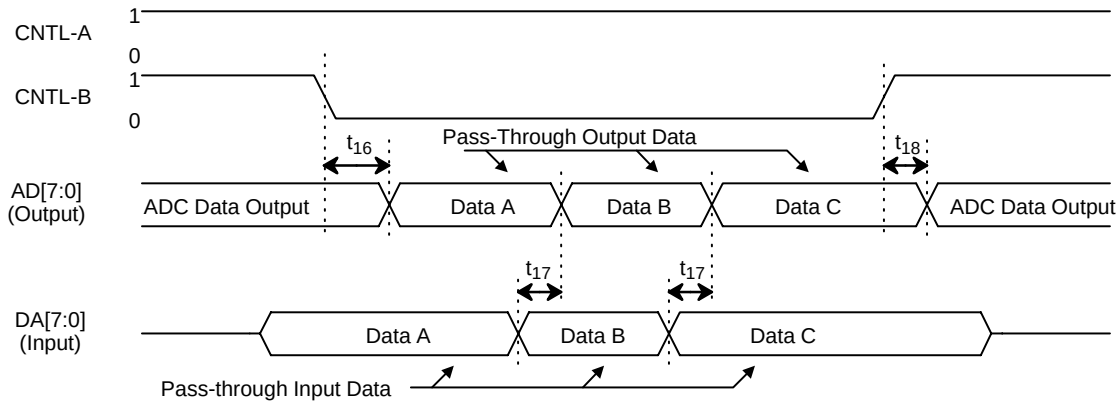



**Figure 5. Pass-Through mode (DA=>AD) Timing Diagram**

## OPERATION MODES

The two signals CNTL-A & CNTL-B are used to put the chip into one of the four operation modes.

### Convert Mode (CNTL-A=high, CNTL-B=high)

This is the normal operation mode. Data for the offset & gain DACs is read in from the DA bus, and ADC data is output on the AD bus.

### Pass-Through Mode
### AD => DA (CNTL-A=low, CNTL-B=high)
### DA => AD (CNTL-A=high, CNTL-B=low)

The pass-through modes are intended to allow the digital ASIC (or µprocessor, DSP, etc) to read from and write to the memory bank which holds the gain and offset DAC data, without requiring a separate data bus between the ASIC and the memory. In the AD => DA mode, pins AD[7:0] are programmed as digital inputs, and they simply pass data (through an internal bus) to pins DA[7:0] which are programmed as digital outputs. In the DA => AD mode things are reversed, DA[7:0] are programmed as

digital inputs and AD[7:0] are programmed as digital outputs. Please note that when DA[7:0] are used as inputs they accept TTL level signals, when AD[7:0] are used as inputs they accept CMOS level inputs.

While in either of the pass-through modes, CLK-A & CLK-B should both be held high.

**Test Mode (CNTL-A=low, CNTL-B=low)**

This mode is used to test the gain and offset DACs. The ADC reference voltages are output on the two MSB pins of the AD bus, $V_{RT}$ on pin AD9 and $V_{RB}$ on pin AD8. The data from the DA bus is read in to the DACs the same as during normal conversion operation (i.e. on the rising edges of CLK-A & CLK-B).

**Controlling ADC Gain and Offset**

The input range of the ADC is set by the voltages at its top ($V_{RT}$) and bottom ($V_{RB}$) reference nodes. The Offset DAC sets the voltage at the $V_{RB}$ node. The Gain DAC sets the span $V_{RT}$-$V_{RB}$. The following equations relate the DAC codes to the voltages at $V_{RB}$ & $V_{RT}$:

$V_{REF}$ = voltage at $V_{REF}$, pin 18

$D_{OFFSET}$ = Offset DAC code, 6 bits, OS[5:0]

$D_{GAIN}$ = Gain DAC code, 10 bits, GD[9:0]

$$V_{RB} = \left(0.178 + \frac{D_{OFFSET}}{64} \cdot 0.170\right) \cdot V_{REF}$$

$$V_{RT} - V_{RB} = \left(\frac{D_{GAIN}}{1024}\right) \cdot 2.82 \cdot V_{REF}$$

$$V_{RT} = \left\{\left(\frac{D_{GAIN}}{1024}\right) \cdot 2.82 \cdot V_{REF}\right\} + V_{RB}$$

***Note:***
*The output of the Gain DAC becomes non-linear when $V_{RT}$, calculated using the above equations, is higher than $V_{DD}$-1.6V. The ADC itself remains linear, but its input range, set by the DACs, deviates from the calculated values. This can only happen if $V_{REF}$ is larger than 1.068V.*

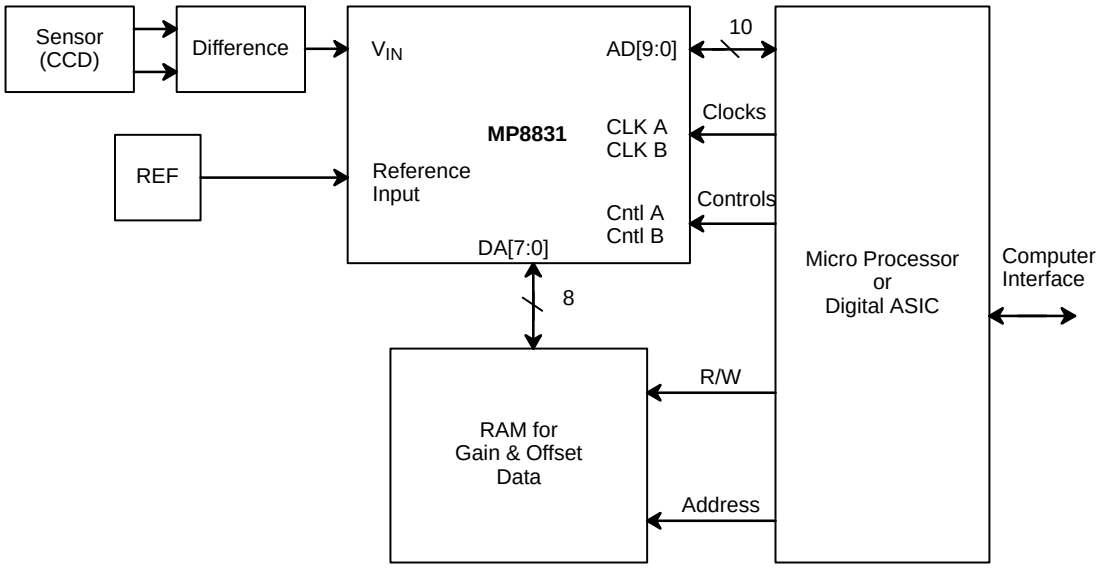
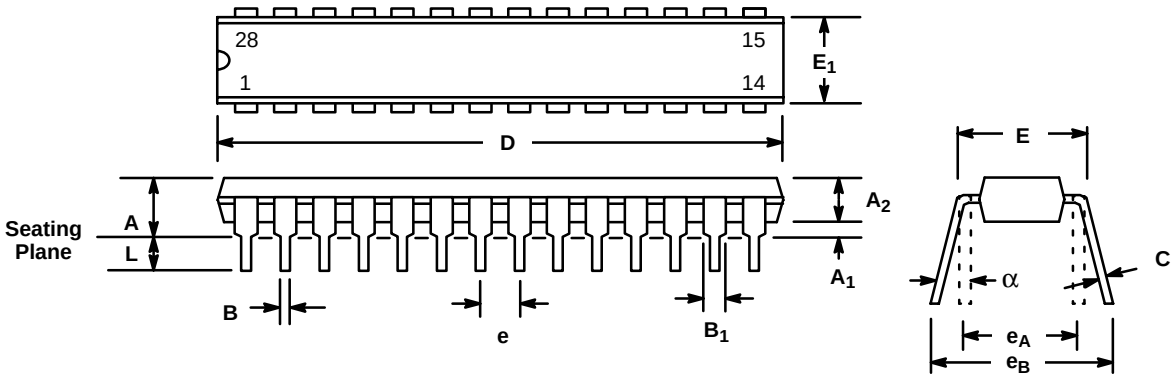



**Figure 6. General Scanner System Using the MP8831**

# 28 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

*Rev. 1.00*

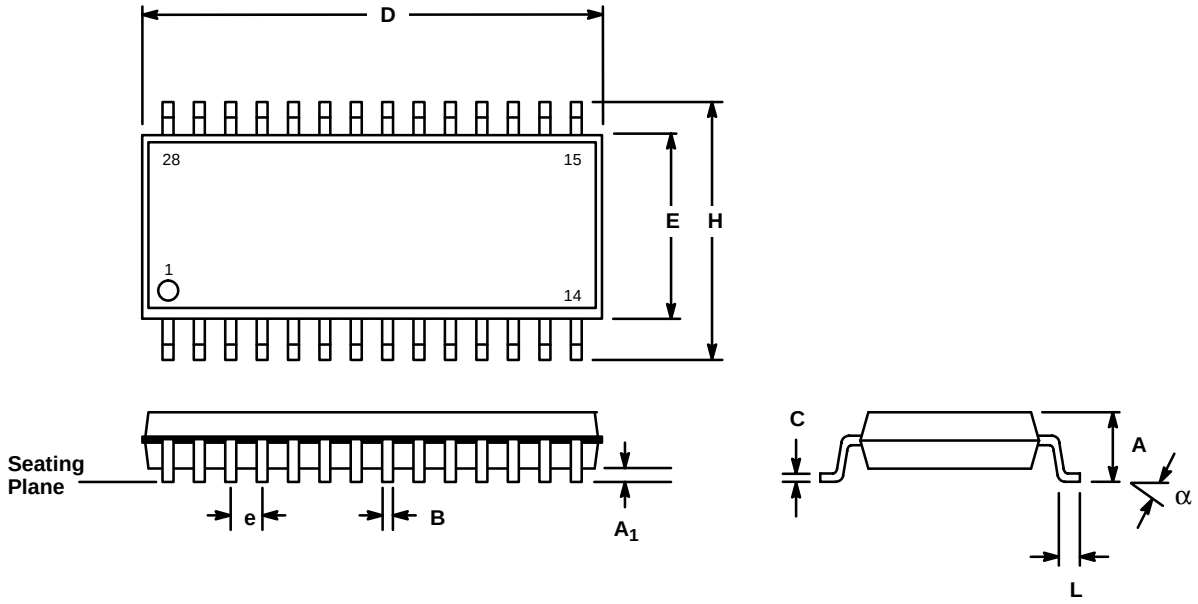



| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.145 | 0.210 | 3.68 | 5.33 |
| $A_1$ | 0.015 | 0.070 | 0.51 | 1.78 |
| $A_2$ | 0.115 | 0.195 | 2.92 | 4.95 |
| B | 0.014 | 0.024 | 0.36 | 0.56 |
| $B_1$ | 0.030 | 0.070 | 0.76 | 1.78 |
| C | 0.008 | 0.014 | 0.20 | 0.38 |
| D | 1.345 | 1.400 | 34.16 | 35.56 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| $E_1$ | 0.265 | 0.310 | 7.11 | 7.49 |
| e | 0.100 BSC | | 2.54 BSC | |
| $e_A$ | 0.300 BSC | | 7.62 BSC | |
| $e_B$ | 0.310 | 0.430 | 7.87 | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |

*Note: The control dimension is the inch column*

## 28 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)

*Rev. 1.00*




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.697 | 0.713 | 17.70 | 18.10 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

*Note: The control dimension is the millimeter column*

# Notes

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# Notes

NOTICE

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