NEC

MOS INTEGRATED CIRCUIT

MC-42S4000LAB32

4 M-WORD BY 32-BIT DYNAMIC RAM MODULE (SO DIMM) FAST PAGE MODE

Description

The MC-42S4000LAB32 is a 4,194,304 words by 32 bits dynamic RAM module (Small Outline DIMM) on which 8 pieces of 16 M DRAM: μPD42S17800L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 4,194,304 words by 32 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-42S4000LAB32-A60	60 ns	110 ns	1,448 mW	4.32 mW (CMOS level input)
MC-42S4000LAB32-A70	70 ns	130 ns	1,304 mW	
MC-42S4000LAB32-A80	80 ns	150 ns	1,160 mW	

- 2,048 refresh cycles/128 ms
- 72-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V ±0.3 V power supply

Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-42S4000LAB32SA-A60	60 ns	72-pin Dual In-line Memory Module (Socket Type) Edge connector: Gold plated	8 pieces of μPD42S17800LG5 (400 mil TSOP (II)) [Double side]
MC-42S4000LAB32SA-A70	70 ns		
MC-42S4000LAB32SA-A80	80 ns		

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

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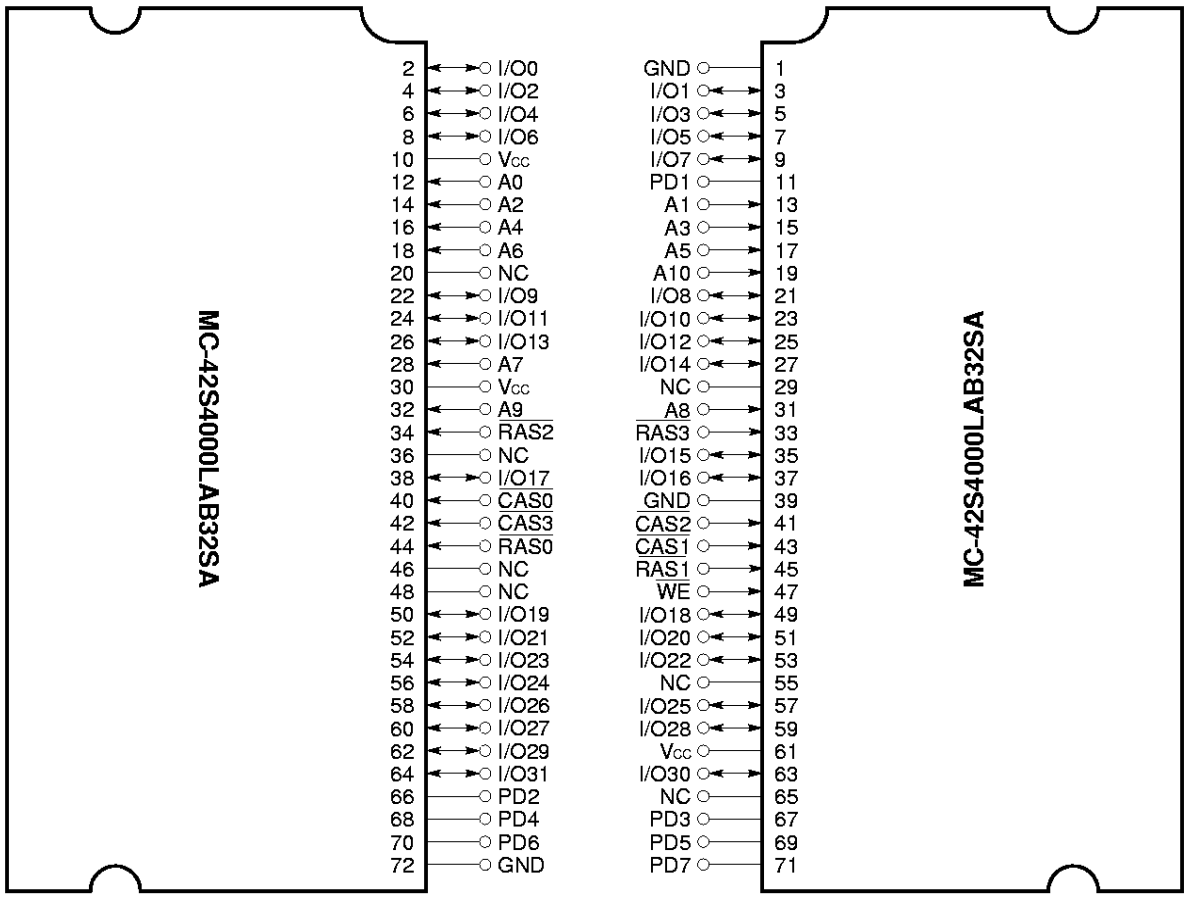
Pin Configuration

72-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

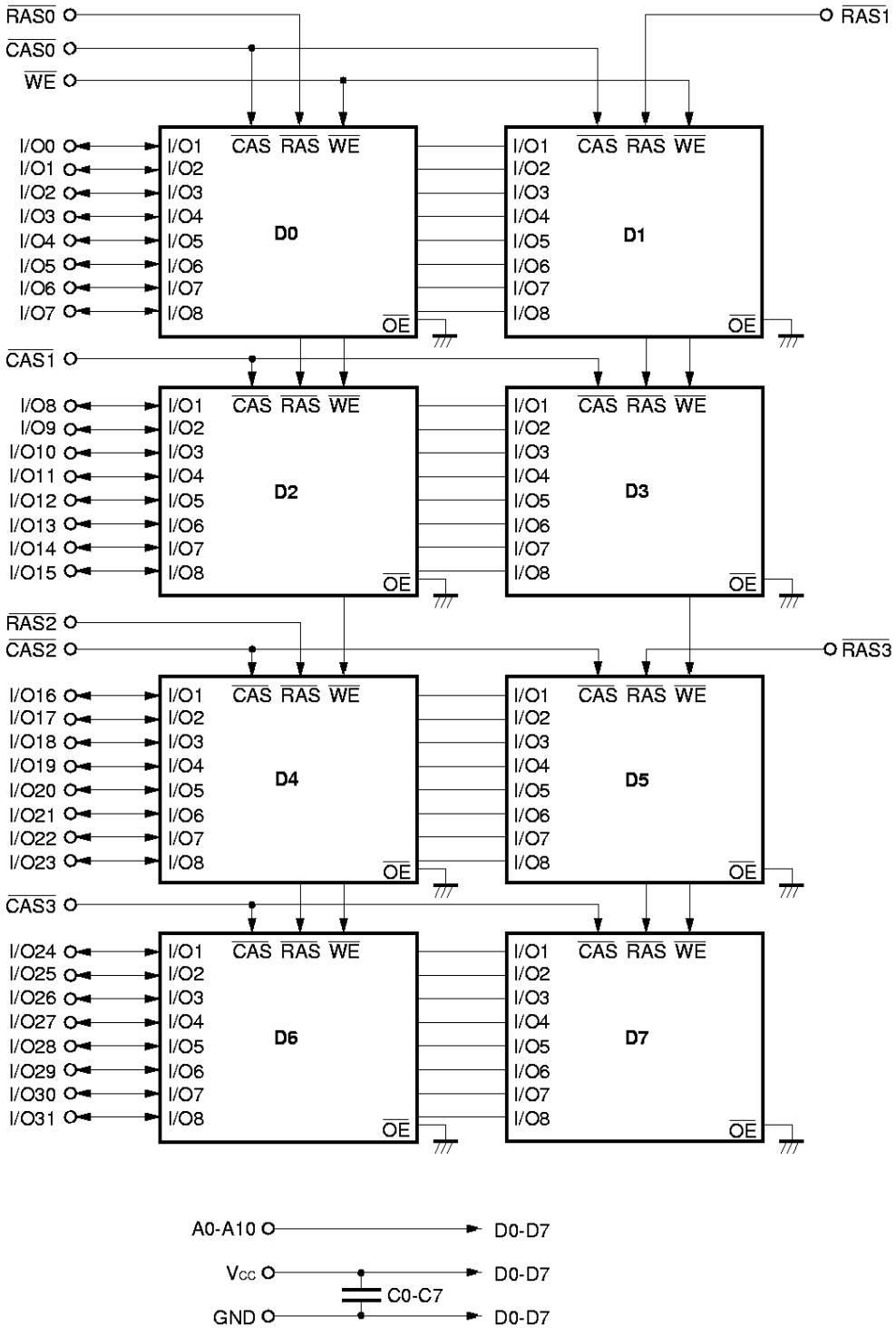


A0 - A10 : Address Inputs
[Row: A0-A10, Column: A0-A9]
I/O0 - I/O31 : Data Inputs/Outputs
$\overline{RAS0}$ - $\overline{RAS3}$: Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$: Column Address Strobe
$\overline{WE}$: Write Enable
PD1 - PD7 : Presence Detect Pins
VCC : Power Supply
GND : Ground
NC : No connection

The internal connection of PD pins (PD1 to PD7).

Pin name	Pin No.	Access time		
		60 ns	70 ns	80 ns
PD1	11	GND	GND	GND
PD2	66	NC	NC	NC
PD3	67	GND	GND	GND
PD4	68	GND	GND	GND
PD5	69	NC	GND	NC
PD6	70	NC	NC	GND
PD7	71	GND	GND	GND

Block Diagram



Remark D0 - D7 : μPD42S17800L

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		–0.5 to +4.6	V
Supply voltage	V_{CC}		–0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A10			55	pF
	C_{I2}	$\overline{WE}$			71	
	C_{I3}	$\overline{RAS0}$ - $\overline{RAS3}$			30	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			24	
Data input/output capacitance	$C_{I/O}$	I/O0 - I/O31			19	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		402	mA	1, 2, 3
			t_{RAC} = 70 ns		362		
			t_{RAC} = 80 ns		322		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$	I_O = 0 mA		4.0	mA	
		$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V	I_O = 0 mA		1.2		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS} \geq V_{IH\ (MIN.)}$ $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		402	mA	1, 2, 3, 4
			t_{RAC} = 70 ns		362		
			t_{RAC} = 80 ns		322		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling $t_{PC} = t_{PC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		282	mA	1, 2, 5
			t_{RAC} = 70 ns		242		
			t_{RAC} = 80 ns		202		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ cycling $t_{RC} = t_{RC\ (MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		402	mA	1, 2
			t_{RAC} = 70 ns		362		
			t_{RAC} = 80 ns		322		
★ $\overline{CAS}$ before $\overline{RAS}$ long refresh current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh: t_{RC} =62.5 μs $\overline{RAS}$, $\overline{CAS}$: $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$	$t_{RAS} \leq 300$ ns		3.2	mA	1, 2
		Standby: $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V Address : V_{IH} or V_{IL} $\overline{WE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leq 1$ ns		3.6		
★ $\overline{CAS}$ before $\overline{RAS}$ self refresh current	I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: t_{RASS} = 5 ms $V_{CC} - 0.2\ V \leq V_{IH} \leq V_{IH\ (MAX.)}$ $0\ V \leq V_{IL} \leq 0.2\ V$ I_O = 0 mA			1.6	mA	2
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V All other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O\ (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.

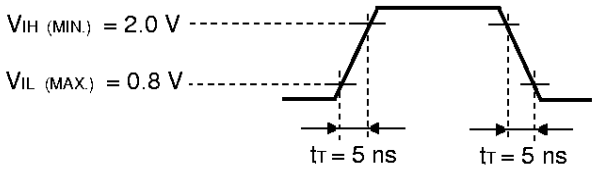
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

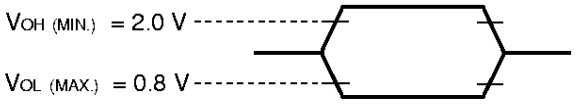
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

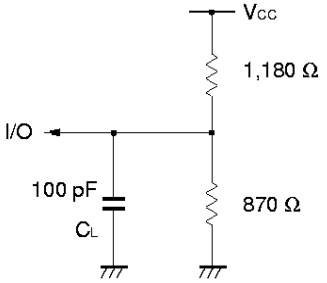
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t_{RC}	110	–	130	–	150	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	1
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	18	10,000	20	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	18	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	25	60	ns	2
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	ns	2
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	3
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	12	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns	
$\overline{CAS}$ to data setup time	t_{CLZ}	0	–	0	–	0	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
Refresh time	t_{REF}	–	128	–	128	–	128	ms	

Notes 1. In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.

2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

3. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	ns	1
Access time from $\overline{CAS}$	t_{CAC}	–	15	–	18	–	20	ns	1
Access time from column address	t_{AA}	–	30	–	35	–	40	ns	1
Column address lead time referenced to $\overline{RAS}$	t_{RAL}	30	–	35	–	40	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{CAS}$	t_{OFF}	0	13	0	15	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{RAS}$
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.

3. $t_{OFF\ (MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t_{WCH}	10	–	10	–	15	–	ns	1
$\overline{WE}$ setup time	t_{WCS}	0	–	0	–	0	–	ns	2
Data-in setup time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in hold time	t_{DH}	10	–	15	–	15	–	ns	3

Notes 1. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.

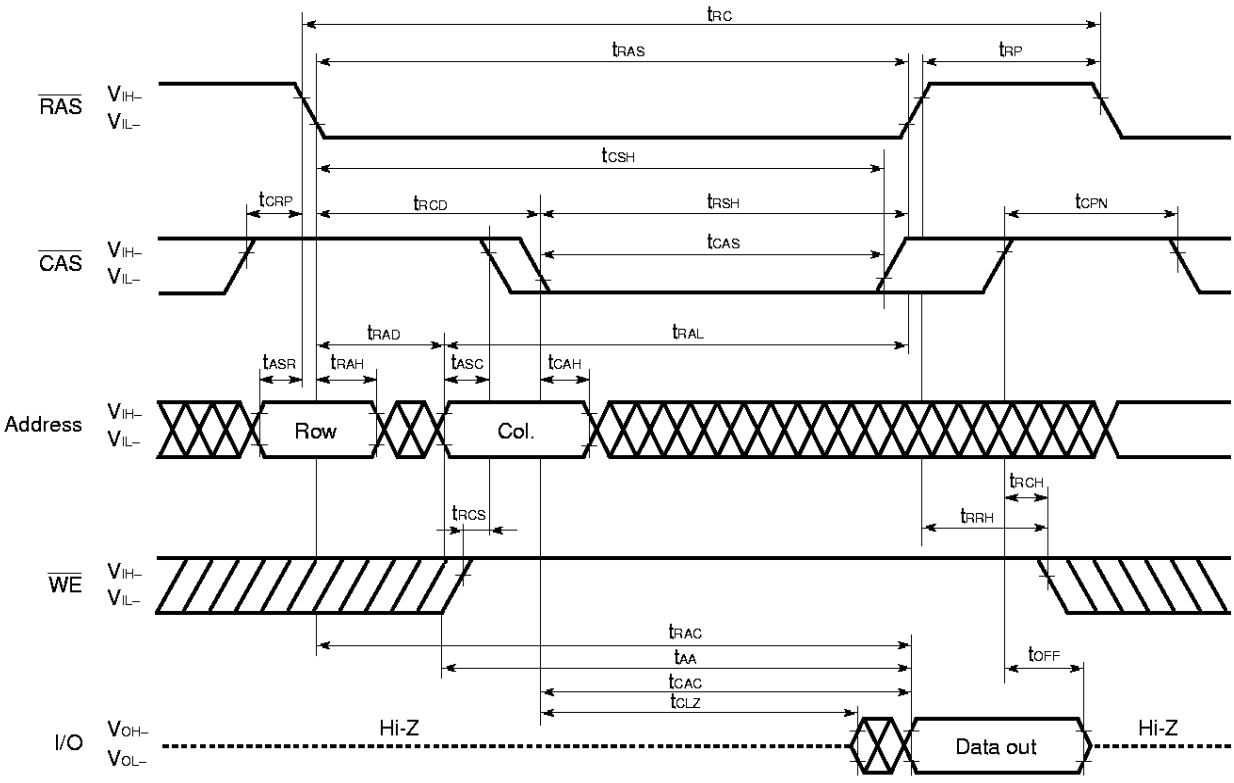
Fast Page Mode

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t_{PC}	40	–	45	–	50	–	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	–	35	–	40	–	45	ns	
$\overline{RAS}$ pulse width	t_{RASP}	60	125,000	70	125,000	80	125,000	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	–	40	–	45	–	ns	

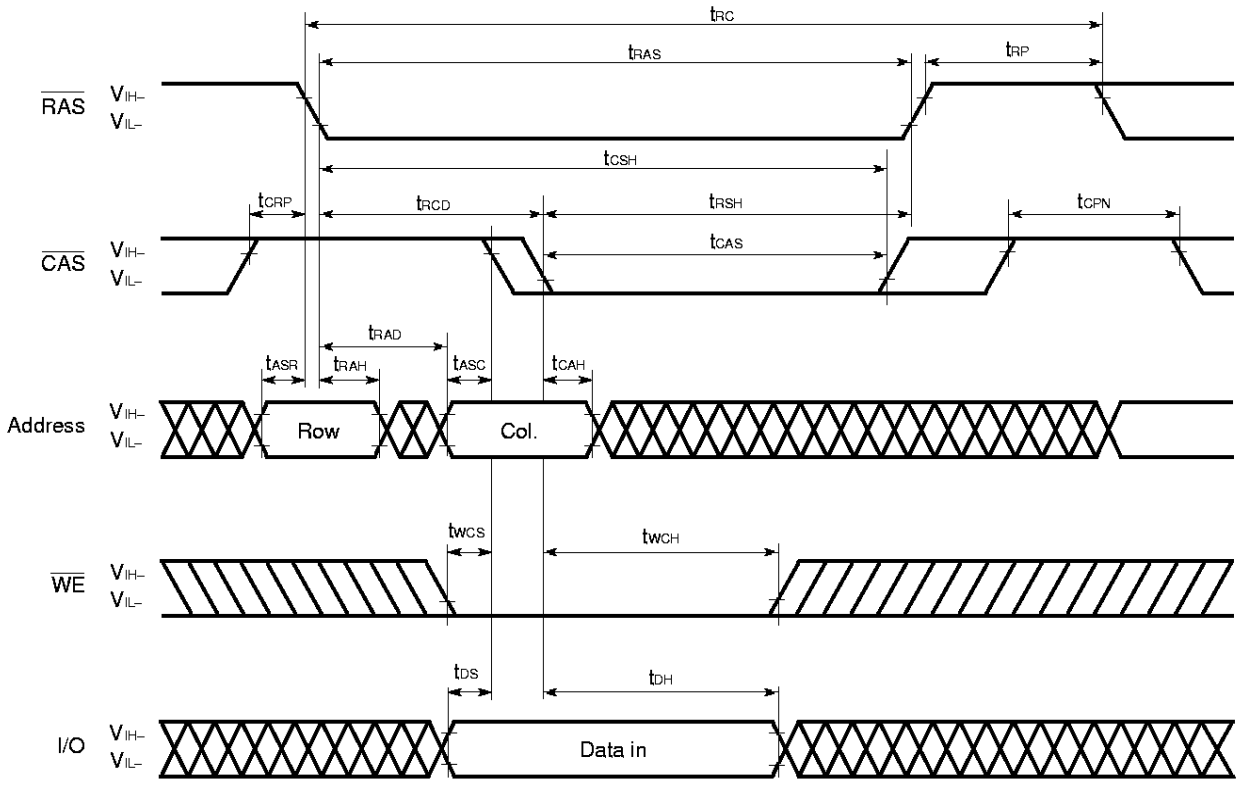
Refresh Cycle

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ setup time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RASS}	100	–	100	–	100	–	μs	
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{RPS}	110	–	130	–	150	–	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh)	t_{CHS}	–50	–	–50	–	–50	–	ns	
$\overline{WE}$ setup time	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time	t_{WHR}	15	–	15	–	15	–	ns	

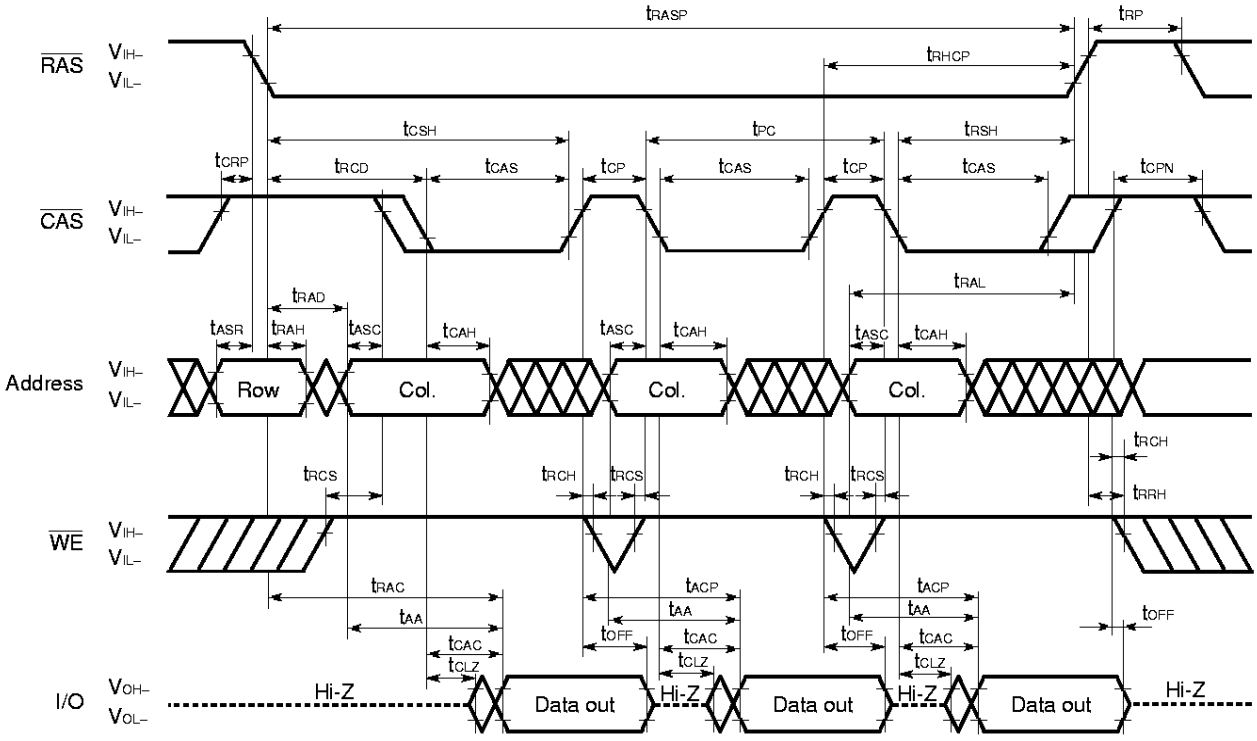
Read Cycle


tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCPN
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tRAC
tAA
tOFF
tCAC
tCLZ
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

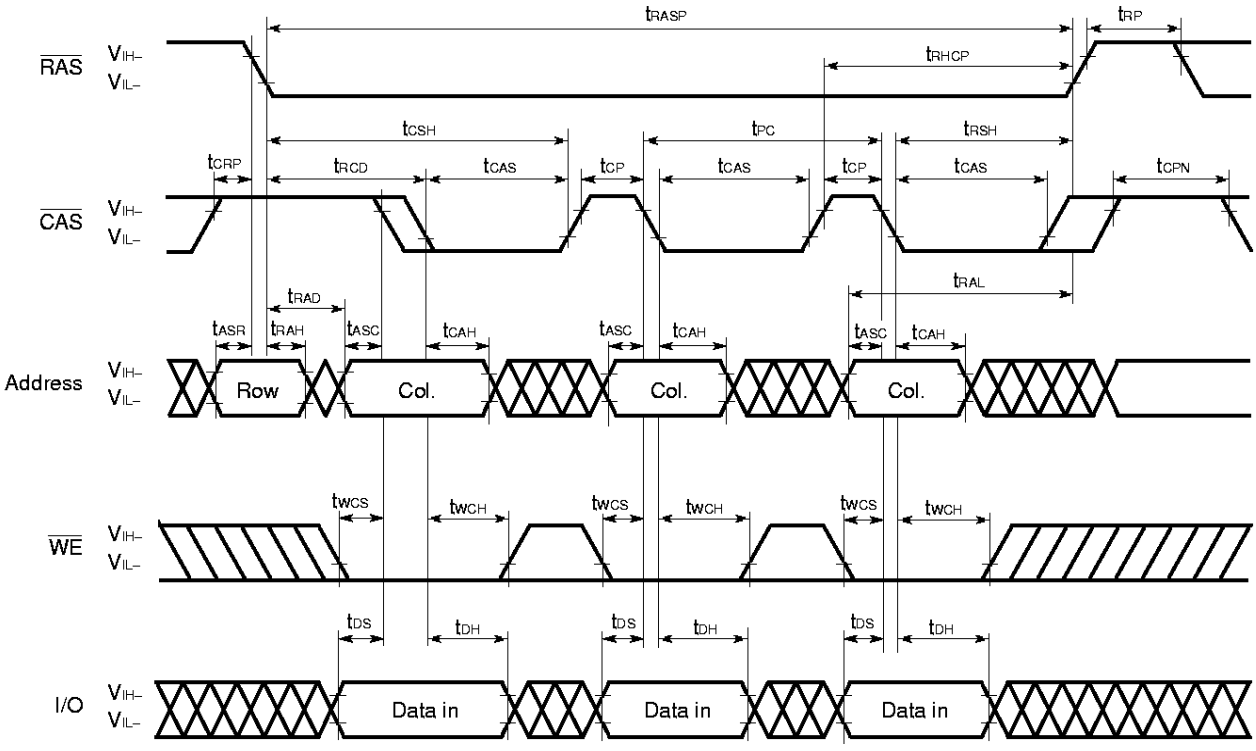


Fast Page Mode Read Cycle



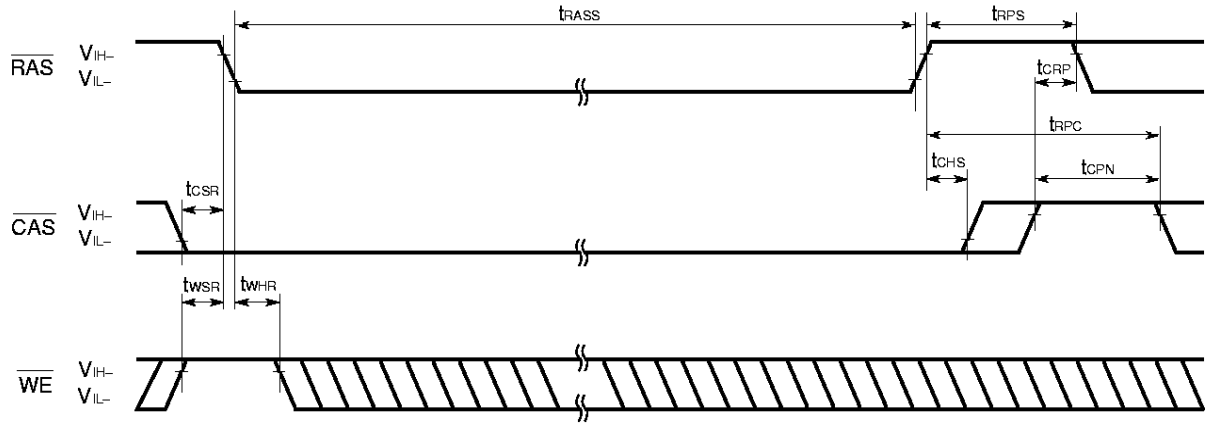
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle



Remark Address : Don't care I/O : Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

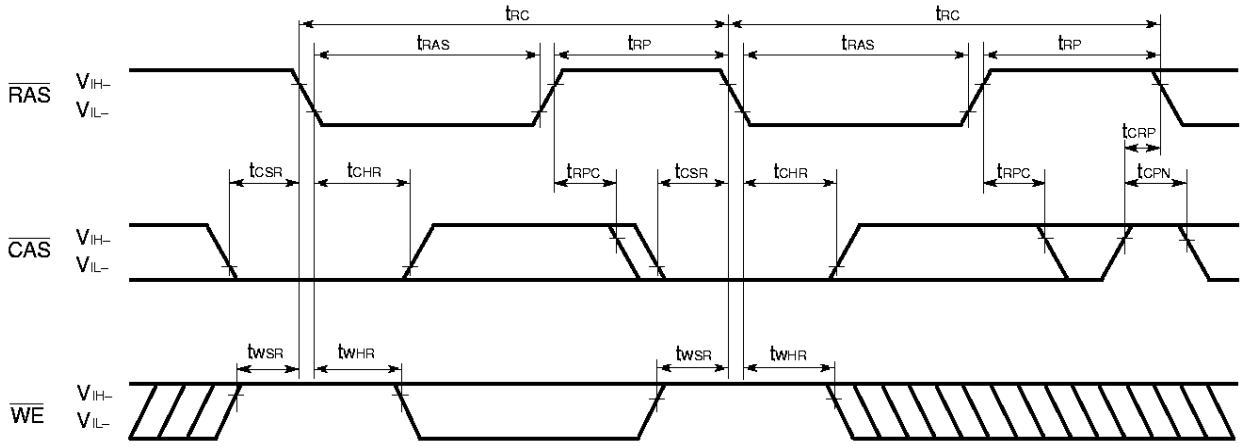
(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh

When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 2,048 times within a 32 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles (2,048/128 ms) should be met.

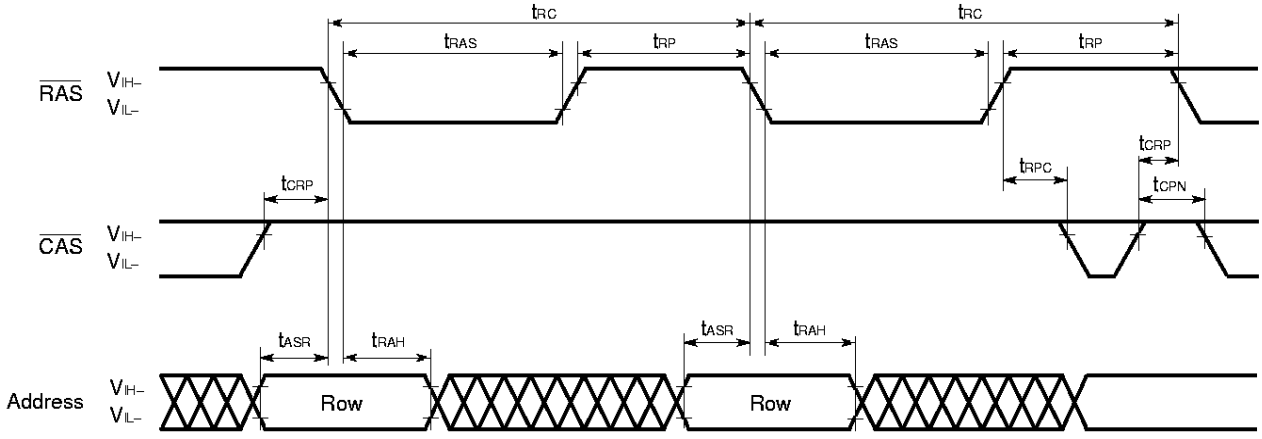
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



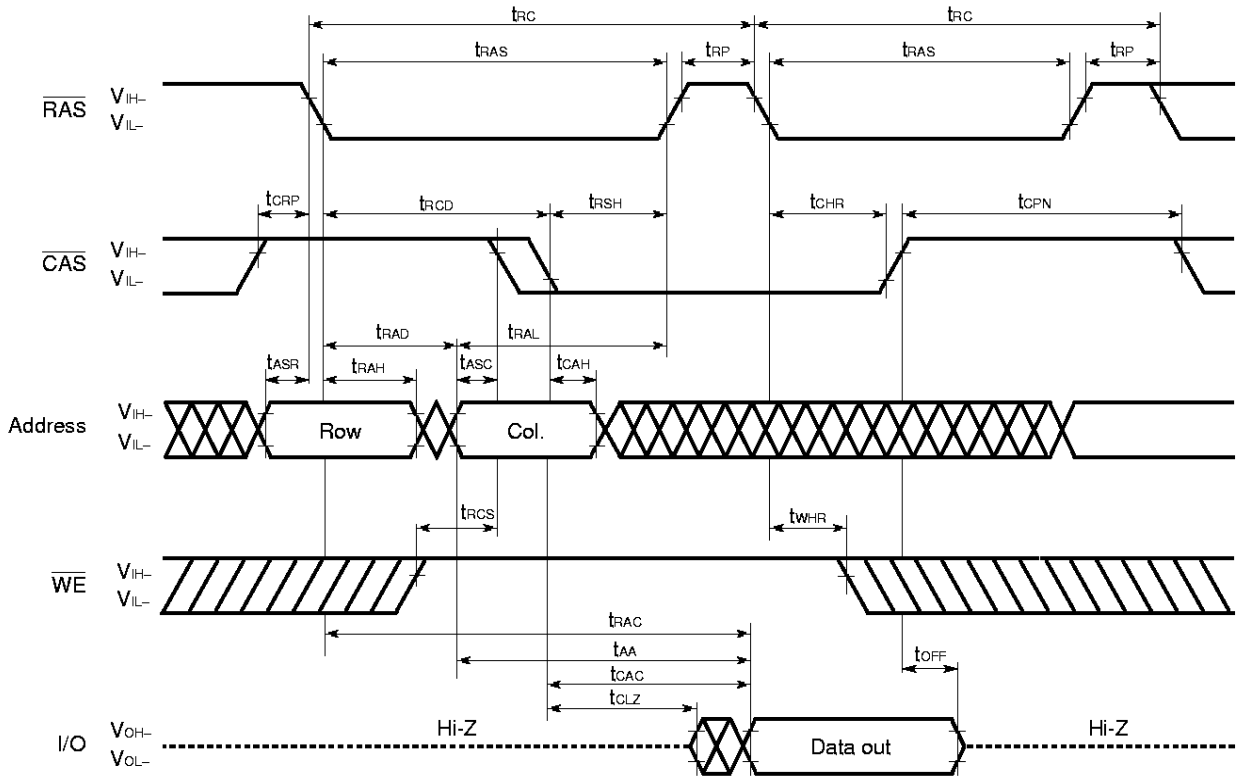
Remark Address : Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

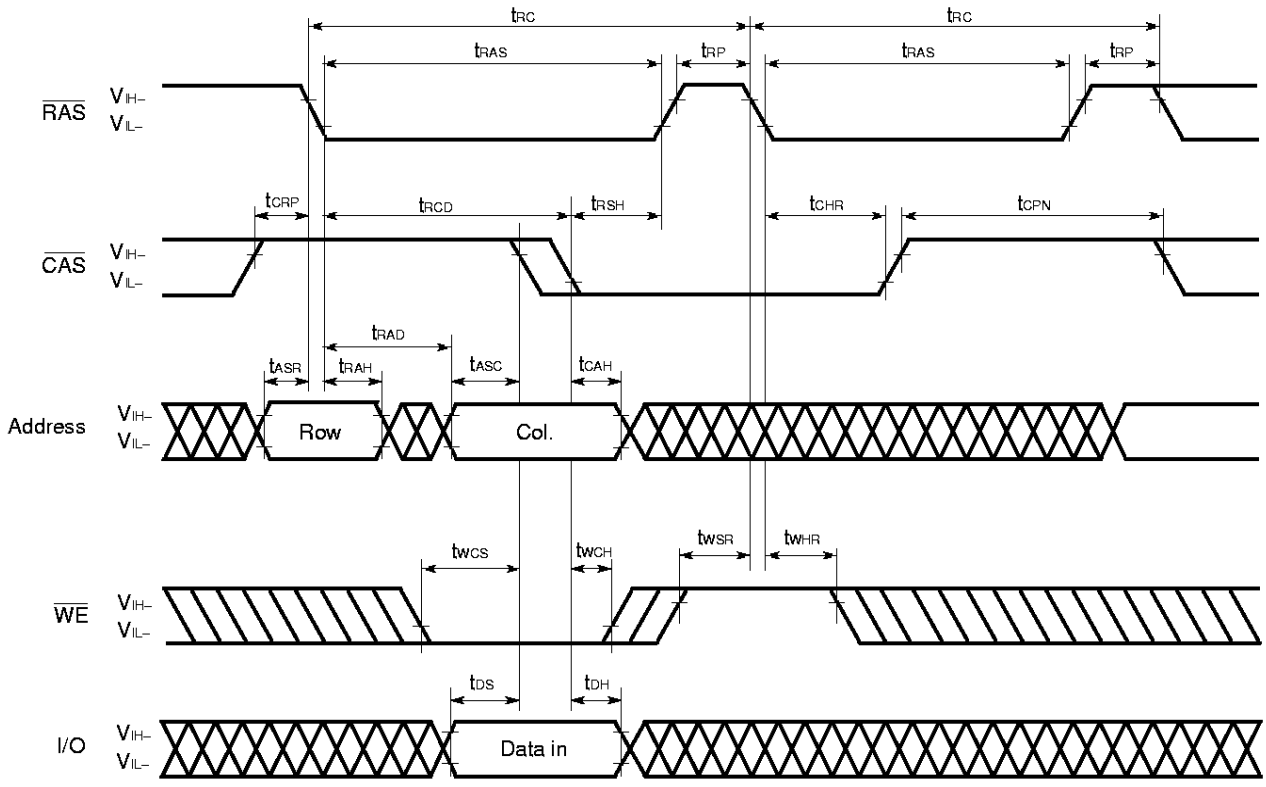


Remark $\overline{WE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

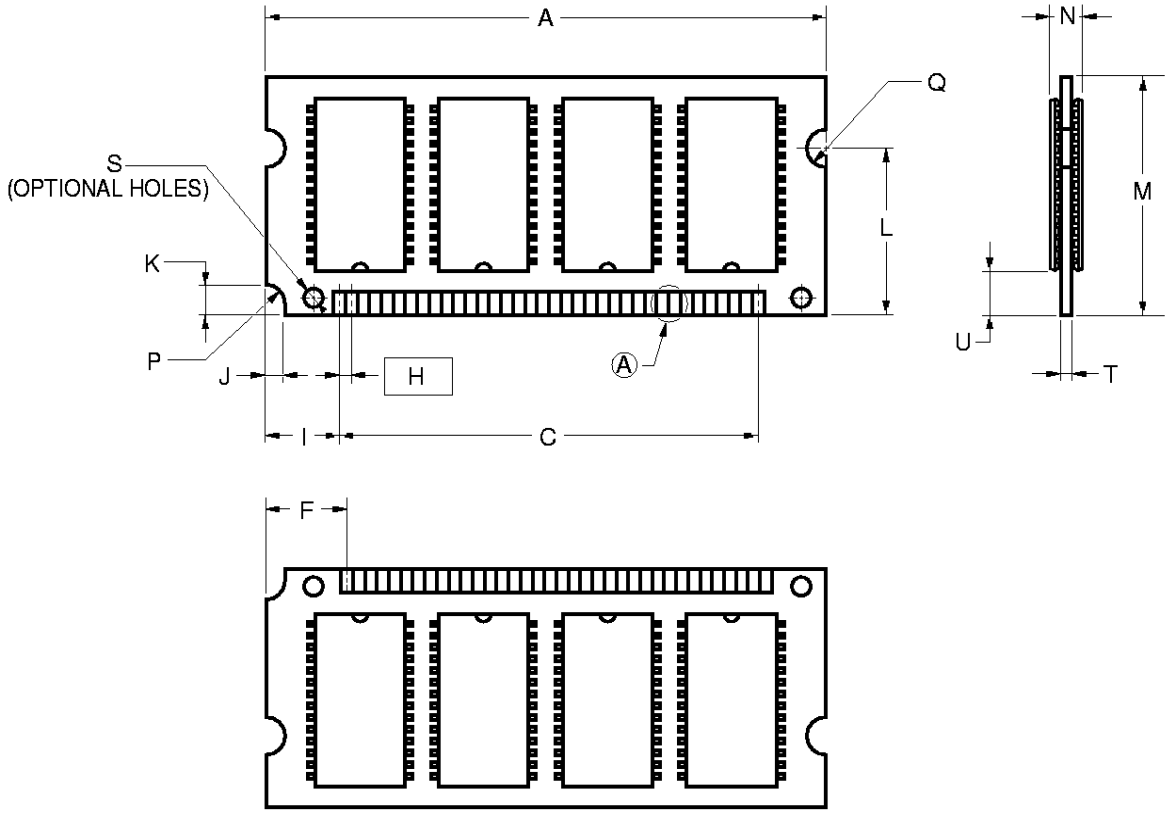


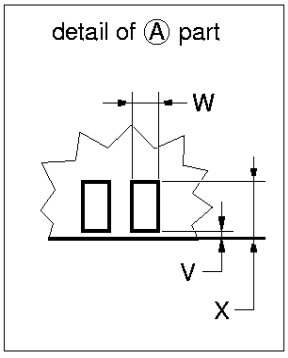
Hidden Refresh Cycle (Write)



Package Drawing

72PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS	INCHES
A	59.69±0.13	2.35±0.006
C	44.45	1.750
F	8.255	0.325
H	1.27 (T.P.)	0.050 (T.P.)
I	7.62	0.300
J	2.03±0.13	$0.080^{+0.005}_{-0.006}$
K	3.175±0.13	0.125±0.006
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	3.81 MAX.	0.150 MAX.
P	R2.0	R0.079
Q	R2.0	R0.079
S	ϕ1.8	ϕ0.071
T	1.0±0.1	$0.039^{+0.005}_{-0.004}$
U	3.175 MIN.	0.125 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

M72S-50A2-2

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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