MX·COM, INC. MX403Q

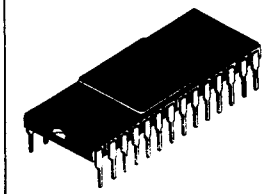
SEQUENTIAL TONE TRANSPONDER

FEATURES:

- Encodes & Decodes N-Digit Addresses
- Decodes HSC Suffix Instructions
- Accepts "Group" & "All Call" Codes
- Outputs Beeps, Call & Data Flags
- Reads/Writes Data in ROM
- CMOS Low Power Requirements

APPLICATIONS:

- Radio Alarms
- Selective Calling/Paging
- Automatic Number ID
- Supervisory Controls



MX403Q
(28p Side-Braize)

DESCRIPTION:

The MX403 Transponder compares an N-digit input sequence against digits programmed in a ROM to decode a selective calling address. It can acknowledge receipt of a valid address by encoding an N-digit reply. It is also able to encode a sequence of digits in response to a local stimulus.

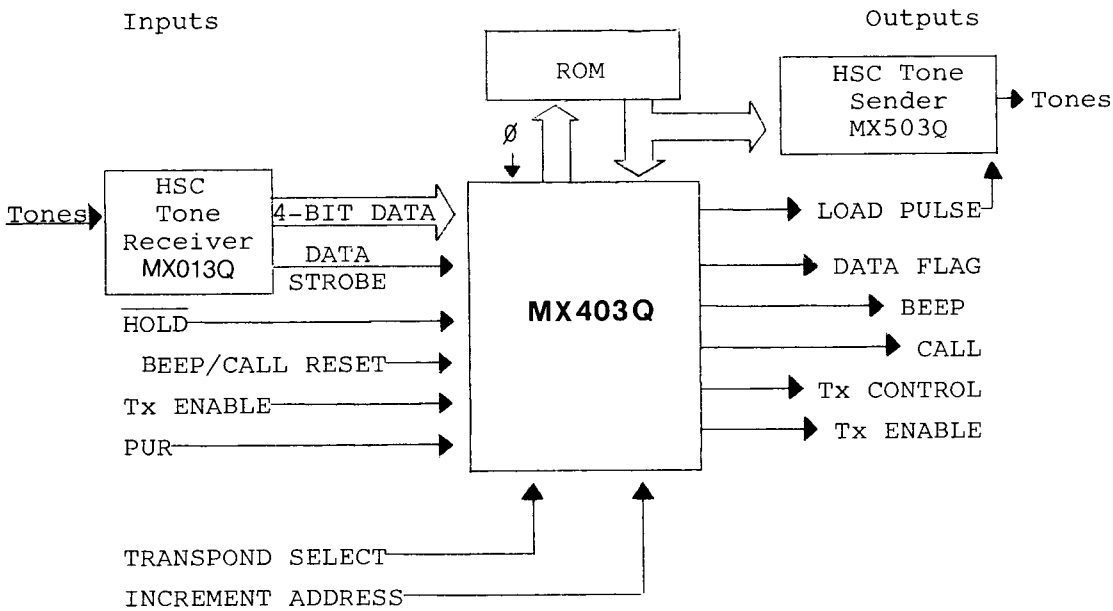


FIG. 1: MX403 INPUT/OUTPUT DIAGRAM

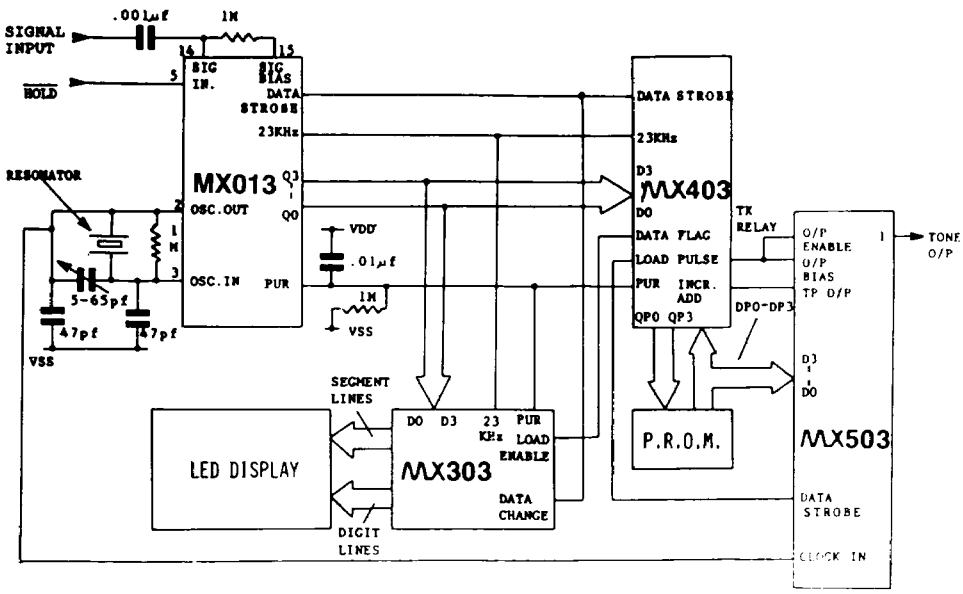
DEVICE OPERATION

Encoding is permitted only during an idle tone channel (NOTONE) condition and transpond sequences are prohibited in response to all or group call codes. The detection of a valid discrete address of 1 to 7 decimal digits results in a transponded reply of 1 to 7 digits — of the same or different data — provided the TRANSPOND SELECT line has been set true. The decoding of a discrete address results in a transponded reply provided the TRANSPOND SELECT line has been set true. If no reply is desired, entry of the flag tone "C" inhibits the transmission. Conversely, should transponding be required of a unit in which the TRANSPOND SELECT line has not been set true, entry of "C" elicits the desired encoded response. Following the transponded sequence a BEEP signal of 211Hz is output continuously in a pulsed (50% duty cycle) pattern. Also output is a continuous logic "1" on the CALL OUTPUT line, useful in unmuting audio circuits and/or lighting a call lamp.

Special function Hexadecimal Sequential Code characters (see HSC System Overview) are decoded on chip and without need of a ROM program. These permit group and all call signals, the transmission of sucessively repeated characters, address or data boundary codes, output of a data flag, and for the MX403Q, a transpond sequence.

Receipt of an all or group call inhibits transponding and outputs a continuous (100% duty cycle) BEEP and a logic "1" on the CALL line. Receipt of a discrete address followed by the data flag, code "B", results in a syncopated BEEP tone pattern, a logic "1" on the CALL OUTPUT and a load enable DATA FLAG output accompanied by a LOAD PULSE for each suceeding digit that serves to strobe data into external memory and display units.

FIG. 2: MX403 CIRCUIT CONNECTION DIAGRAM



MX403 PIN FUNCTION TABLE

PIN FUNCTION/DESCRIPTION

1 **DATA STROBE:** A short, positive pulse strobes the data presented to D0-D3.

2 a logic "1" on the PUR input (delivered by an external R-C network) for a minimum of 80μS.

3 **Vss**

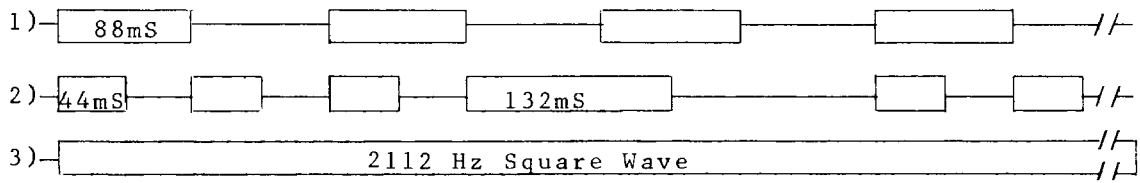
4 **BEEP RESET I/O:** This line LO in response to a discrete address or group call and all call code, can be pulled HI by an external R-C network to produce an automatic reset of the BEEP OUTPUT after a user determined period. The CALL OUTPUT is unaffected in such a case. But the output of pin 4 in response to a call that includes the data suffix "B" is a LO resulting from an internal pull-down transistor that cannot be readily pulled HI except through a low impedance circuit (a switch). In this event pulling pin 4 HI resets both BEEP and CALL OUTPUTS. Thus a subscriber may be required to manually reset the audio for calls with data appended, while the audible alarm for other calls is allowed to self reset, leaving only the CALL OUTPUT (a lamp or open speaker) as the call memory.

5 **$\overline{\text{HOLD}}$:** An input responsive to a logic "0," holds a decode sequence in abeyance at any point in a transmission — useful in imposing externally determined time limits etc. on the interval between successive decimal digits, when required. It has no effect on HSC flag tones or during encoded sequences, and does not reset the CALL, BEEP, Tx ENABLE I/O, or Tx CONTROL OUTPUTS. Hold at logic "1" to permit decoding.

6 **TRANSPOND SELECT:** With pin 6 set at Vdd the MX403Q will respond to a valid decoded discrete address with an encoded reply. The transpond sequence may be inhibited by the transmission of the suffix code "C." Conversely, a transpond sequence can be triggered in an MX303Q whose TRANSPOND SELECT line is set LO by transmission of the valid discrete address plus the suffix code "C." Thus code "C" may be viewed as an override on the TRANSPOND SELECT function of pin 6. Transponding will not result from the detection of all or group call codes. Transpond sequences commence only when the hexadecimal "F" NOTONE code is detected. BEEP and CALL are not output until the transpond sequence has been completed. Any alert pattern latched active as a result of a prior call is reset.

7 **BEEP OUTPUT:** Four beep patterns are output from this pin, as determined by the decoded address and instruction. The output impedance is 3KΩ, the tone frequency 2112Hz, Vdd-Vss squarewave. The four beep tone patterns are shown below.

Information Decoded	Audible Pattern
1) Discrete Address	50% Duty Cycle
2) Address & Data	Syncopated Pattern
3) Group Address	100% Continuous Tone
4) Suffix Code "D"	No BEEP



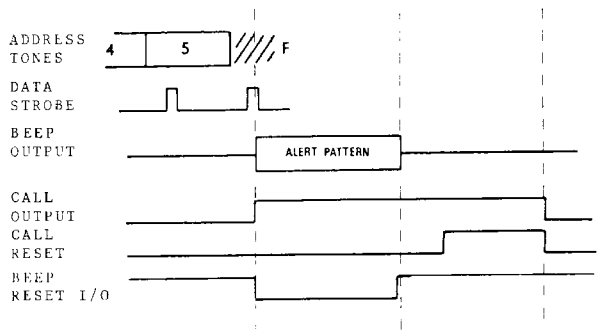
4) NO OUTPUT

FIG. 3: BEEP TONE PATTERNS

MX403 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION
8	∅: A 23.3kHz clock should be input as sourced by the MX013Q Tone Receiver.
9	**INCREMENT ADDRESS:** This input is enabled only when the Tx CONTROL output is HI, the result of either a transpond or transmit request. A Schmitt trigger associated with pin 9 is activated by a logic "1" pulse of 1mS minimum duration to increment an output 40 to 470μS later on the ROM ADDRESS lines, Qp0-Qp3 (pins 11-14). 470μS following the ROM ADDRESS output a 40μS pulse appears on the LOAD PULSE line, pin 10.
10	**LOAD PULSE:** An output that strobes the ROM ADDRESS lines Qp0-Qp3 into the ROM, triggered by a pulse on the INCREMENT ADDRESS line during a transpond or transmit sequence.
11,12, 13,14	**ROM ADDRESS, Qp0 through Qp3:** The external memory is addressed by four address lines which increment as a binary count under control of the LOAD PULSE. In the quiescent state in which the MX403Q is prepared to either receive or transmit a digit sequence, the ROM ADDRESS lines are set to address the first ROM location (0001). Each received digit advances the address to the next location. But when transmitting or transponding the ROM ADDRESS lines are set to the 9th ROM location (1001) for the first digit and advanced sequentially until that sequence is complete. Detection of a coding error on the DATA INPUT, D0-D3 lines, during a receive sequence resets the ROM ADDRESS to the first digit select state (0001). If the transpond mode is selected detection of an appropriate HSC termination code (in a transmission that is free of the all or group call code "A") advances the ROM ADDRESS to the 9th digit 1001 position for the first digit of a transpond sequence. Detection of the hexadecimal "E" code on the input lines from the ROM (Dp0-Dp3) resets the ROM ADDRESS to the first ROM location (0001).
15,16, 17,18	**INPUTS FROM ROM, Dp0 through Dp3:** Dp0 is the least significant bit.
19	**TX CONTROL:** Quiescent state is at logic "0." Output goes HI in response to either a remotely requested transpond sequence or a local transmit command.
20	**Tx ENABLE I/O:** As an input an AC coupled logic "1" pulse of 40μS duration triggers a transmit sequence, unless the MX403Q is in the process of decoding an address — i.e. the input is not an "F" code or the TX CONTROL is already HI. As an output, the Tx ENABLE line latches HI when a transmit command is accepted. The BEEP OUTPUT resets if active. Output of the Tx ENABLE line is reset by an input from the ROM memory of a hex code "E."
21	**CALL OUTPUT:** By means of the CALL OUTPUT a call lamp may be latched or an audio circuit unmuted. The quiescent state is at Vss (logic "0"), active HI (Vdd).
22	**CALL RESET:** An input, responds to a logic "1" to reset both the CALL OUTPUT (pin 21) and BEEP OUTPUT (pin 7).
23	**Vdd**

FIG. 4: ADDRESS ALERT (WITHOUT DATA OR TRANSPOND)



MX403 PIN FUNCTION TABLE

PIN	FUNCTION/DESCRIPTION
24	**DATA FLAG:** Receipt of a valid discrete address with a "B" tone code appended switches the DATA FLAG output HI. This lags the data strobe which input "B" by typically 40μS, and it switches back to "0" following the data strobe for the first "F" code (NOTONE). Thus the data prefix code "B" and NOTONE code "F" act as boundary characters for the transmission of a data block. While the DATA FLAG remains true, a 40μS logic "1" pulse appears on the LOAD PULSE (pin 10) for each data character detected. This facilitates loading of data into associated display and memory circuits.
25,26, 27,28	**DATA INPUT, D0 through D3:** 4-Bit data inputs are presented on these lines as positive true binary numbers that include all decimal digits (0-9) as well as the hexadecimal suffix instruction code "B," the all and group call code "A," the repeat tone code "E," and the NOTONE "F." D0 is the least significant bit.

Programming the External Memory:

The first 8 locations of the external memory are used only in the decode mode. An address is first "written" into these locations for later comparison with a received code, in decoding a valid address. Addresses up to seven digits in length are permissible, and must be terminated with the hex code "E."

Codes to be transmitted are "written" into the ROM after location 8. Codes may contain up to seven digits, and must be terminated with the hex code "E."

When programming the ROM hex code "E" should not be used to indicate repeat of a digit. The memory should be programmed as written.

e.g. (i) Address Code 12345,
should be written as 12345E.
(ii) Address Code 12234.
should be written as 12234E.

In the transpond and transmit mode the MX403Q automatically steps to the 9th memory location and transmits the data stored there. To transmit HSC tones the MX403 should be connected to the MX503 as shown in the Circuit Connection Diagram above. Data to be encoded should be programmed beginning at address 9 and must be followed immediately by the "E" code (used in the ROM as an end of message code — i.e. it is not transmitted).

e.g. External
Memory 1 2 3 4 5 6 7 E 9 10 11 12 13 E 15 16
Locations
for decoding for encoding

FIG. 5: EXTERNAL MEMORY (ADDRESS MODE)

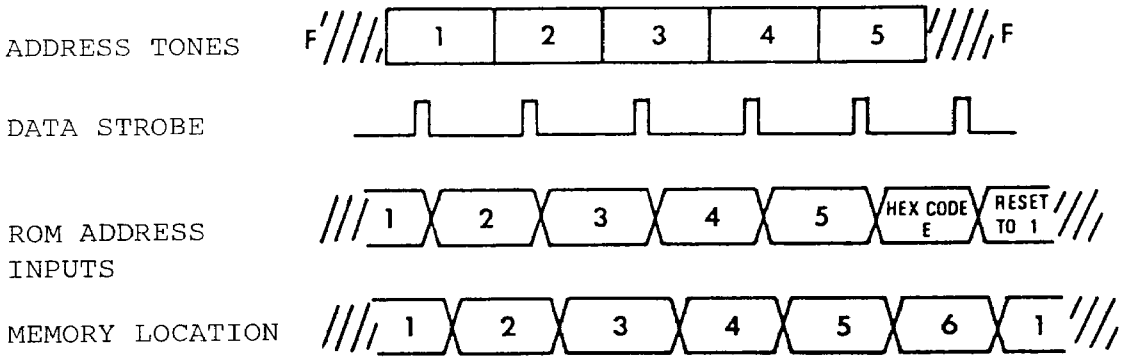
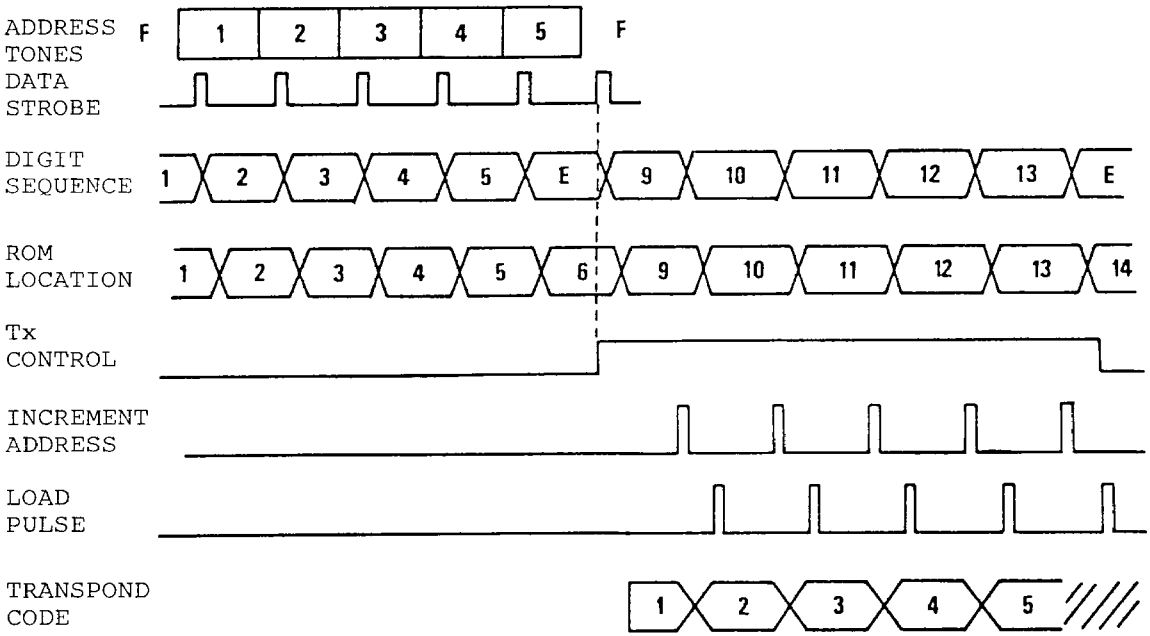


FIG. 6: EXTERNAL MEMORY (TRANSPOND MODE)



MX403 ELECTRICAL SPECIFICATIONS
(Vdd = 5V, Clock 23.3kHz, −30°C≤TA≤85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
Vdd	Supply Voltage, Vss = 0V	4.5	5	7	V	
Idd	Supply Current		100		μA	No Load
Voh	Logic Output Level "1"	4.5			V	1 source = 0.1mA pins 10,11,13, 14,19,21,24
Vol	Logic Output Level "0"			0.5	V	1 sink = 0.1mA
Vih	Logic Input Level "1"	3.5			V	pins 1,4,5,6,8, 15,16,17,18,22, 25,26,27,28
Vil	Logic Input Level "0"			1.5	V	
	Input Level to Activate pins 2,9,20		3.25		V	Schmitt trigger inputs
	Input Level to Deactivate pins 2,9		1.75			
	Internal Pull-down Impedance		30		KΩ	pin 4
	Internal Pull-up Impedance		12		KΩ	pin 20
∅	Clock Freq. Input to pin 8	10	23.33	35	kHz	(1)
Ta	Working Temperature	−30		+85	°C	
Tstg	Storage Temperature	−55		+125	°C	

(1) Alert frequency, pattern timing and logic sequences are directly related to clock frequency.