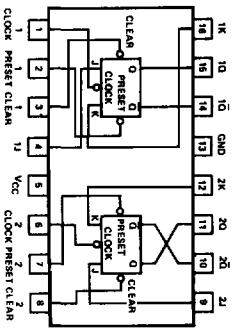
SPEED/PACKAGE AVAILABILITY

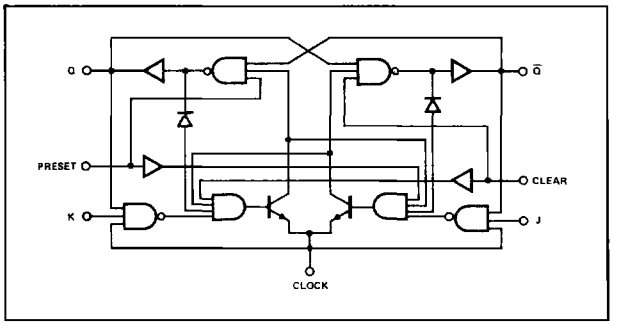
54H F,W 74H B,F

PIN CONFIGURATION

B,F,W PACKAGE



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74H C_L=25pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			40	50		MHz
$t_{w(Clock)}$	Width of clock pulse						
	High level			10			ns
	Low Level			15			
$t_{w(Clear)}$	Width of clear pulse			16			ns
t_{Setup}	Input setup time						
	Data high			10			ns
	Data low			13			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Preset			8	12	ns
t_{PHL}	High-to-low						
	Clock low				23	35	
	Clock high				15	20	
t_{PLH}	Low-to-high	Clock		5	10	15	
t_{PHL}	High-to-low			8	16	20	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse.
2. t_n+1 = bit time after clock pulse.

LOGIC