Signetics

54F398, 54F399
Registers

54F398 – Quad 2-Port Register w/ True & Complementary Outputs
54F399 – Quad 2-Port Register

Product Specification

Military FAST Products

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge-triggered operation**
- **Both True and Complementary outputs – 54F398**

DESCRIPTION

The 54F398 and 54F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 54F399 is the 16-pin version of the 54F398, with only the Q outputs of the flip-flops available.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F398/BRA 54F399/BEA
Ceramic Flat Pack	54F398/BSA 54F399/BFA
Ceramic LLCC	54F398/B2A 54F399/B2A

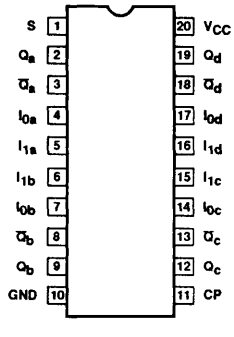
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a} - I_{0d}	Data inputs from source 0	1.0/1.0	20μA/0.6mA
I_{1a} - I_{1d}	Data inputs from source 1	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q_a - Q_d	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a$ - $\overline{Q}_d$	Register complementary outputs (54F398)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

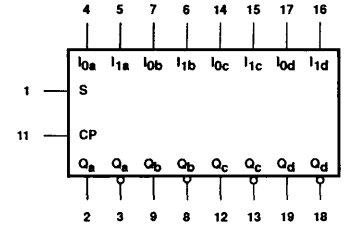
54F398



For LLCC pin assignments, see JEDEC Standard No. 2

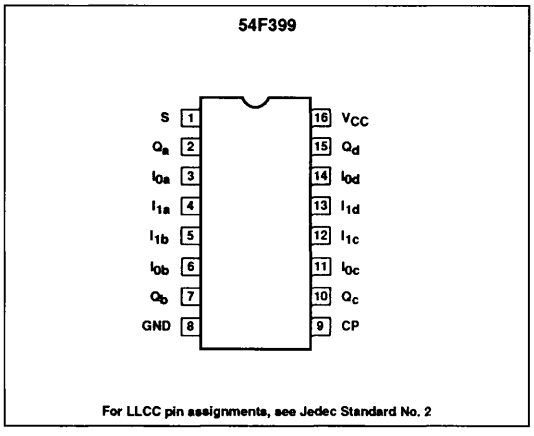
LOGIC SYMBOL

54F398

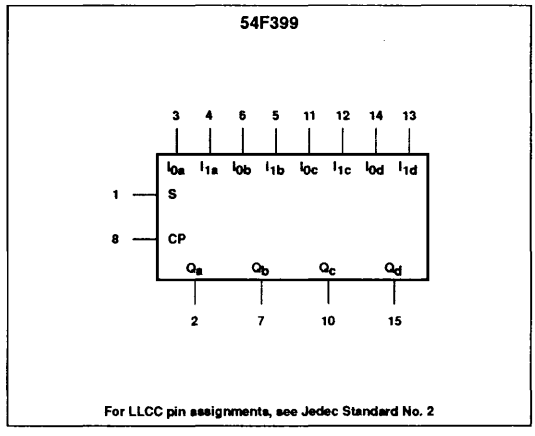


For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION



LOGIC SYMBOL



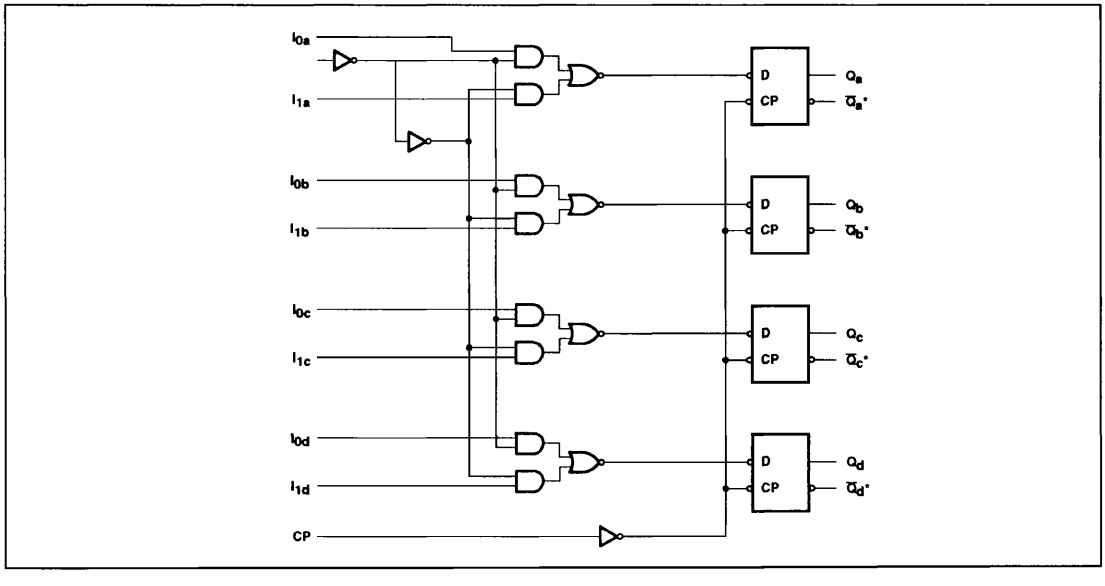
The 54F398 and 54F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a set-up time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 54F398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*54F398 only
l = Low voltage level one setup time prior to Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
H = High voltage level
X = Don't care

LOGIC DIAGRAM (54F398 only)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)	54F398	V_{CC} = Max		25	38	mA
		54F399			22	34	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

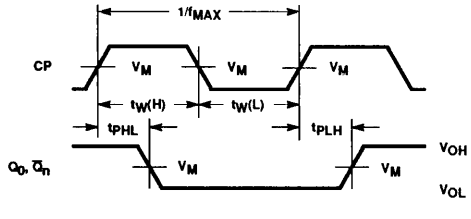
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q or $\overline{Q}$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	9.5 10.5	ns ns

AC SETUP REQUIREMENTS

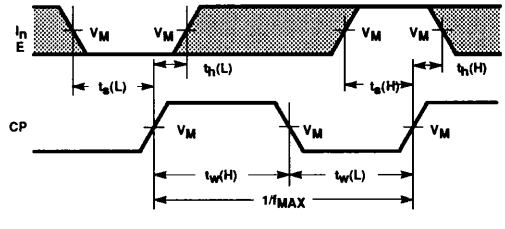
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low I_n to CP	Waveform 2	3.0 3.0			4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_n to CP	Waveform 2	1..0 1.0			1.5 1.5		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low S to CP	Waveform 2	7.5 7.5			10.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 6.0			4.0 7.0		ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS} the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.
4. V_{IN} = High; apply 3V, 0V, 3V to CP then make measurement.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



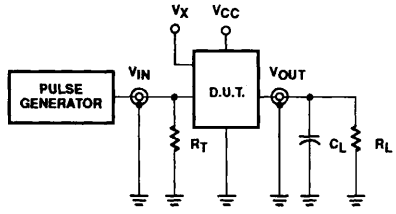
Waveform 1. Clock to Output Delays and Clock Pulse Width



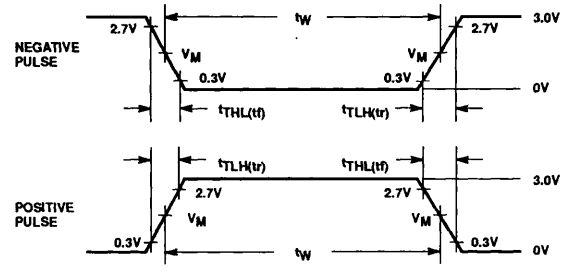
Waveform 2. Data Setup and Hold Times

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns