

# SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS595G – OCTOBER 1997 – REVISED SEPTEMBER 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW) Packages, and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

## description

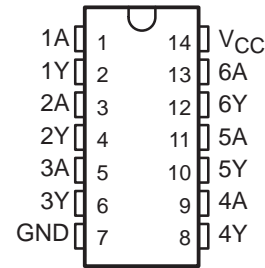
These hex buffers/drivers are designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The outputs of the 'LVC07A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

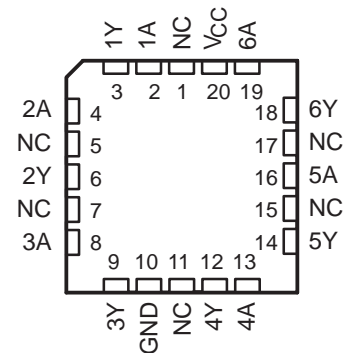
Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of these devices as translators in a mixed-system environment.

The SN54LVC07A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVC07A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54LVC07A . . . J OR W PACKAGE  
SN74LVC07A . . . D, DGV, OR PW PACKAGE  
(TOP VIEW)



SN54LVC07A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L



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 **TEXAS  
INSTRUMENTS**

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## recommended operating conditions (see Note 3)

		SN54LVC07A		SN74LVC07A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	1.65	5.5	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2		
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	5.5	0	5.5	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4		mA
		V <sub>CC</sub> = 2.3 V		12		
		V <sub>CC</sub> = 2.7 V		12		
		V <sub>CC</sub> = 3 V		24		
		V <sub>CC</sub> = 4.5 V		24		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC07A			SN74LVC07A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.2			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45			0.45	
		2.3 V			0.7			0.7	
	I <sub>OL</sub> = 12 mA	2.7 V			0.4			0.4	
		3 V			0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5			±5	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0						±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5			5	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

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**SN54LVC07A, SN74LVC07A**  
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC07A										UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

switching characteristics over recommended operating free-air temperature range, (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC07A										UNIT
			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

operating characteristics,  $T_A = 25^\circ\text{C}$

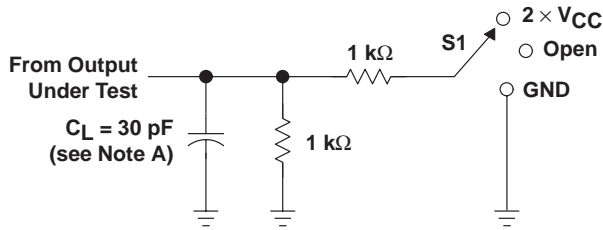
PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance per buffer/driver	$f = 10\text{ MHz}$	1.8	2	2.5	3.78	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



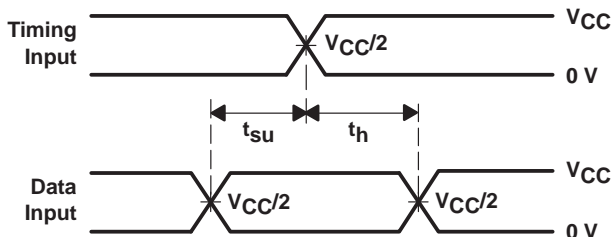
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

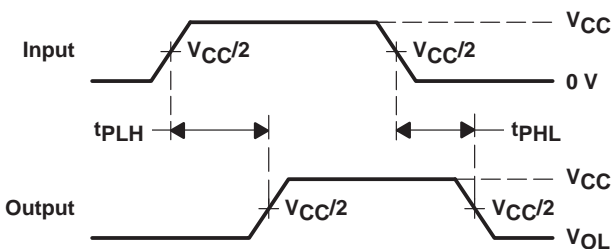


LOAD CIRCUIT

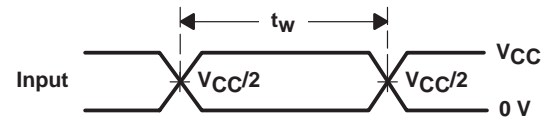
TEST	S1
$t_{pZL}$ (see Note F)	2 $\times$ $V_{CC}$
$t_{pLZ}$ (see Note G)	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	2 $\times$ $V_{CC}$



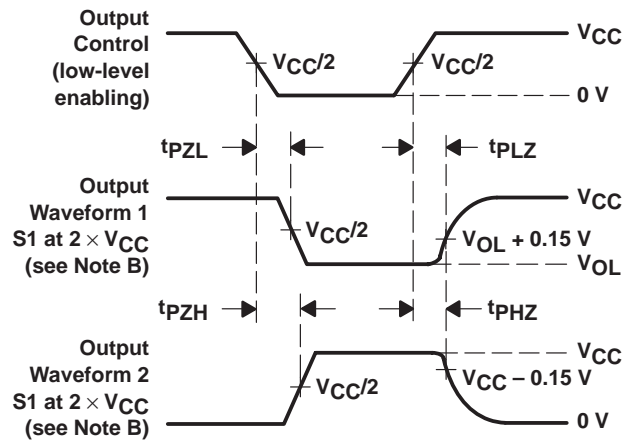
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{pZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .

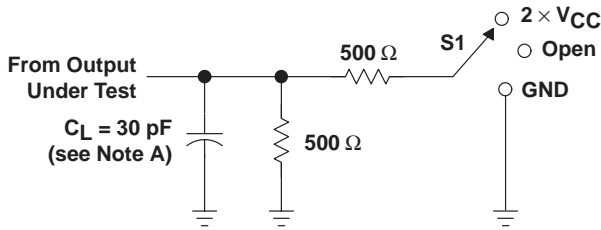
Figure 1. Load Circuit and Voltage Waveforms

**SN54LVC07A, SN74LVC07A**  
**HEX BUFFERS/DRIVERS**  
**WITH OPEN-DRAIN OUTPUTS**

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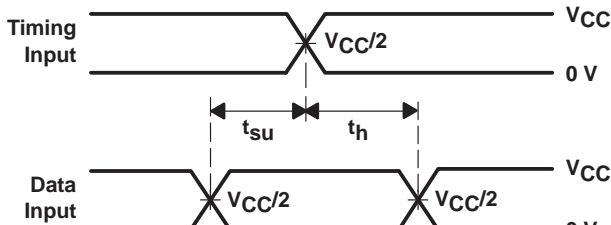
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

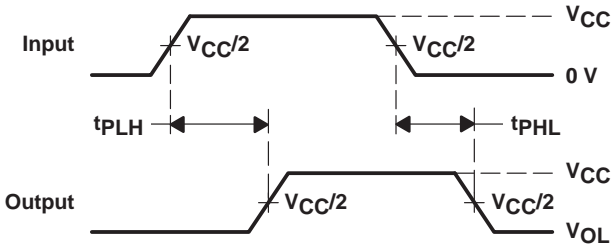


**LOAD CIRCUIT**

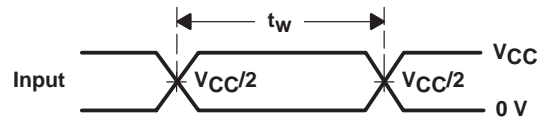
TEST	S1
$t_{pZL}$ (see Note F)	2 $\times V_{CC}$
$t_{pLZ}$ (see Note G)	2 $\times V_{CC}$
$t_{PHZ}/t_{PHZ}$	2 $\times V_{CC}$



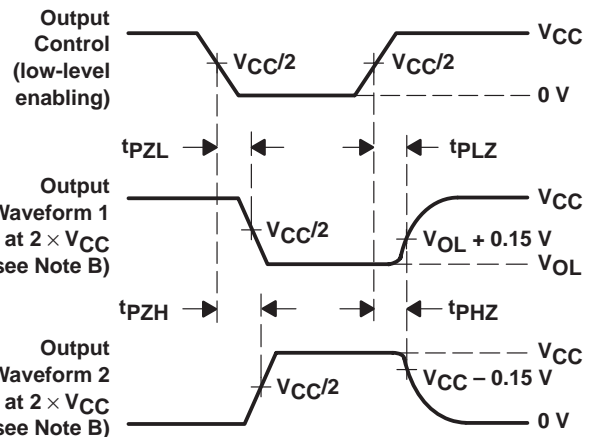
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



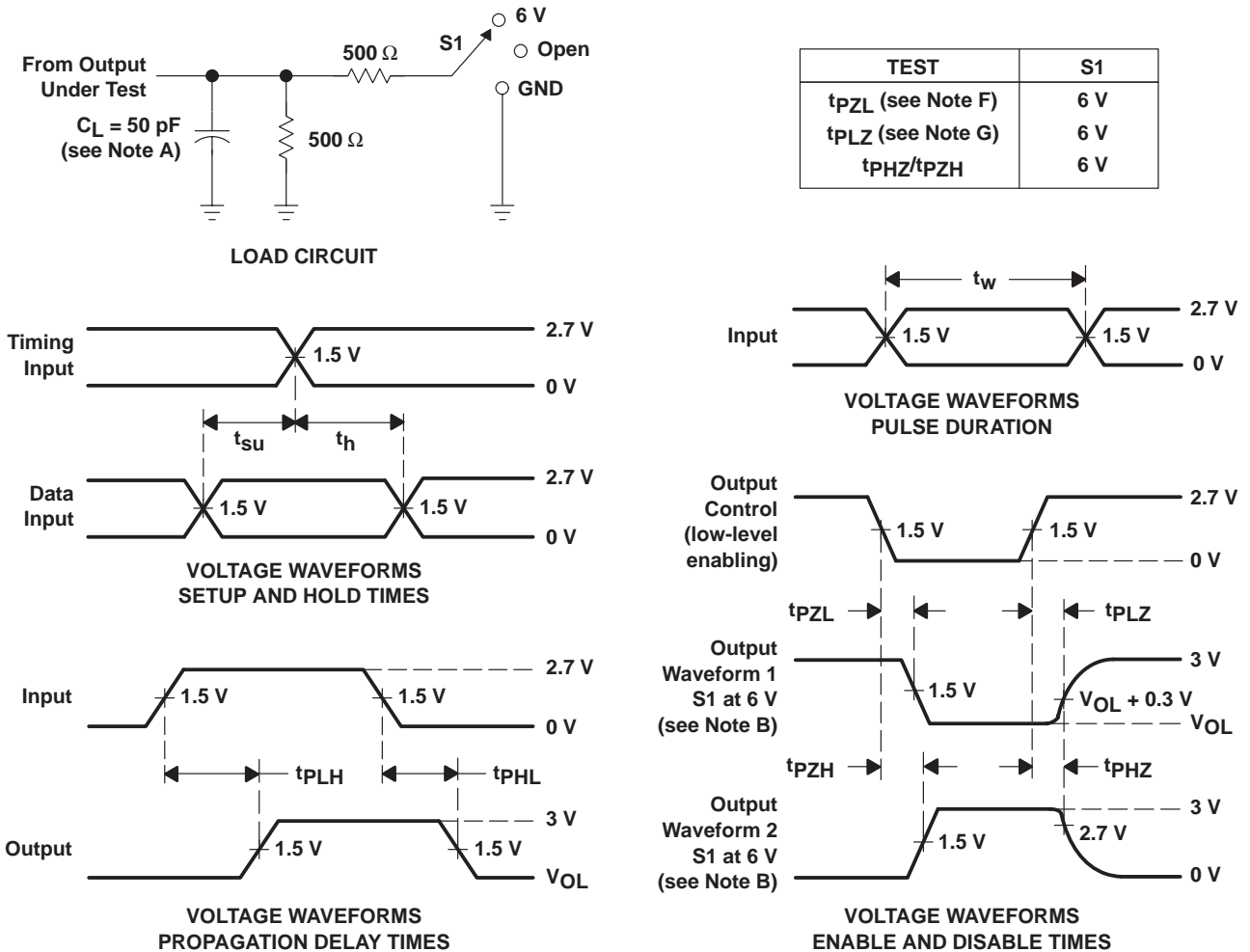
**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .
  - F.  $t_{pZL}$  is measured at  $V_{CC}/2$ .
  - G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ AND } 3.3 \text{ V} \pm 0.3 \text{ V}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{PZL}$  is measured at 1.5 V.  
 G.  $t_{PLZ}$  is measured at  $V_{OL} + 0.3 \text{ V}$ .

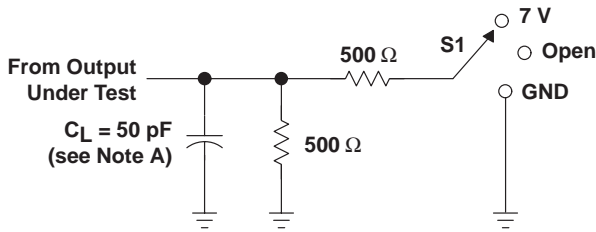
Figure 3. Load Circuit and Voltage Waveforms

**SN54LVC07A, SN74LVC07A**  
**HEX BUFFERS/DRIVERS**  
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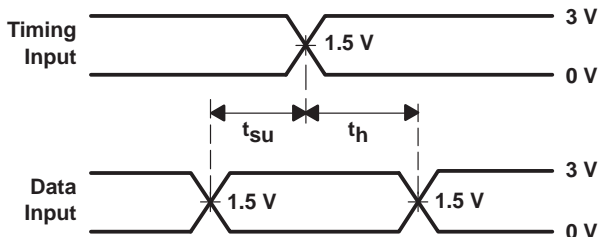
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

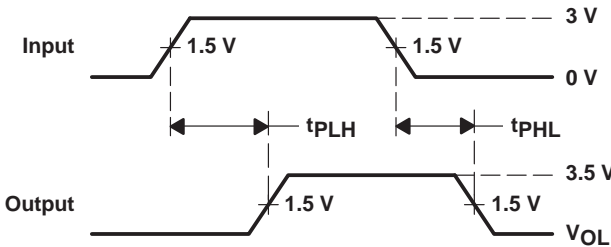


**LOAD CIRCUIT**

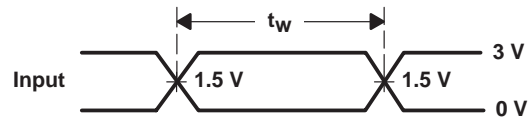
TEST	S1
$t_{pZL}$ (see Note F)	7 V
$t_{pLZ}$ (see Note G)	7 V
$t_{PHZ}/t_{PZH}$	7 V



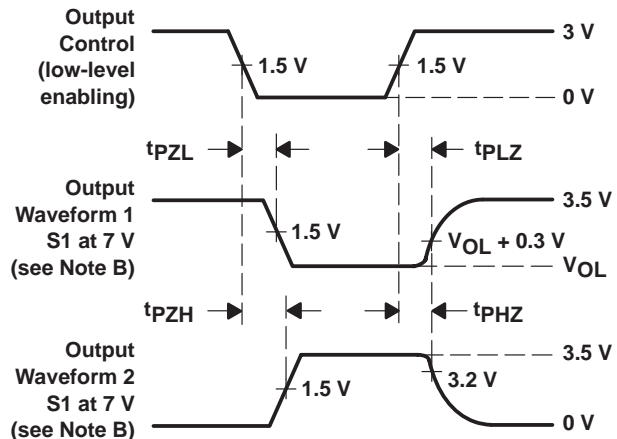
**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .
  - F.  $t_{pZL}$  is measured at 1.5 V.
  - G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.3\text{ V}$ .

**Figure 4. Load Circuit and Voltage Waveforms**

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