1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416V1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416V1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416V1200A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **1024 cycle/16ms (Normal)**
  - **1024 cycle/128ms (L-version)**
  - **1024 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

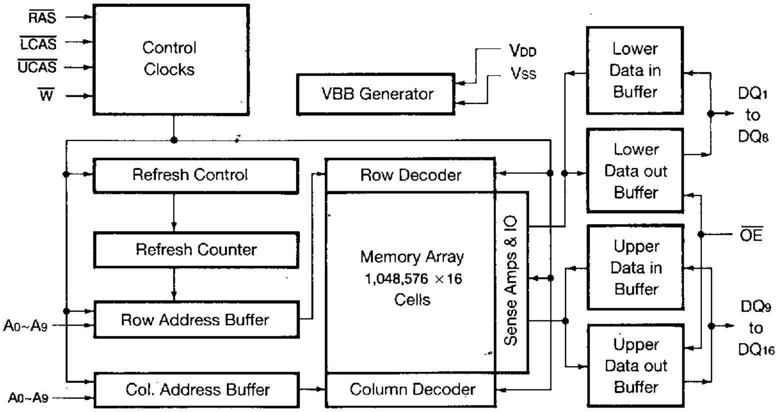
GENERAL DESCRIPTION

The Samsung KM416V1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

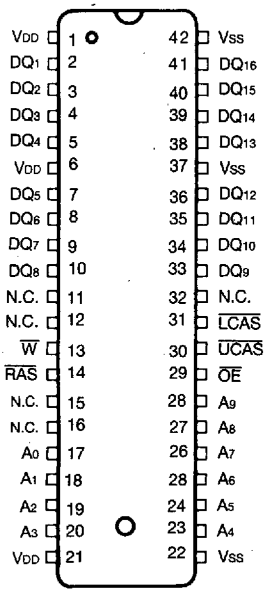
The KM416V1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



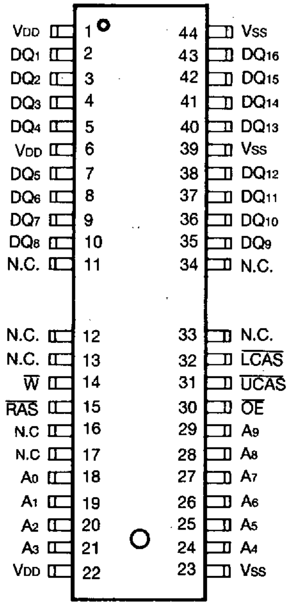
PIN CONFIGURATION (Top Views)

• KM416V1200AJ



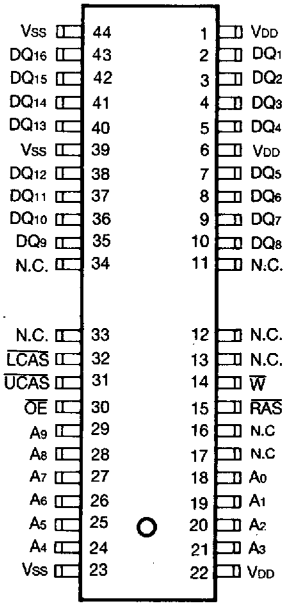
(SOJ)

• KM416V1200AT



(TSOP(II)-Forword)

• KM416V1200AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-16}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{DD}	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to+150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I_{CC1}	-	150 140 130	mA mA mA
Standby Current ($\overline{\text{RAS}}$=$\overline{\text{UCAS}}$=$\overline{\text{LCAS}}$=$\overline{\text{W}}$=V_{IH})	KM416V1200A KM416V1200A-L KM416V1200A-F	I_{CC2}	-	2 1 1	mA mA mA
$\overline{\text{RAS}}$-Only Refresh Current* ($\overline{\text{UCAS}}$=$\overline{\text{LCAS}}$=V_{IH}, $\overline{\text{RAS}}$, Address Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I_{CC3}	-	150 140 130	mA mA mA
Fast Page Mode Current* ($\overline{\text{RAS}}$=V_{IL}, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @t_{PC}=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I_{CC4}	-	100 90 80	mA mA mA
Standby Current ($\overline{\text{RAS}}$=$\overline{\text{UCAS}}$=$\overline{\text{LCAS}}$=$\overline{\text{W}}$=V_{DD}-0.2V)	KM416V1200A KM416V1200A-L KM416V1200A-F	I_{CC5}	-	1 300 200	mA µA µA
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ Cycling @t_{RC}=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I_{CC6}	-	150 140 130	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$= 0.2V D_{IN}=Don't Care, t_{RC}=125µs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416V1200A-L	I_{CC7}	-	350	µA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=0.2V$ $\overline{W}=\overline{OE}=A_0\text{-}A_9=V_{DD}\text{-}0.2V$ or 0.2V $DQ_1\text{-}DQ_{16}=V_{DD}\text{-}0.2V$ or 0.2V or Open	KM416V1200A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, Address can be changed maximum once while page mode cycle time t_{PC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_9)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{DD}=3.3V \pm 0.3V$, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15		15		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	45		55		60		ns	6
Refresh period (Normal)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (F-version)	t_{REF}		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t_{CPWD}	60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	80		95		100		ns	
$\overline{\text{RAS}}$ pulse eidth (Fast page mode)	t_{RASP}	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	t_{ROH}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

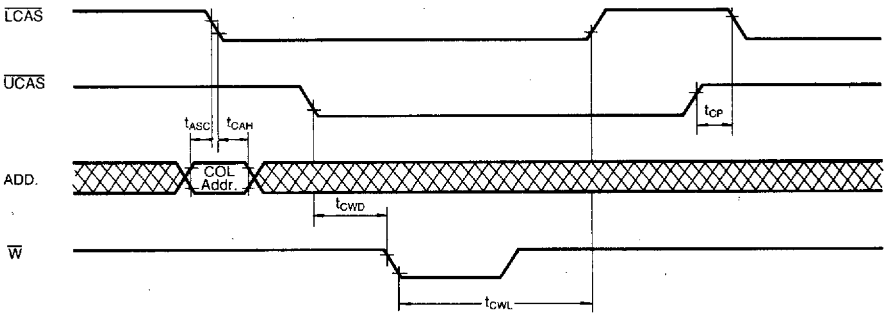
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{OE}}$ access time	t_{OEA}		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	t_{OEH}	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width (F-ver)	t_{RASS}	100		100		100		μs	19
$\overline{\text{RAS}}$ precharge time (F-ver)	t_{RPS}	110		130		150		ns	19
$\overline{\text{CAS}}$ hlod time (F-ver)	t_{CHS}	-50		-50		-50		ns	19

KM416V1200A/A-L/A-F Truth Table

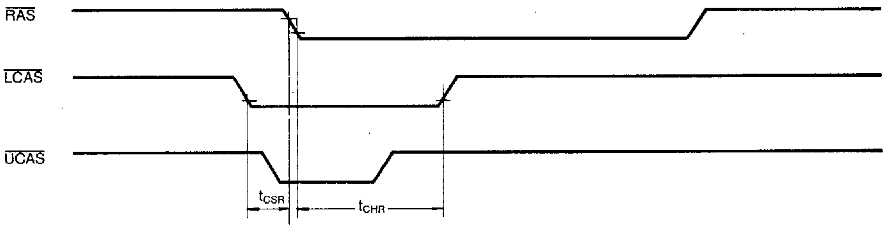
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

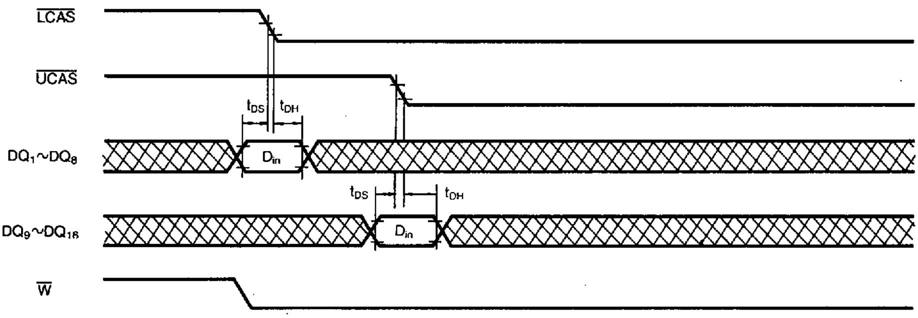
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geqslant t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating apremeters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geqslant t_{CWD(min)}$; $t_{RWD} \geqslant t_{RWD(min)}$, $t_{AWD} \geqslant t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

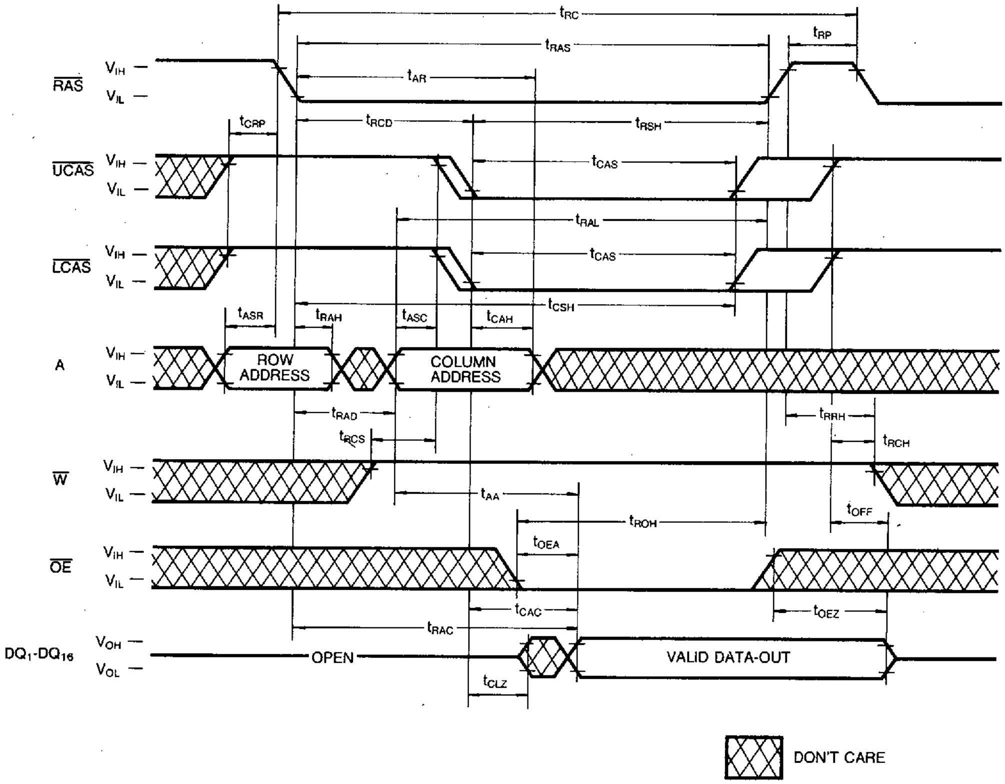


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$.



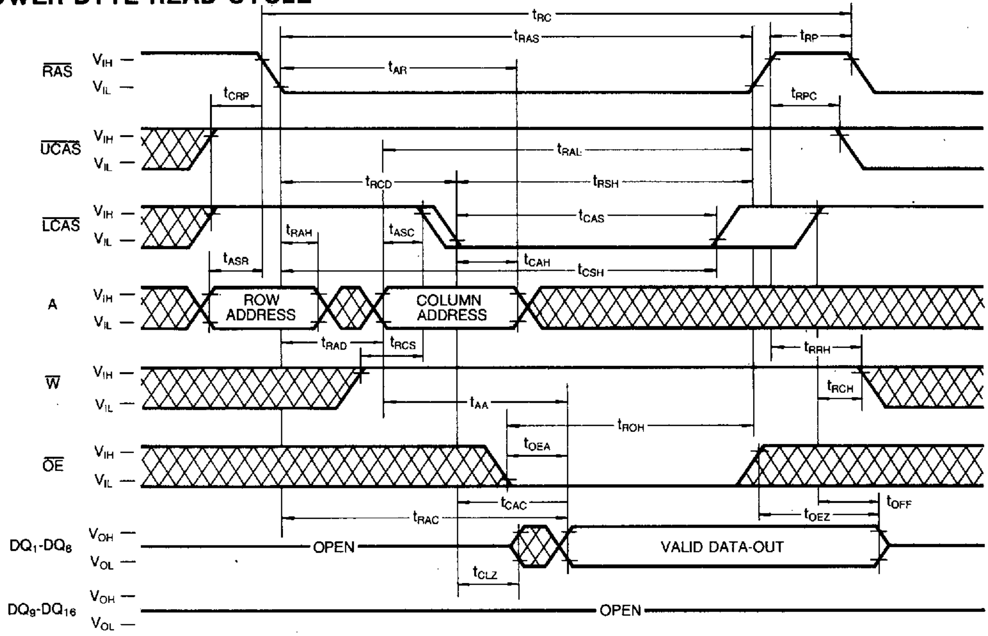
TIMING DIAGRAMS

WORD READ CYCLE

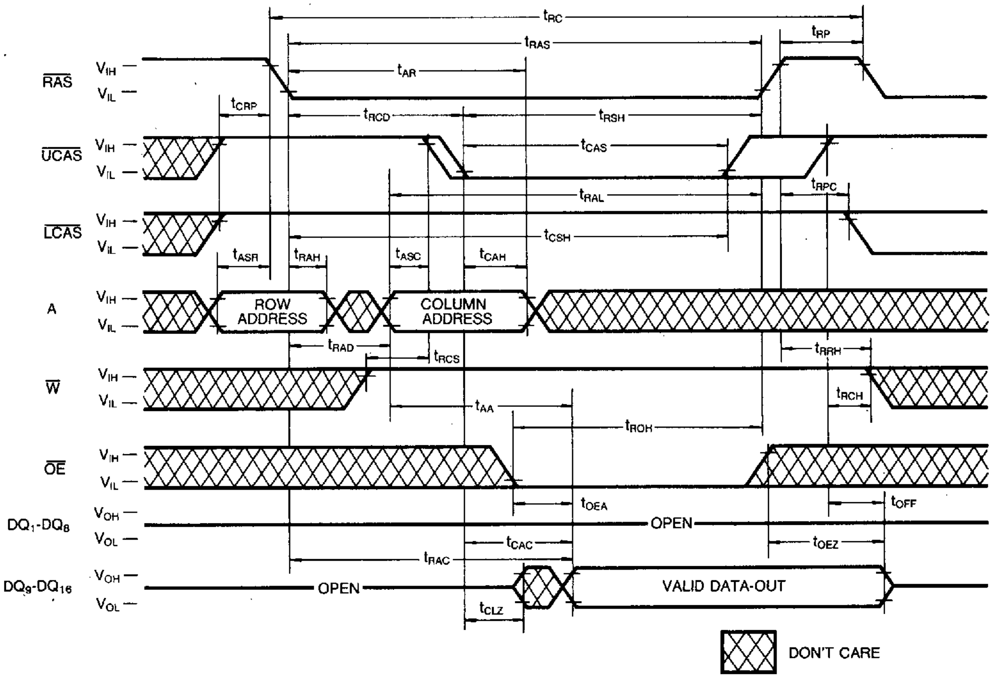


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

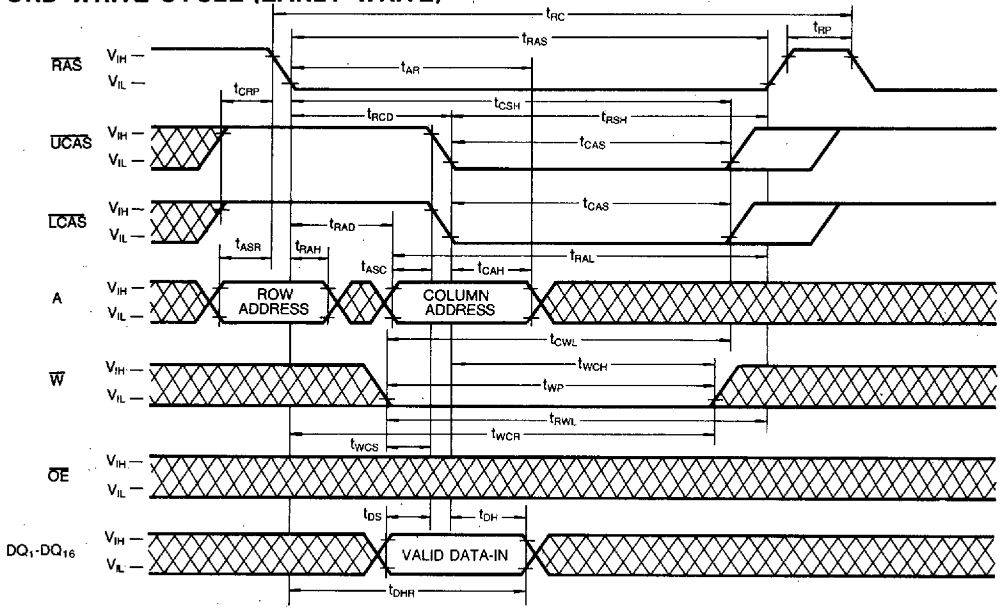


UPPER BYTE READ CYCLE

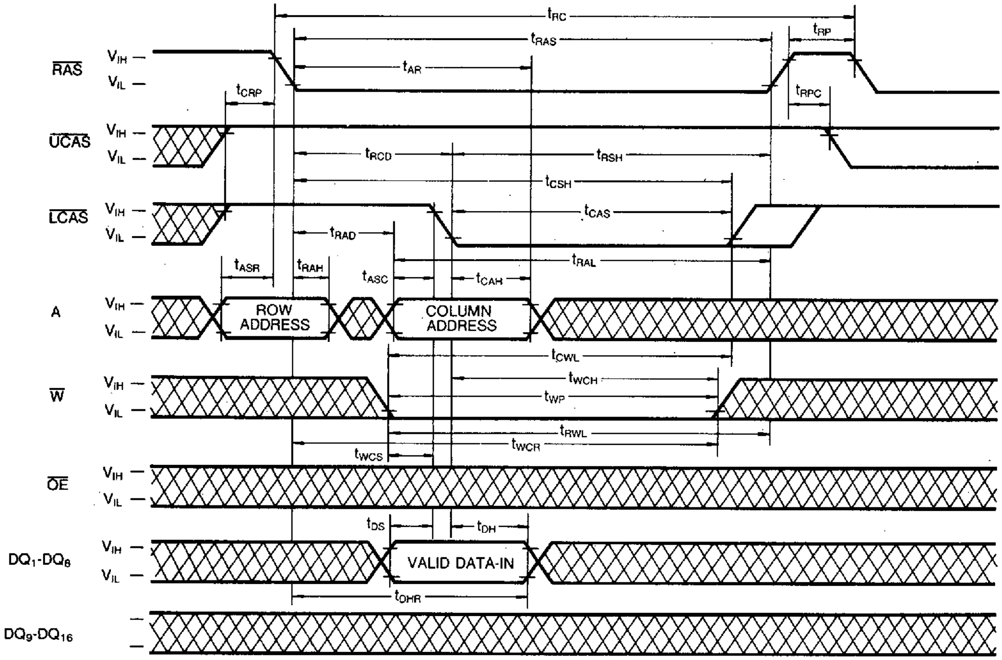


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



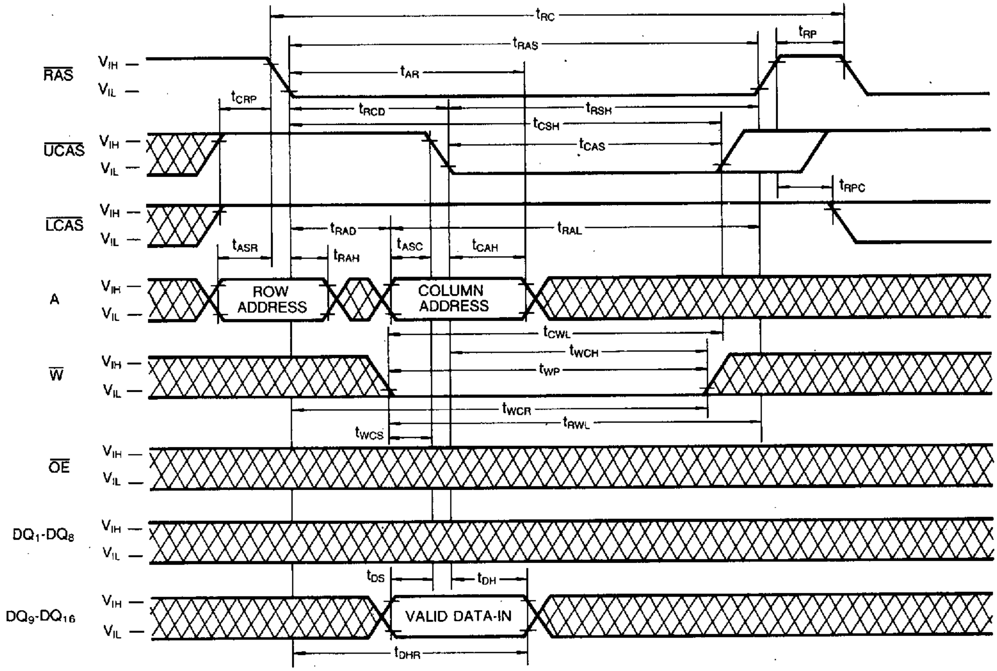
LOWER BYTE WRITE CYCLE (EARLY WRITE)



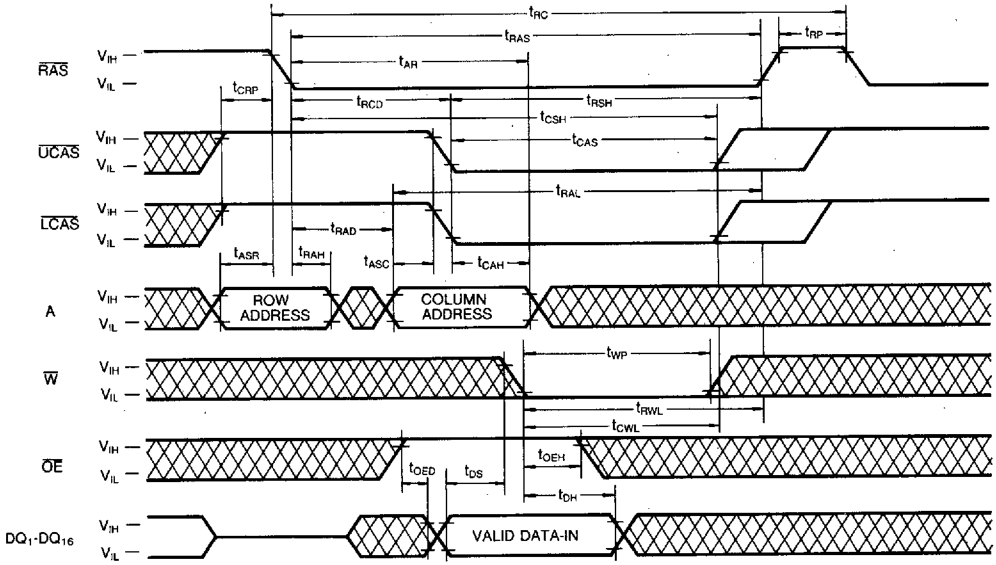
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



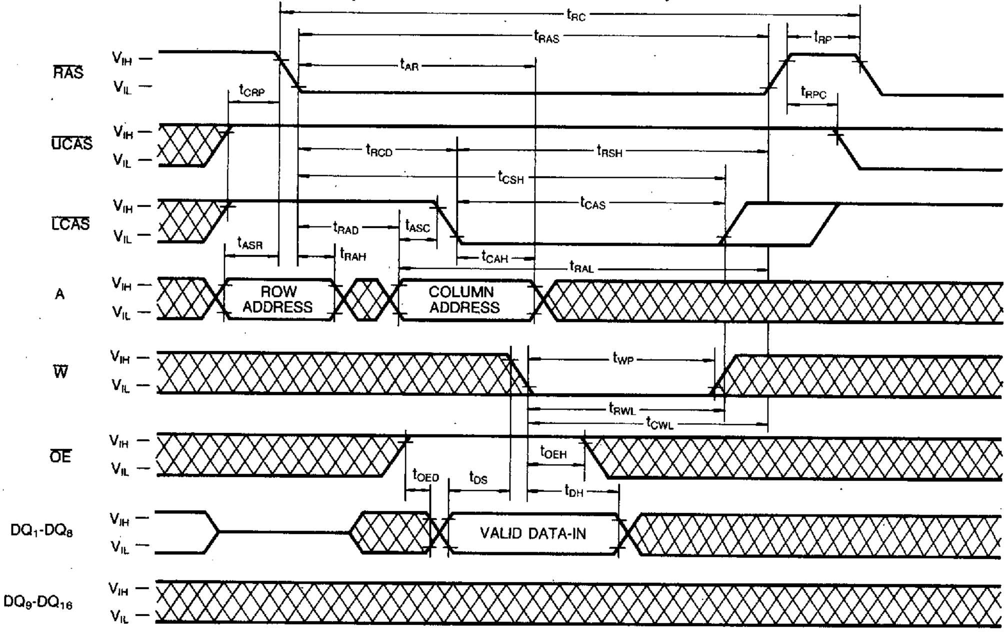
WORD WRITE CYCLE (OE CONTROLLED WRITE)



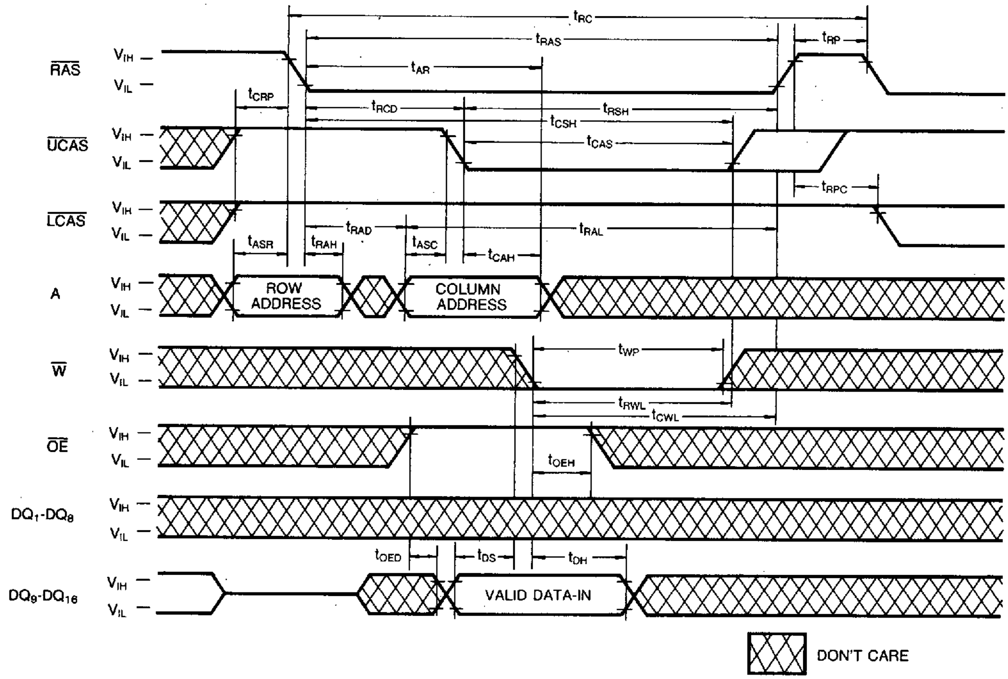
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

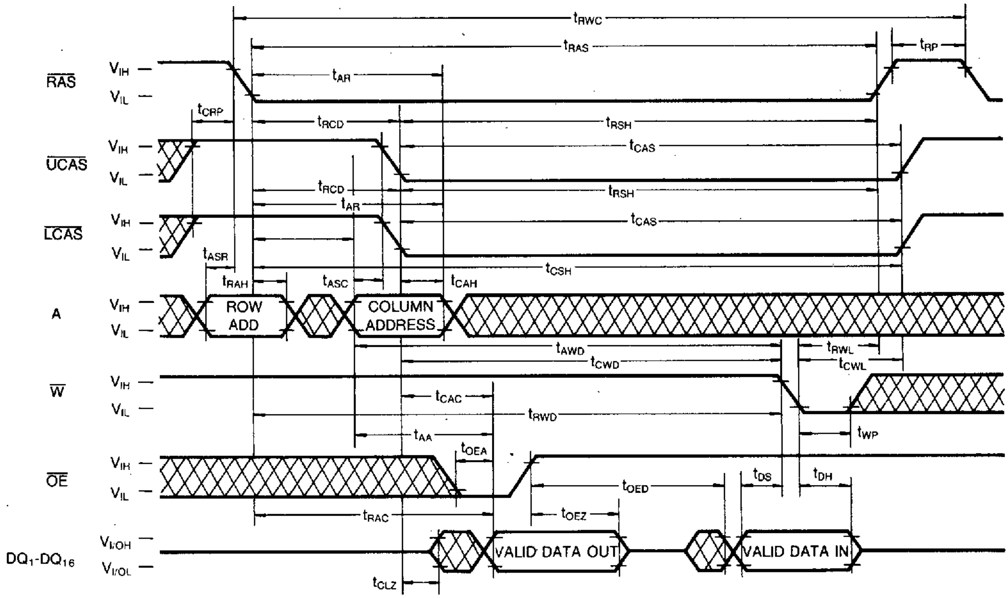


UPPER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

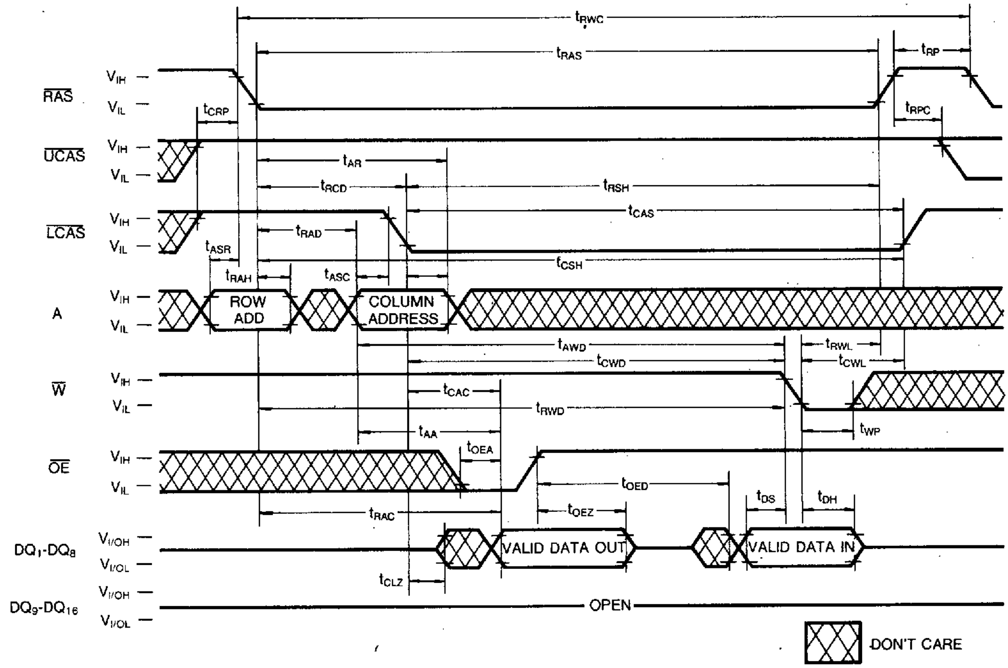


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

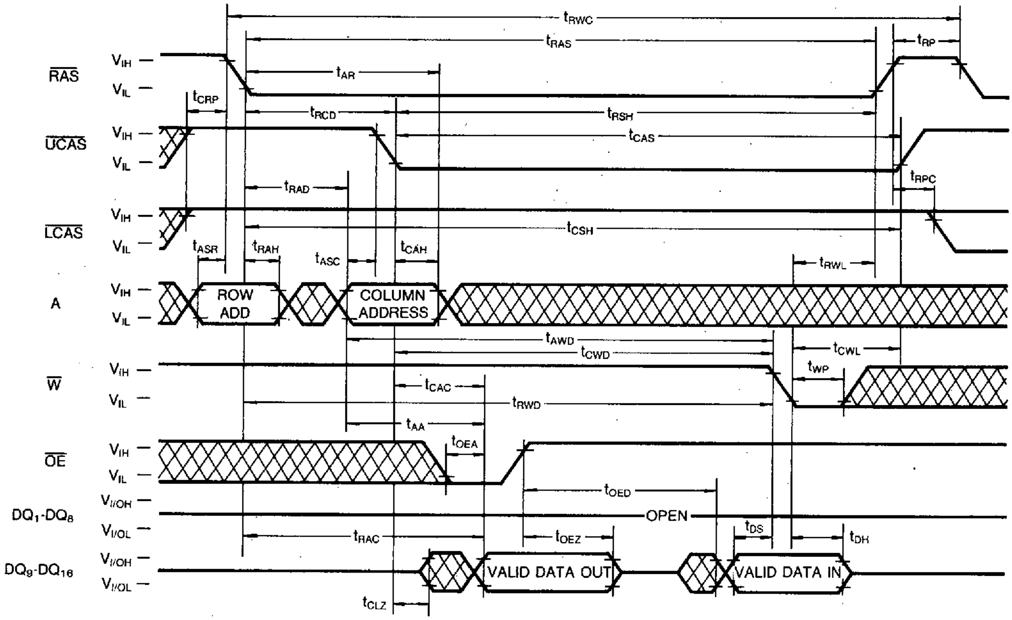


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

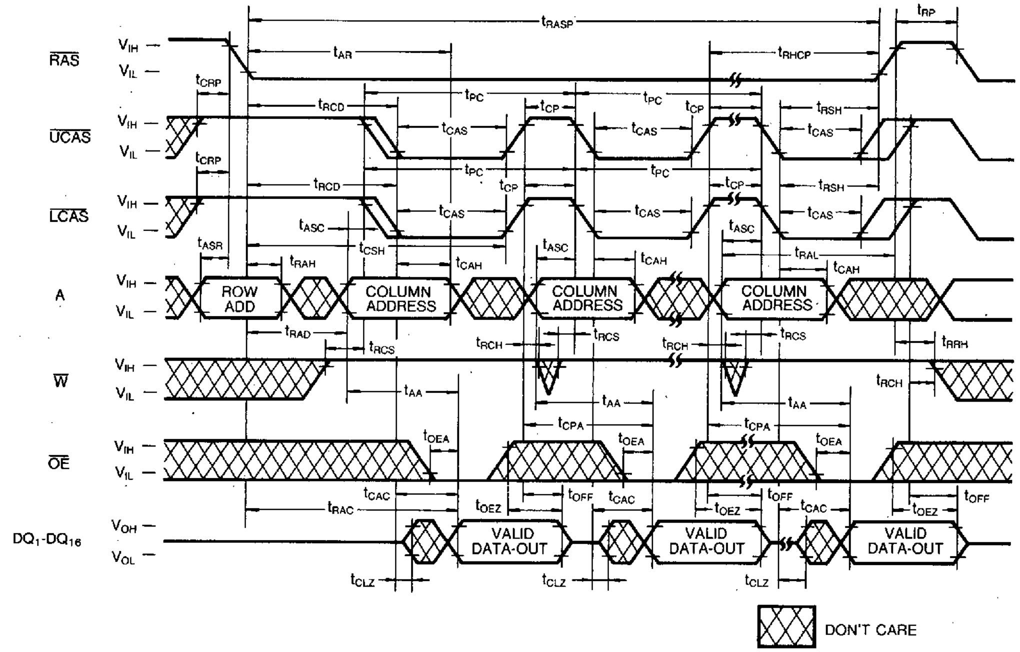


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

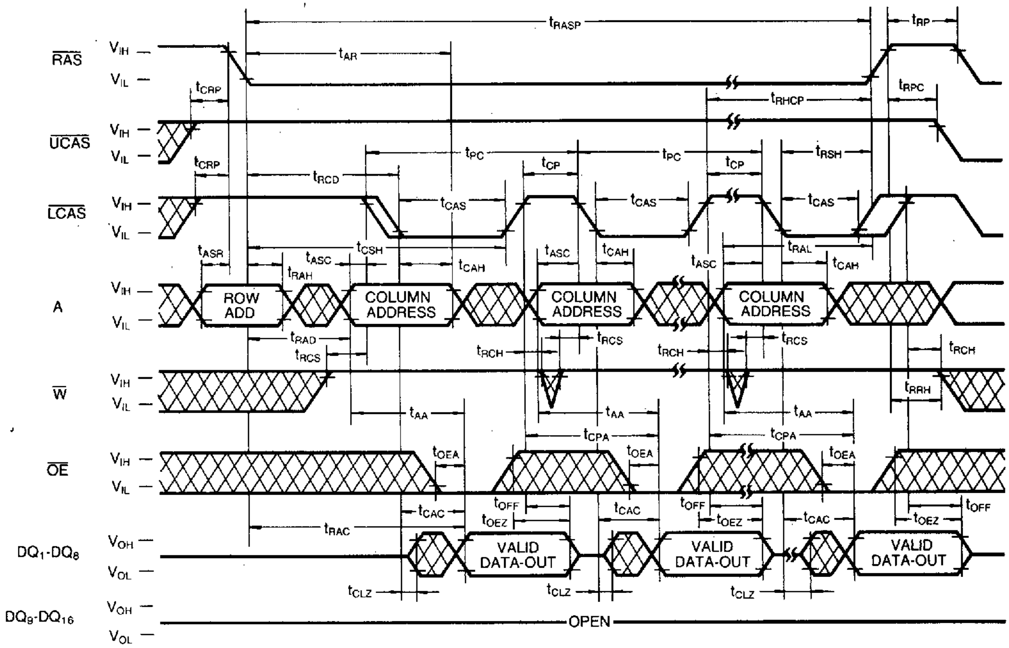


FAST PAGE MODE WORD READ CYCLE

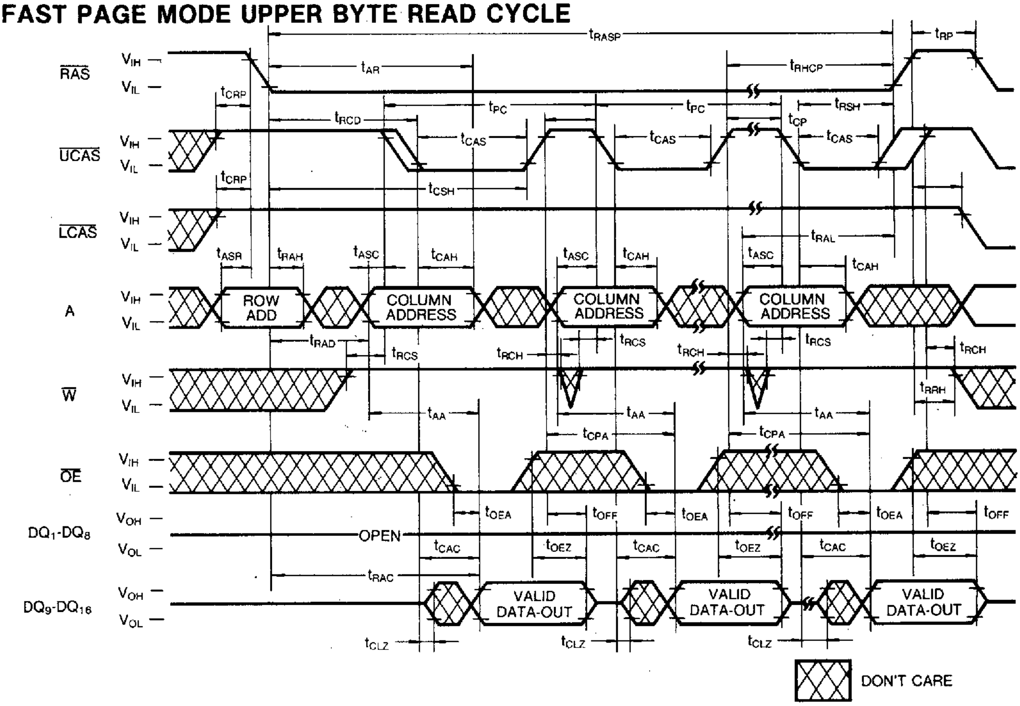


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

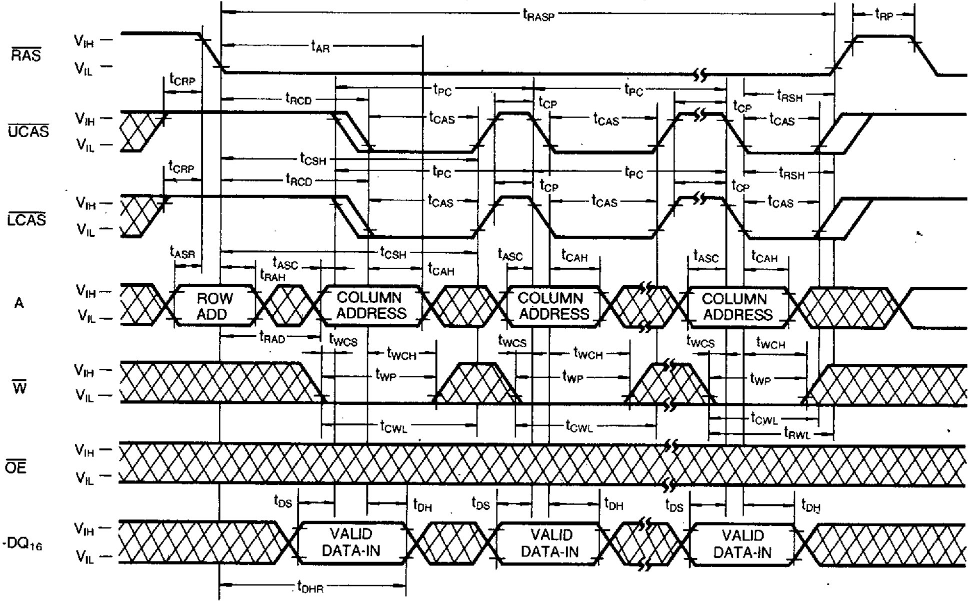


FAST PAGE MODE UPPER BYTE READ CYCLE

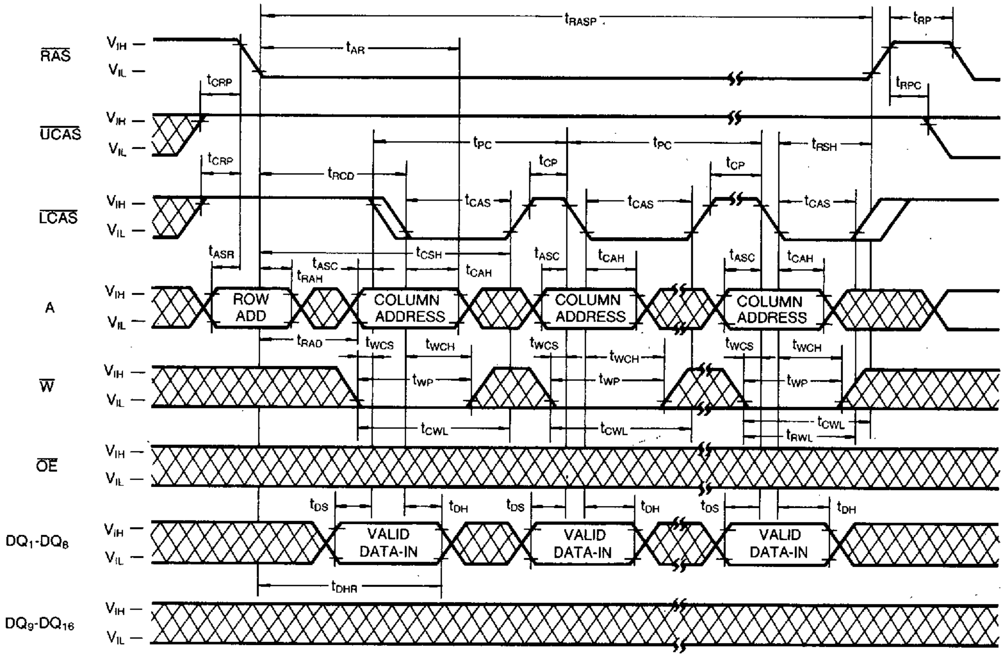


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



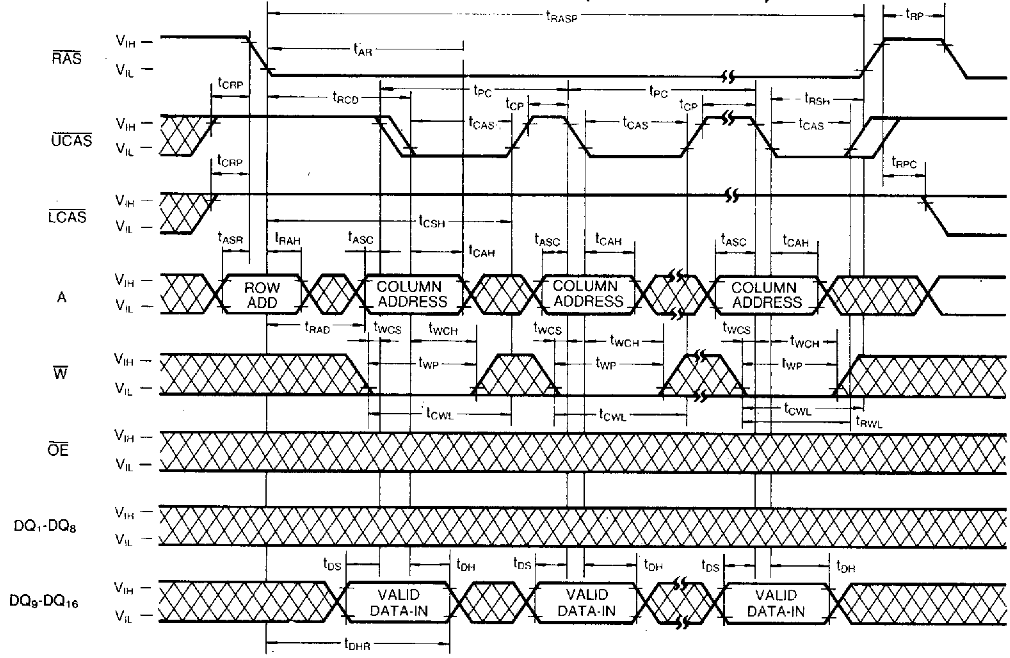
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



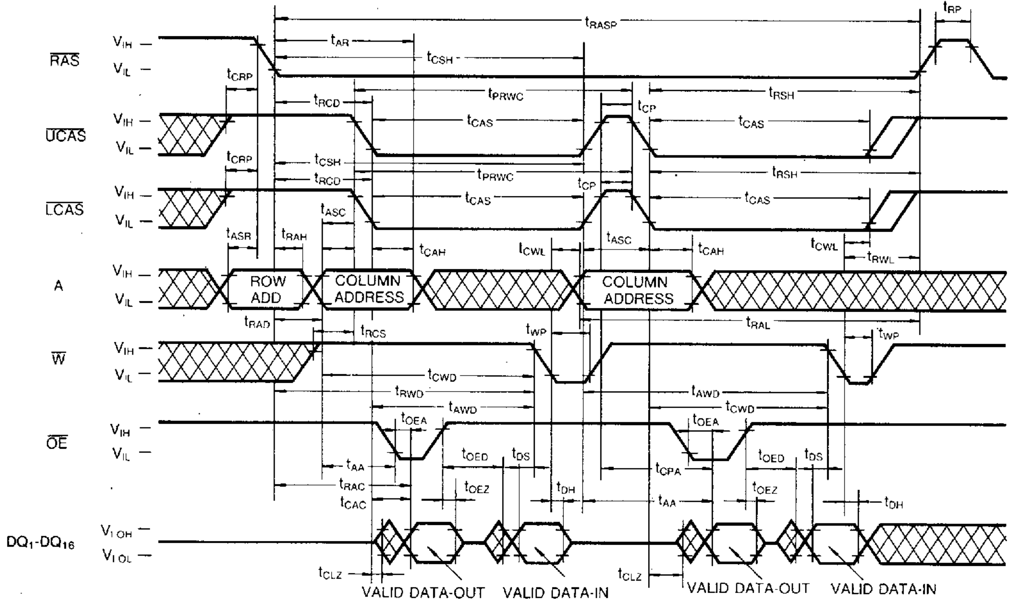
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



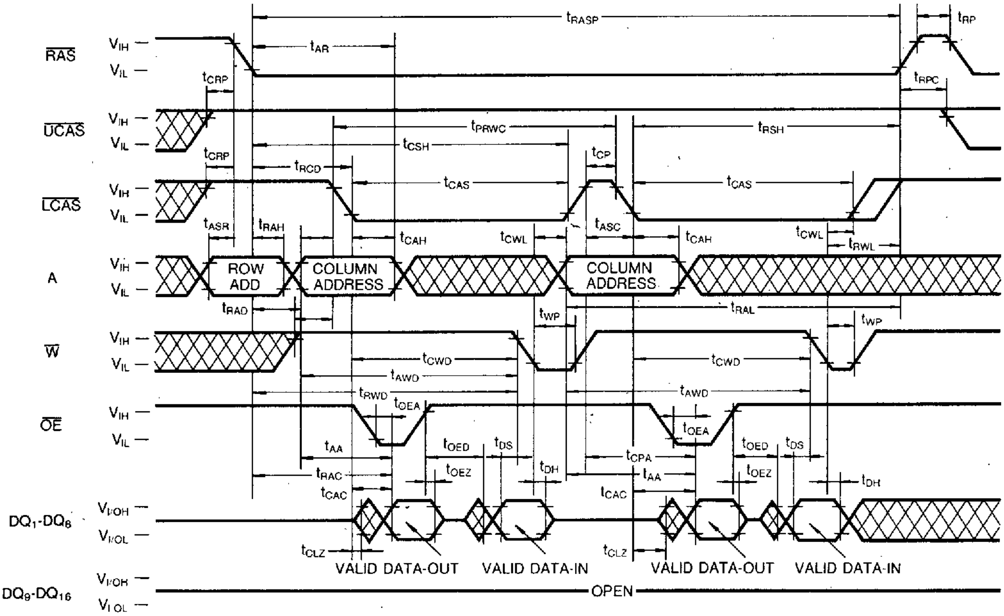
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



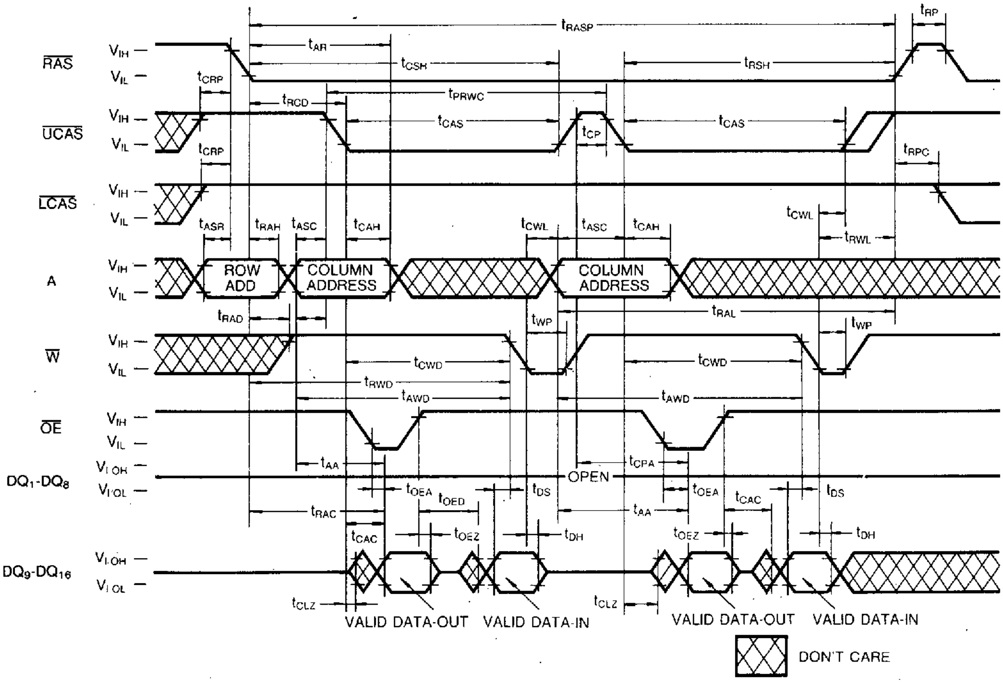
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



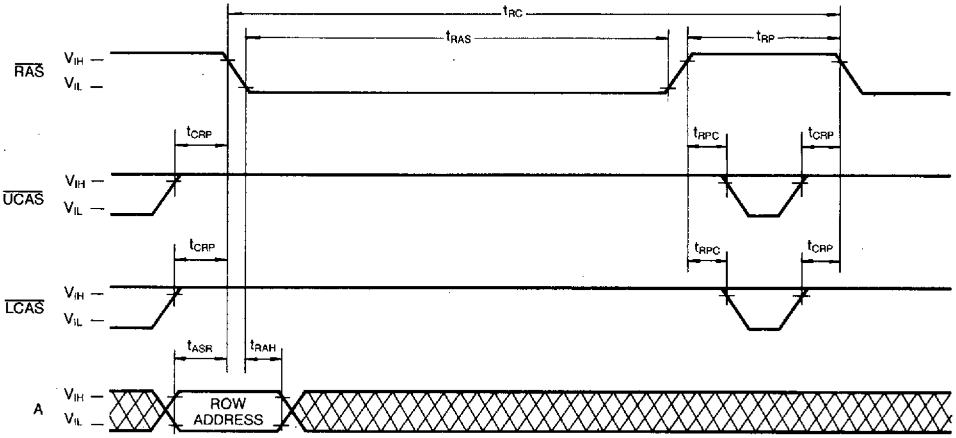
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

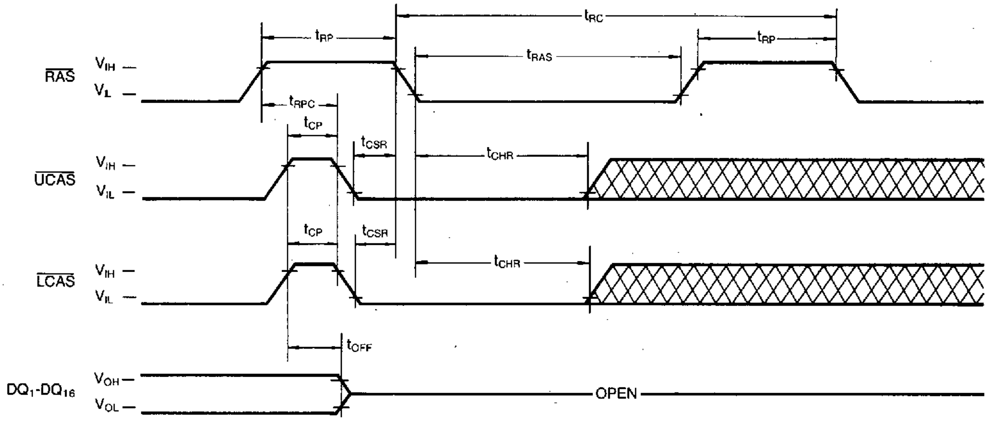
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

NOTE: $\overline{\text{W}}$, $\overline{\text{OE}}$=Don't Care



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

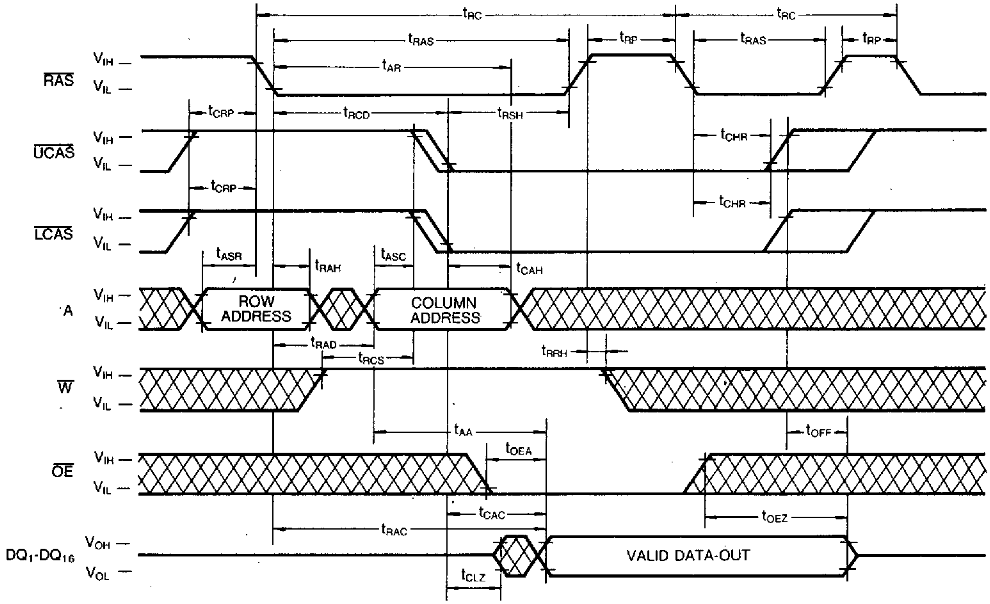
NOTE: $\overline{\text{W}}$=V_{IH}, $\overline{\text{OE}}$, A=Don't Care



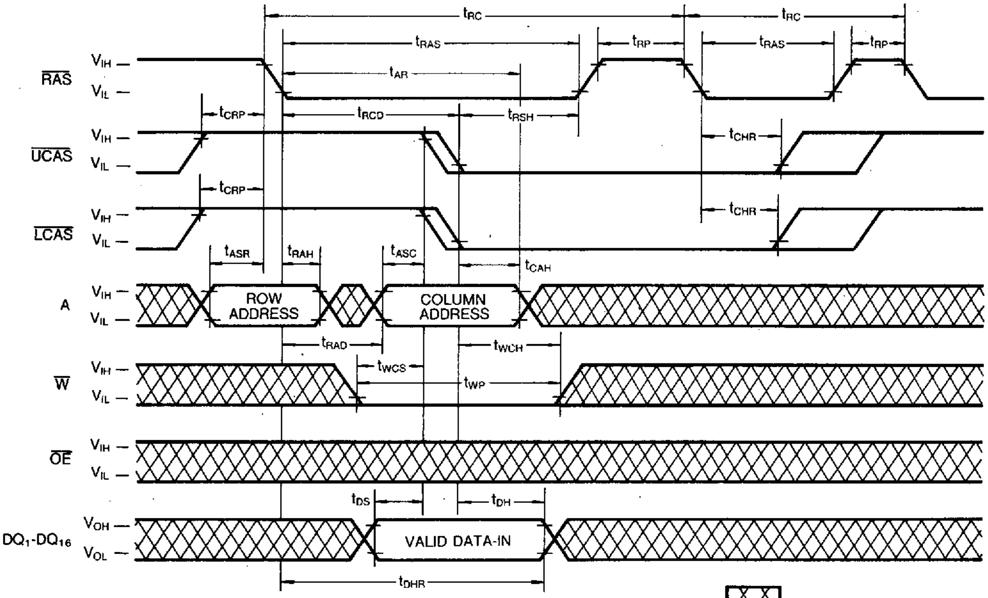
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



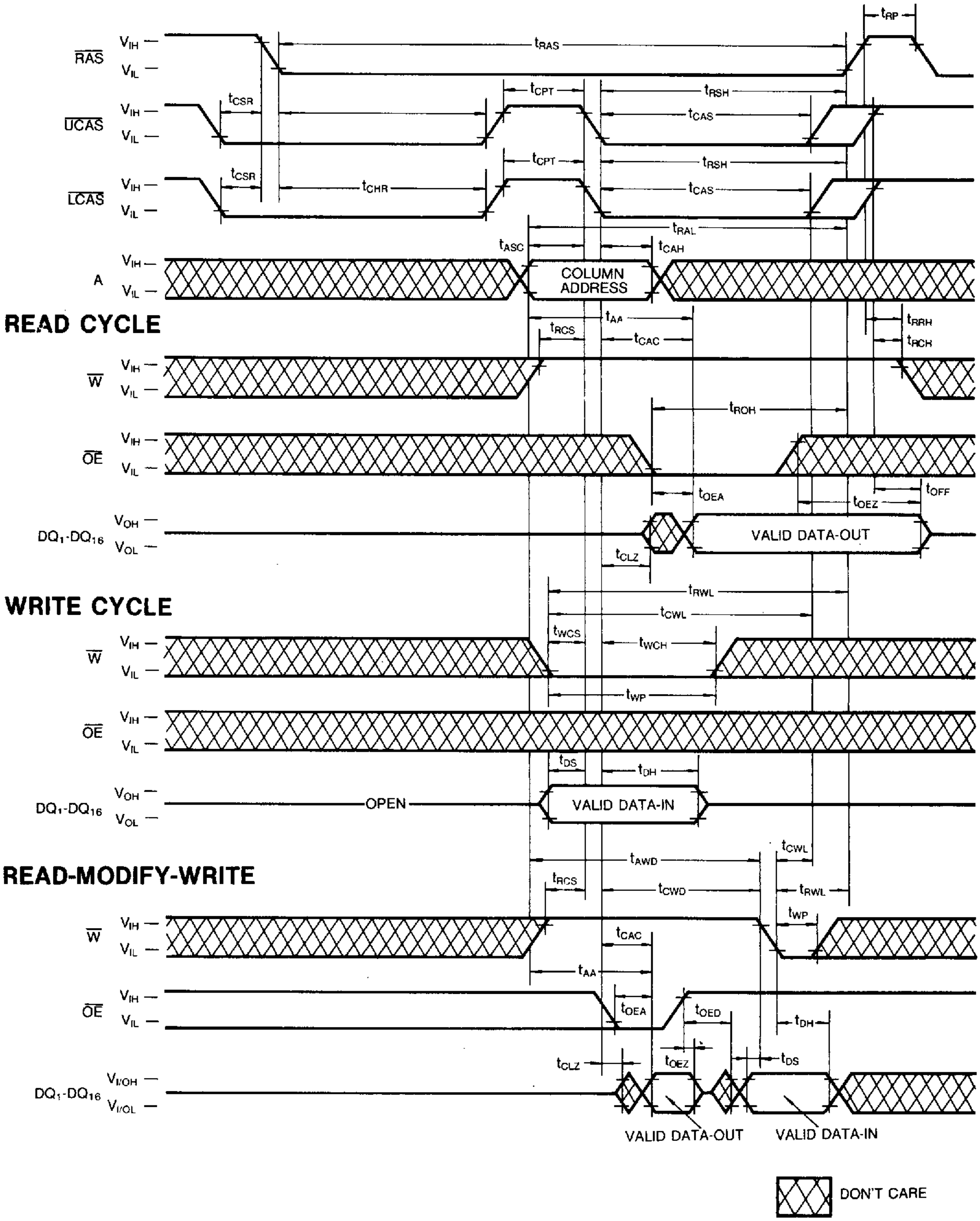
HIDDEN REFRESH CYCLE (WRITE)



▨ DON'T CARE

TIMING DIAGRAMS (Continued)

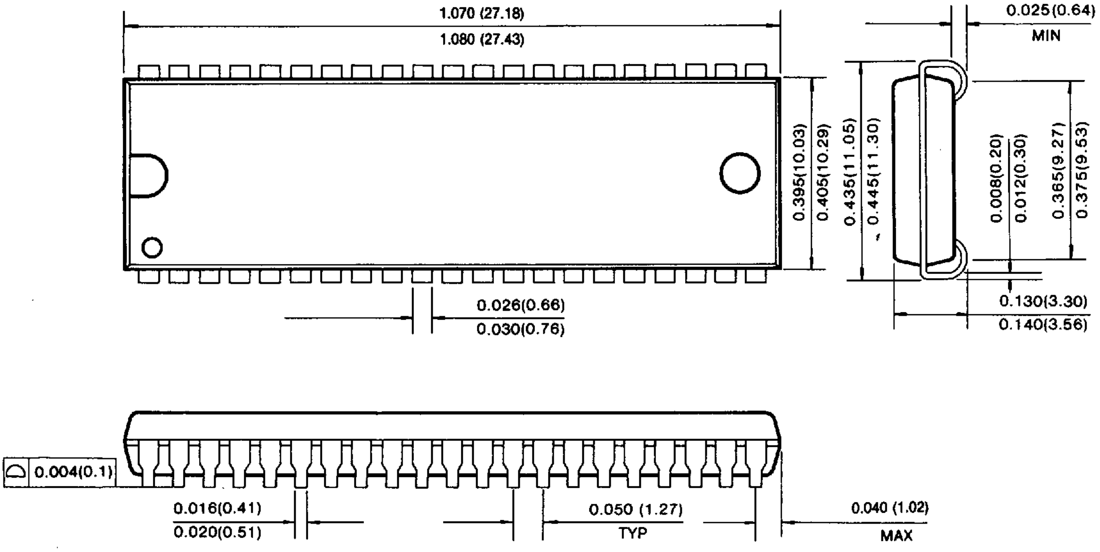
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)