

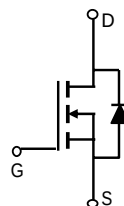
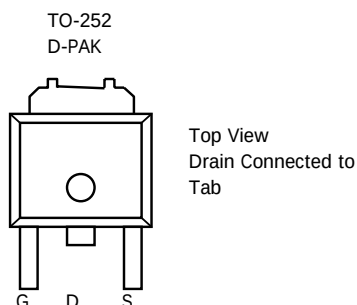
AOD454Y
N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOD454Y uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. *Standard product AOD454Y is Pb free, inside and out. It uses Pb-free die attach and plating material(meets ROHS & Sony 259 specifications). AOD454YL is a Green Product ordering option. AOD454Y and AOD454YL are electrically identical.*

Features

V_{DS} (V) = 40V
 I_D = 12 A (V_{GS} = 10V)
 $R_{DS(ON)} < 33 \text{ m}\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 47 \text{ m}\Omega$ (V_{GS} = 4.5V)


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	12	A
$T_C=25^\circ\text{C}$		12	
$T_C=100^\circ\text{C}$	I_{DM}	30	
Pulsed Drain Current ^C	I_{AR}	12	A
Avalanche Current ^C	E_{AR}	20	mJ
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	P_D	20	W
$T_C=25^\circ\text{C}$		10	
$T_C=100^\circ\text{C}$	P_{DSM}	2	W
$T_A=25^\circ\text{C}$		1.3	
$T_A=70^\circ\text{C}$			
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	17.4	30	$^\circ\text{C/W}$
$t \leq 10\text{s}$		50	60	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case ^B				

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$, $V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^{\circ}\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2.3	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=12\text{A}$		25	33	$\text{m}\Omega$
		$T_J=125^{\circ}\text{C}$		39	52	
		$V_{GS}=4.5\text{V}$, $I_D=6\text{A}$		34	47	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=12\text{A}$		25		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$		404		pF
C_{oss}	Output Capacitance			95		pF
C_{rss}	Reverse Transfer Capacitance			37		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.7		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=12\text{A}$		9.2		nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.5		nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=1.7\Omega$, $R_{GEN}=3\Omega$		3.5		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			13.2		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		22.9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=12\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		18.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300 \mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^{\circ}\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The SOA curve provides a single pulse rating.

Rev 0: Oct. 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

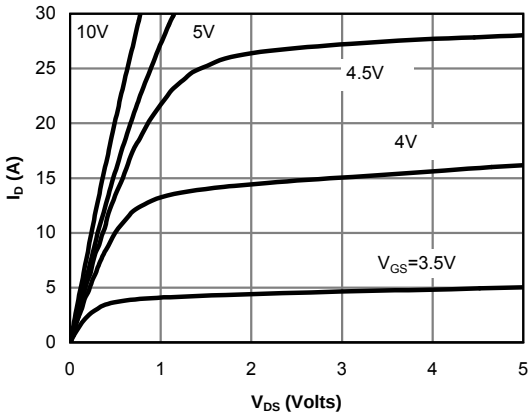


Fig 1: On-Region Characteristics

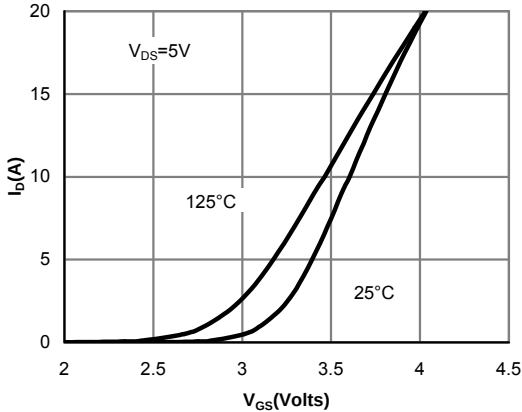


Figure 2: Transfer Characteristics

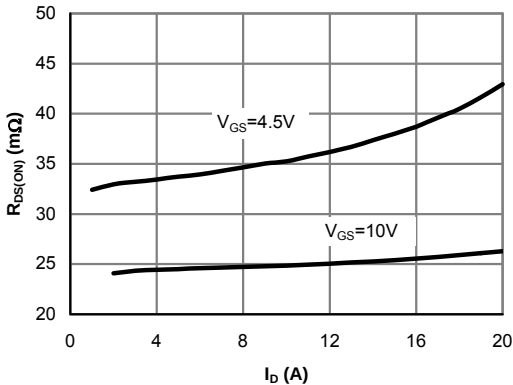


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

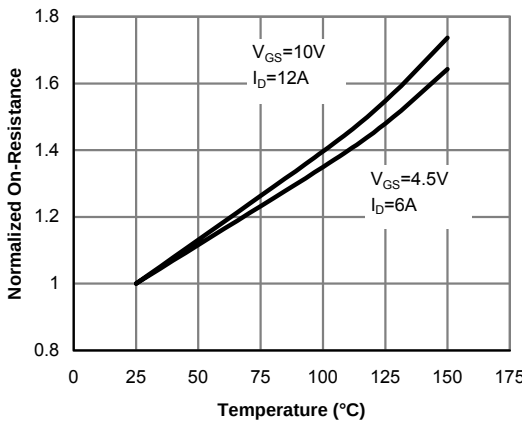


Figure 4: On-Resistance vs. Junction Temperature

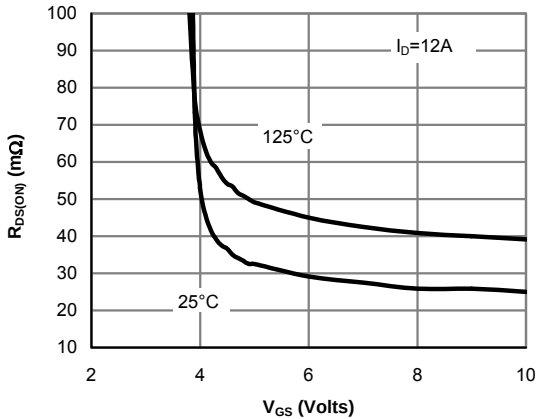


Figure 5: On-Resistance vs. Gate-Source Voltage

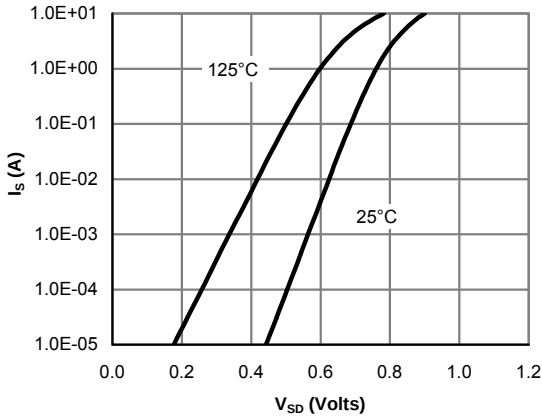


Figure 6: Body-Diode Characteristics

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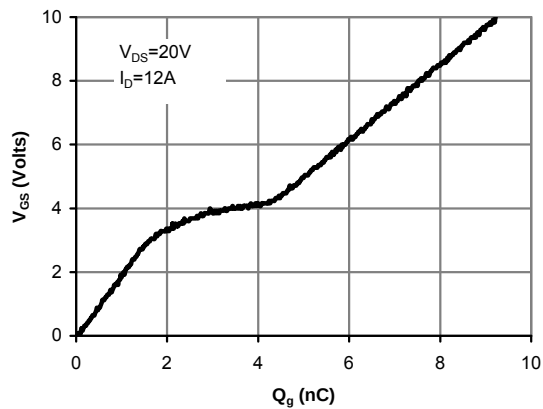


Figure 7: Gate-Charge Characteristics

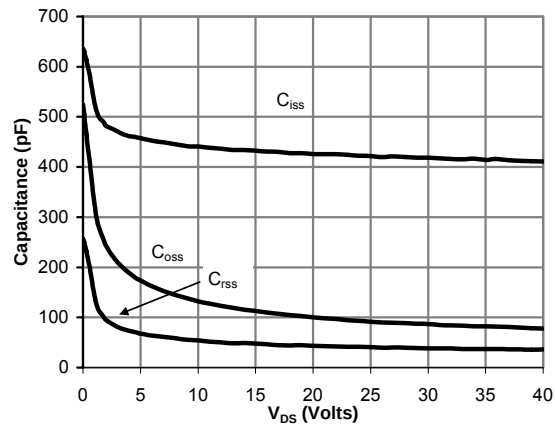


Figure 8: Capacitance Characteristics

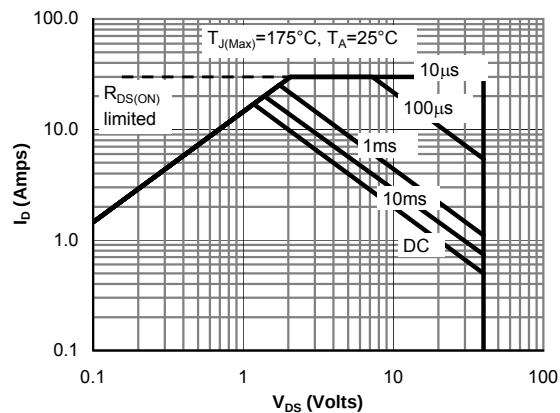


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

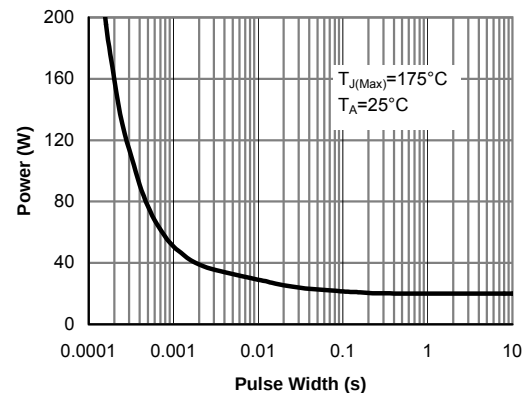


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

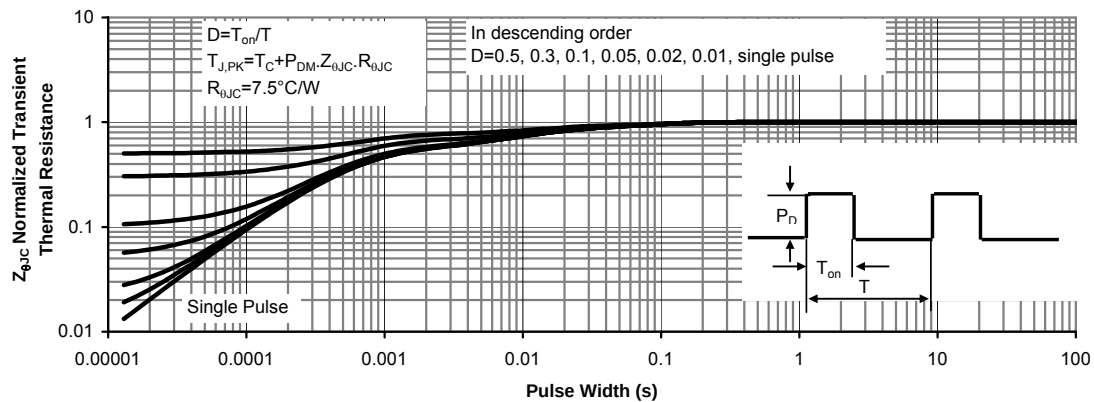


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

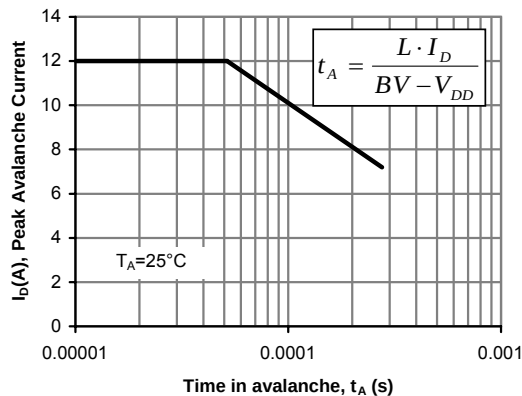


Figure 12: Single Pulse Avalanche capability

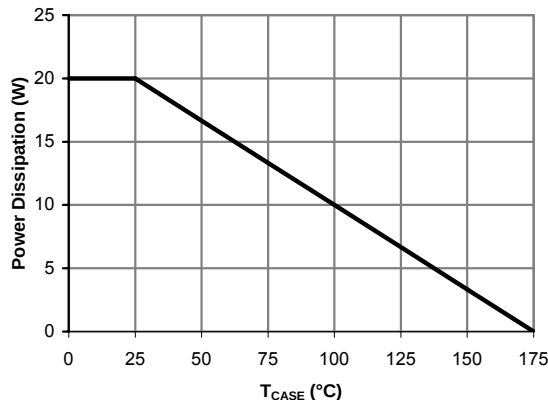


Figure 13: Power De-rating (Note B)

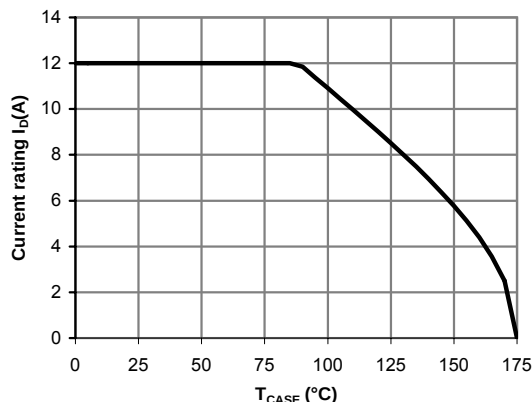


Figure 14: Current De-rating (Note B)

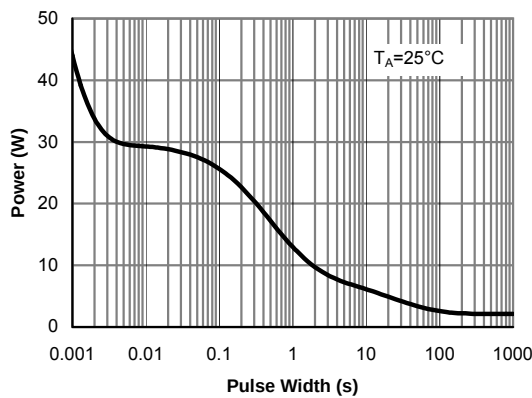


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

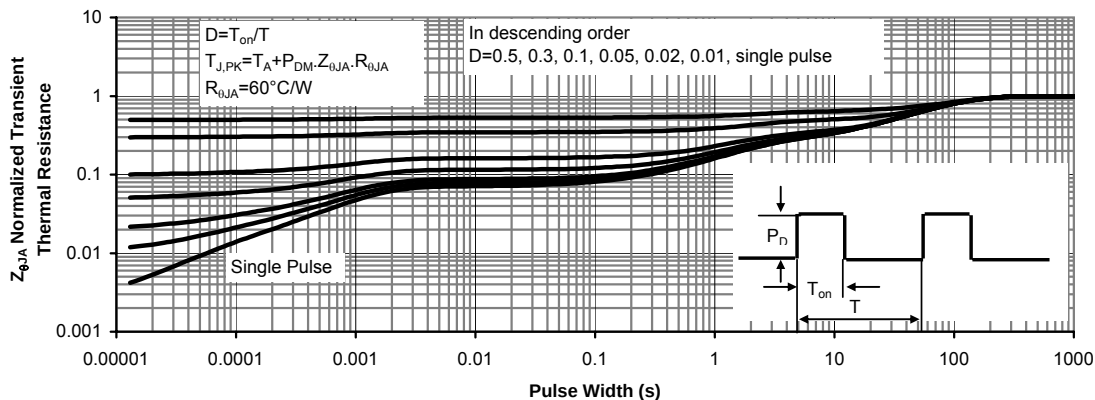


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)