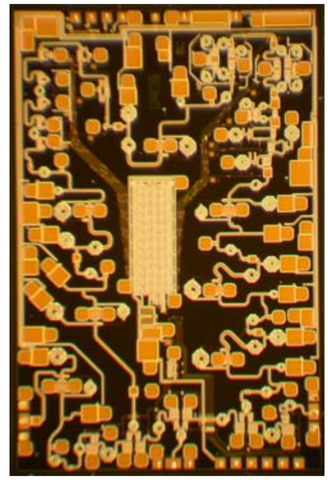
Control Chip, X-Band T/R 7.0—12.0 GHz

Features

- **Highly Integrated MMIC**
  - **Dual Path, Transmit/Receive Operation**
  - **6-Bit Phase Shifter and 6-Bit Attenuator**
  - **Tx Gain = 25 dB; Rx Gain = 19 dB**
  - **Rx Output TOI = 30 dBm**
  - **Serial Control Data Input**
- **50 Ω Input and Output Impedance**
- **Proven Manufacturability and Reliability**
  - **No Airbridges**
  - **Polyimide Scratch Protection**
  - **No Hydrogen Poisoning Susceptibility**



Description

The MAMF-000003-DIE000 is a 3-port, dual path transmit/ receive control MMIC. The on-chip serial-to-parallel converter enables the independent control of the 6-bit phase shifter and 6-bit attenuator and minimizes the required inputs. This product is fully matched to 50 ohms on both the input and output.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG) Process, each device is 100% RF tested on-wafer to ensure performance compliance.

M/A-COM's MSAG process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Radar Systems
- Commercial Avionics

Absolute Maximum Conditions[1]

Parameter	Symbol	Absolute Maximum	Units
Tx Input Power	Tx P_{IN}	5	dBm
Rx Input Power	Rx P_{IN}	6	dBm
Drain Supply Voltage	V_{DD}	7	V
Gate Supply Voltage	V_{GG}	-6.0	V
Quiescent Drain Current (No RF)	I_{DQ}	500	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	2.5	W
Logic Supply Voltage	V_{EE}	-6.0	V
Junction Temperature	T_j	170	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation beyond these limits may result in permanent damage to the part.

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Recommended Operating Conditions[2]

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.8	5.0	5.2	V
Gate Supply Voltage	V_{GG}	-5.2	-5.0	-4.8	V
Digital Supply Voltage	V_{EE}	-5.2	-5.0	-4.8	V
Input Logic High Voltage	V_{IH}	3.0	5.0	5.0	V
Input Logic Low Voltage	V_{IL}	0.0	0.0	0.4	V
Clock Frequency	F_{CLK}		20		MHz
Thermal Resistance	Θ_{JC}		25.6		°C/W
MMIC Base Temperature	T_B			Note 3	°C

2. Operation outside of these ranges may reduce product reliability.
3. Maximum MMIC Base Temperature = 170°C— Θ_{JC}* V_{DD} * I_{DQ}

Electrical Characteristics: T_B = 25°C[4], Z_0 = 50Ω, V_D = 5V, V_G = -5V, V_{EE} = -5V

Parameter	Symbol	Typical	Units
Bandwidth	f	7.0-12.0	GHz
Transmit Gain	Gn	25	dB
Receive Gain	Gn	19	dB
Input VSWR, Common Port, Transmit	VSWR	1.5:1	
Output VSWR, Tx Out Port, Transmit	VSWR	1.5:1	
Input VSWR, Rx In Port, Receive	VSWR	1.5:1	
Output VSWR, Common Port, Receive	VSWR	1.4:1	
Transmit P1dB	P1dB	23	dBm
Receive P1dB	P1dB	18	dBm
Receive Third Order Intercept, Output	OTOI	30	dBm
Receive Noise Figure	NF	10.5	dB
Attenuator Range (6 bits, 64 states)		0 to 31.5	dB
0.5 dB Bit, Relative Gain, LSB		-0.5	dB
1 dB Bit, Relative Gain		-1.0	dB
2 dB Bit, Relative Gain		-2.0	dB
4 dB Bit, Relative Gain		-4.0	dB
8 dB Bit, Relative Gain		-8.0	dB
16 dB Bit, Relative Gain, MSB		-16.0	dB
Phase Shifter Range (6 bits, 64 states)		0 to 354	°
5.6 ° Bit, Relative Phase, LSB		-5.6	°
11.2° Bit, Relative Phase		-11.2	°
22.5° Bit, Relative Phase		-22.5	°
45° Bit, Relative Phase		-45	°
90° Bit, Relative Phase		-90	°
180° Bit, Relative Phase, MSB		-180	°
Gate Supply Current	I_{GG}	10	mA
Drain Supply Current	I_{DD}	500	mA
Logic Supply Current	I_{EE}	50	mA

4. T_B = MMIC Base Temperature

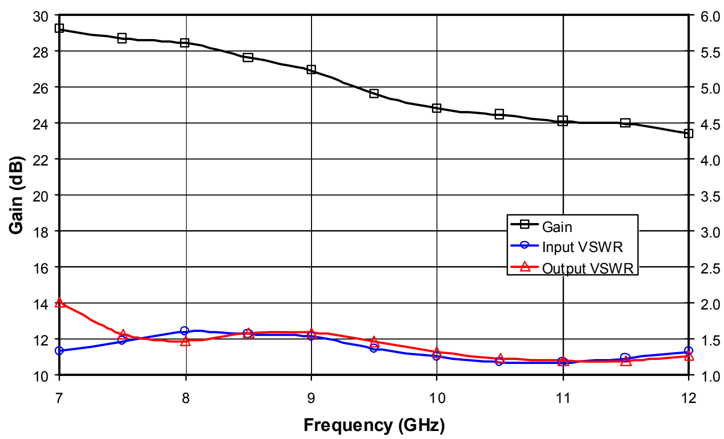

Figure 1. Transmit S-Parameters

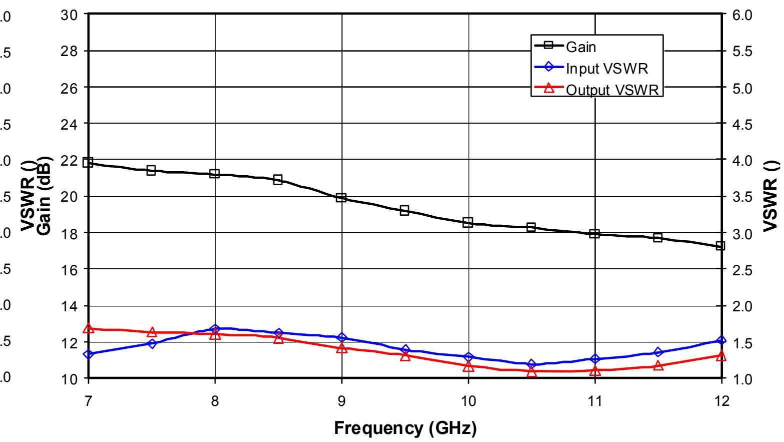

Figure 2. Receive S-Parameters

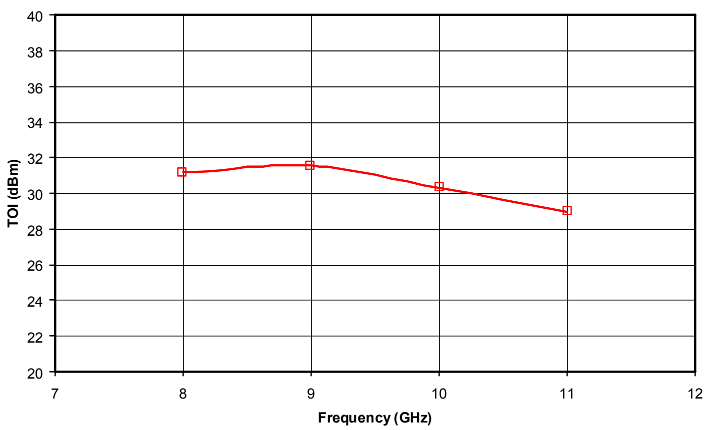

Figure 3. Receive Output TOI

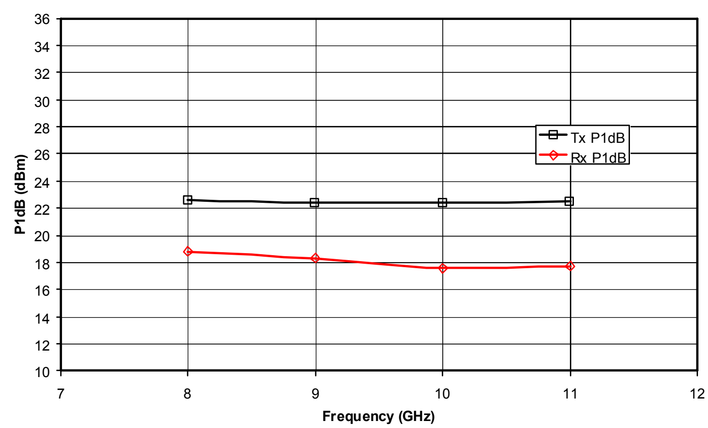

Figure 4. Transmit and Receive P1dB

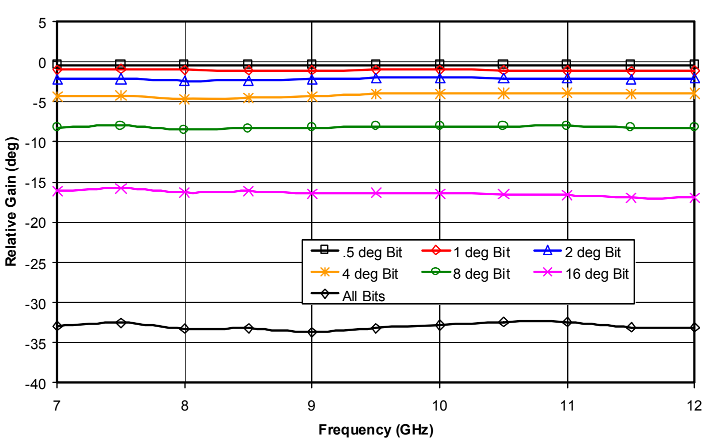

Figure 5. Relative Gain of Major Attenuator States

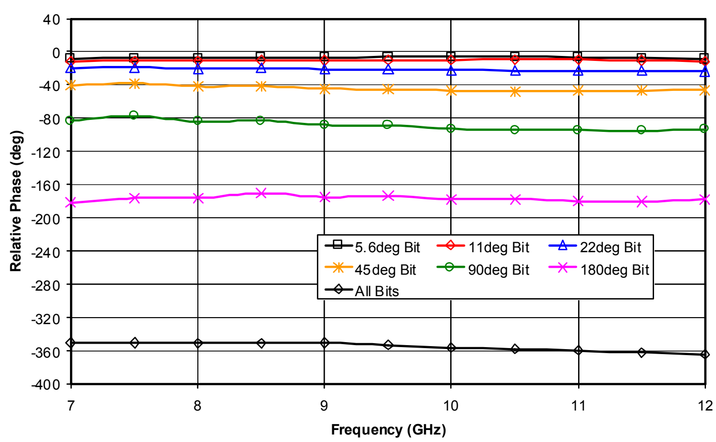

Figure 6. Relative Phase of Major Phase Shifter States

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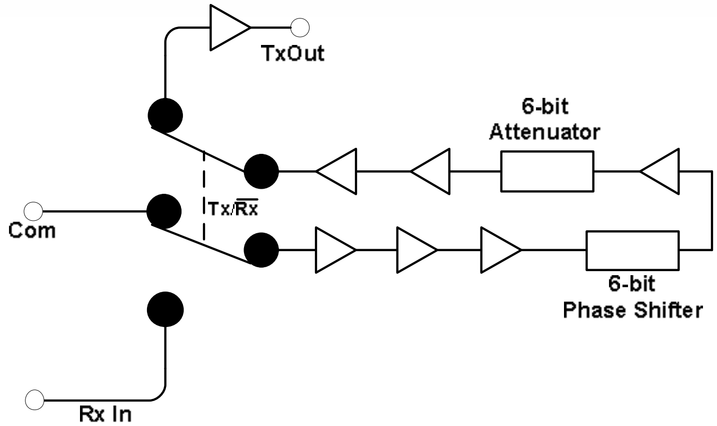

Figure 7. Block Diagram of Transmit/Receive Control MMIC

Truth Table and Data Sequence

X-Band T/R MMIC Control Function		
INPUT SIGNAL	**LOGIC LEVEL**	**FUNCTION**
CK (Clock)	Falling Edge	Shifts the data, DI
DI (Data In)	High/Low	Phase and Attn Setting
LD (Load)	Falling Edge	Loads the data from D24 Shift Register
SL and TR (Select & T/R Control)	Low	Selects odd bits (Transmit) and Transmit Path
SL and TR (Select & T/R Control)	High	Selects even bits (Receive) and Receive Path
Logic Level	Logic High	Logic 1: 3.0 to 5V
	Logic Low	Logic 0: 0 to 0.4V
Attn and Phase States	Logic Low	Phase and Attn in Ref. State
	Logic High	Phase and Attn Shift Negative
LSB data enters first and MSB enters last. LSB data travels all 24 shift registers.		

Serial-to-Parallel Converter I/Os						
Input Data to SPC	**TR "Low" – TX TR "High" – RX**	**Phase and Attn**		**Input Data to SPC**	**TR "Low" – TX TR "High" – RX**	**Phase and Attn**
D1-LSB	Transmit	5.6º-bit PS		D13	Transmit	0.5 dB-bit Attn
D2	Receive			D13	Receive	
D3	Transmit	11 º-bit PS		D15	Transmit	1 dB-bit Attn
D4	Receive			D16	Receive	
D5	Transmit	22 º-bit PS		D17	Transmit	2 dB-bit Attn
D6	Receive			D18	Receive	
D7	Transmit	45 º-bit PS		D19	Transmit	4 dB-bit Attn
D8	Receive			D20	Receive	
D9	Transmit	90 º-bit PS		D21	Transmit	8 dB-bit Attn
D10	Receive			D22	Receive	
D11	Transmit	180 º-bit PS		D23	Transmit	16 dB-bit Attn
D12	Receive			D24	Receive	

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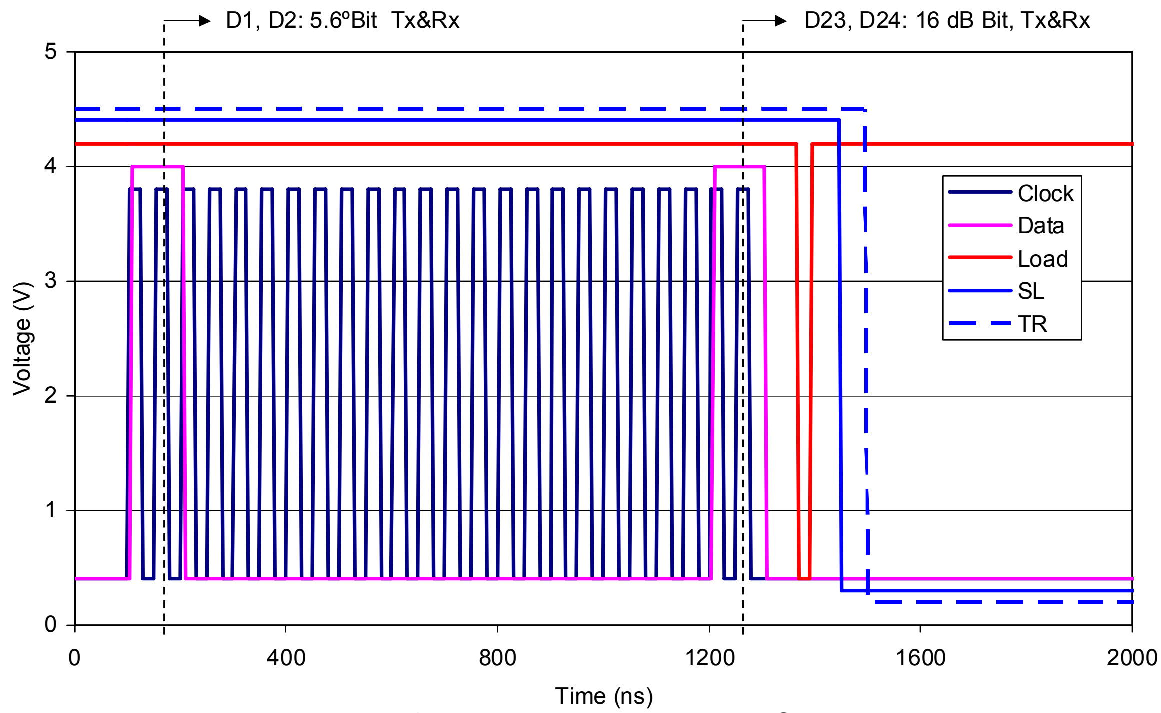

Figure 8. Timing Diagram, Data Sequence

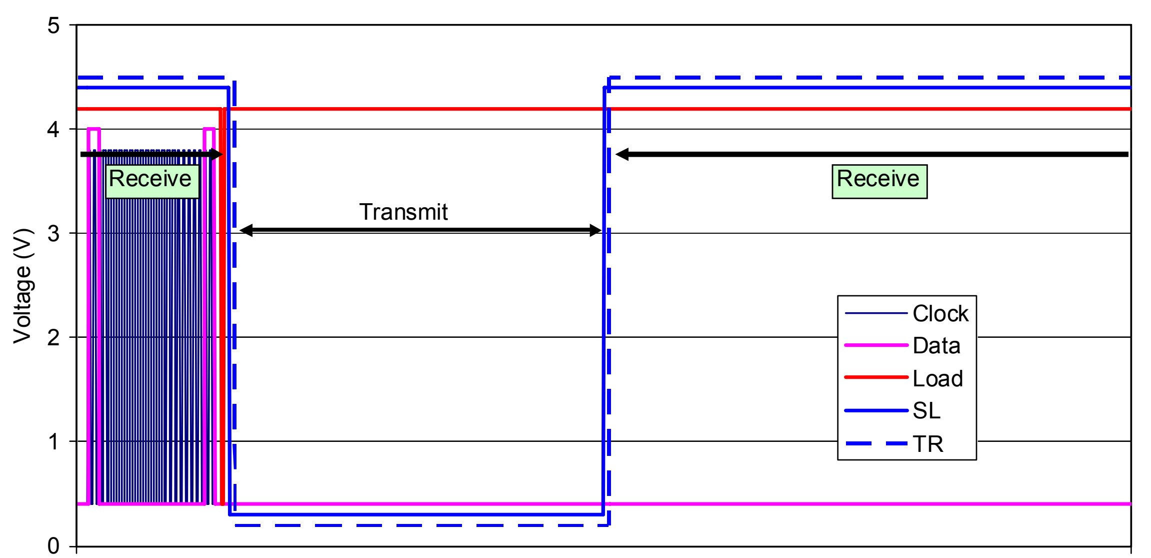

Figure 9. Timing Diagram, Transmit/Receive Relationship

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Mechanical Information

Chip Size: 6.0 x 4.0 x 0.075 mm (236 x 157 x 3 mils)

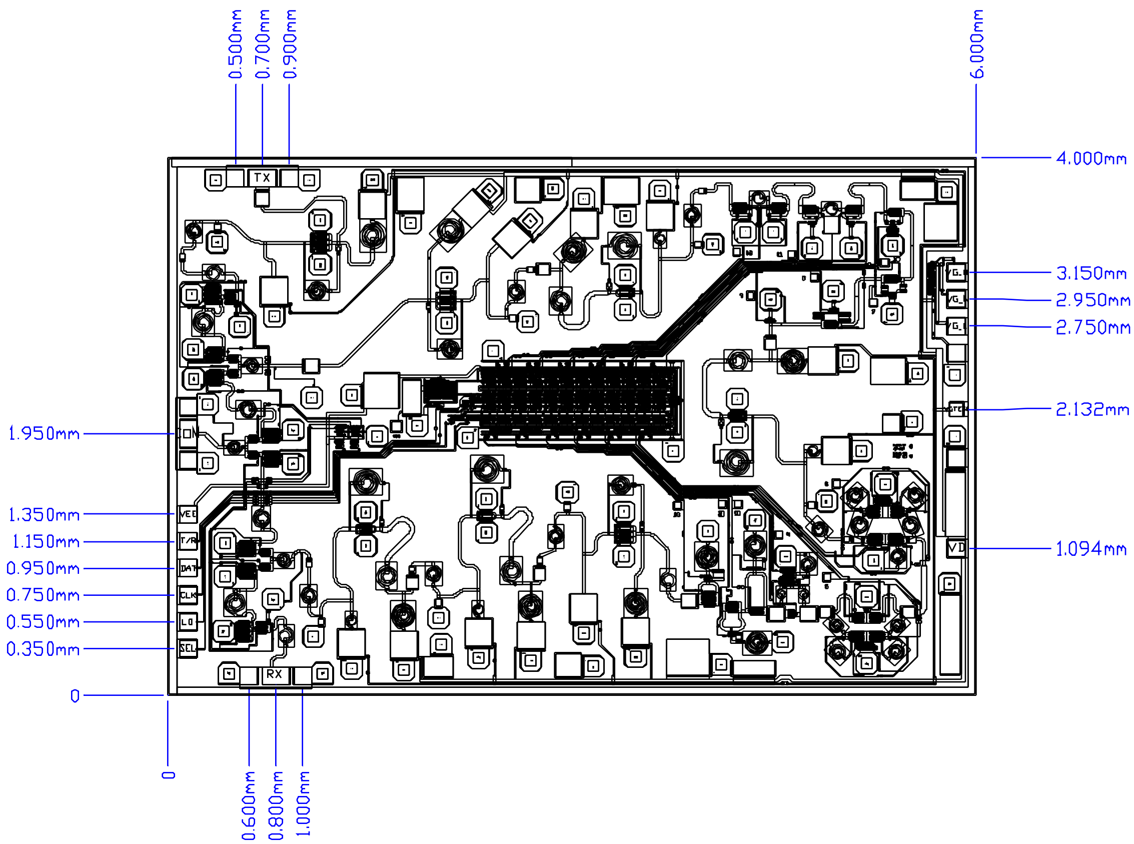


Figure 10 . Die Layout

Bond Pad Information

Pad	Type	Nominal Voltage	Size	
			(µm)	(mils)
Common, Tx Out, Rx In	RF	N/A	150 x 150	6 x 6
T/R, Sel, Load, Data, Clock	Control	0 / 5 V	125 x 125	5 x 5
V_{DD}	DC	5.0 V	150 x 150	6 x 6
V_{EE}	DC	-5.0 V	125 x 125	5 x 5
V_G–HI, V_G–N, V_G–LO	DC	-5.0 V	150 x 150	6 x 6

Assembly and Bonding Diagram

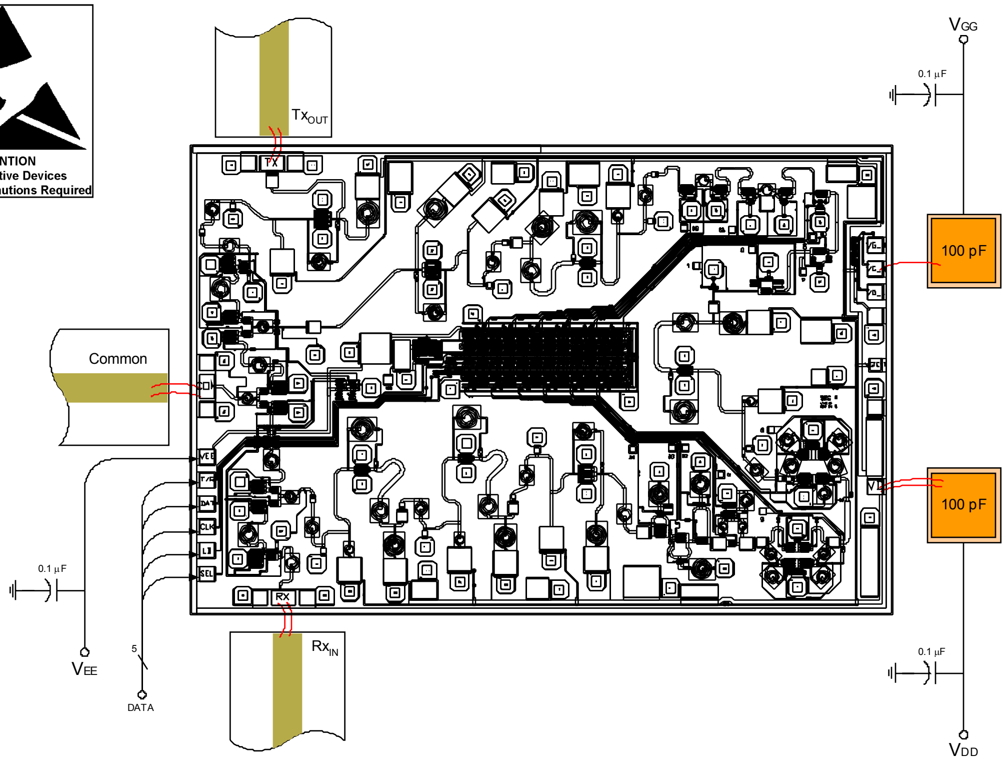


Figure 11. Recommended bonding diagram.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

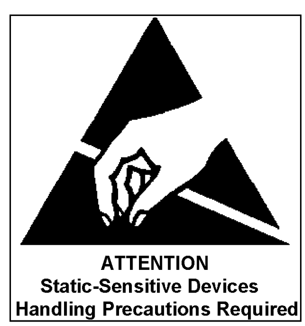
Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -5 V, V_{EE} = -5V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 5 V.
3. Adjust V_{GG} to set I_{DQ}.
4. Set RF input.
5. Power down in reverse. Turn V_{GG} off last.



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