

DRAM CARD

16 Mega Byte

KMCV5324000(3.3V Operating)
4M x 32 / 8M x 16 Fast Page Mode

GENERAL DESCRIPTION

The KMCV5324000 is the industry standard high capacity DRAM memory card and consists of SAMSUNG's advanced TSOP 4Mx4 DRAM devices operating in 3.3V power supply.

The SAMSUNG memory card family is designed to protect the internal circuitry from electrostatic discharge by using metal plates on the top and bottom side of the card. And the memory card supports the JEIDA standard to provide system upgradability and exchangeability

The memory card allows the user to switch x32/x16 for the ease of system interface. The memory card is designed to suit for memory capacity expansion and applications which handles large data.

FEATURES

- Performance range :

	tRAC	tCAC	tRC
KMCV5324000 - 7	70 ns	27 ns	140 ns
KMCV5324000 - 8	80 ns	27 ns	160 ns
- Organization : 4Mx32 / 8Mx16
- Power Supply : 3.3±0.3V
- Fast Page Mode Operation
- TTL compatible inputs and outputs
- All inputs buffered except \overline{RAS} inputs
- Extended refresh : 4096 cycles/256 ms
 - \overline{RAS} only and Hidden refresh
 - \overline{CAS} before \overline{RAS} refresh
- Supported Industry Standard (JEIDA / JEDEC)
- Connector type : 88 pin two piece (Two Row)
 - Card Dimensions : 85.6 x 54.0 x 3.3 (mm)

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PIN CONFIGURATION

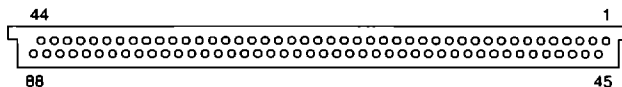
1	Vss	16	A4	31	NC	46	DQ16	61	A9	76	PD8
2	DQ0	17	Vcc	32	NC	47	DQ17	62	A11	77	NC
3	DQ1	18	A6	33	NC	48	DQ18	63	Vss	78	NC
4	DQ2	19	A8	34	DQ8	49	DQ19	64	NC	79	NC
5	DQ3	20	A10	35	Vcc	50	DQ20	65	NC	80	DQ24
6	DQ4	21	NC	36	DQ9	51	DQ21	66	$\overline{CAS2}$	81	DQ25
7	DQ5	22	$\overline{RAS0}$	37	NC	52	DQ22	67	Vss	82	DQ26
8	DQ6	23	$\overline{CAS0}$	38	DQ10	53	DQ23	68	$\overline{CAS3}$	83	DQ27
9	NC	24	$\overline{CAS1}$	39	DQ11	54	NC	69	NC	84	DQ28
10	DQ7	25	Vcc	40	DQ12	55	NC	70	\overline{WE}	85	DQ29
11	Vcc	26	$\overline{RAS2}$	41	DQ13	56	Vss	71	PD1	86	DQ30
12	NC	27	NC	42	DQ14	57	A1	72	PD3	87	DQ31
13	A0	28	PD2	43	DQ15	58	A3	73	Vss	88	Vss
14	A2	29	PD4	44	Vss	59	A5	74	PD5		
15	NC	30	PD6	45	Vss	60	A7	75	PD7		

PIN DESCRIPTION

A0 - A11	Address Inputs
DQ0 - DQ31	Data Input / Outputs
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
\overline{WE}	Read / Write Input
Vcc	Power (+3.3V)
Vss	Ground
NC	No Connection

	70 ns	80 ns
PD1	GND	GND
PD2	GND	GND
PD3	NC	NC
PD4	GND	GND
PD5	NC	NC
PD6	GND	NC
PD7	NC	GND
PD8	NC	NC

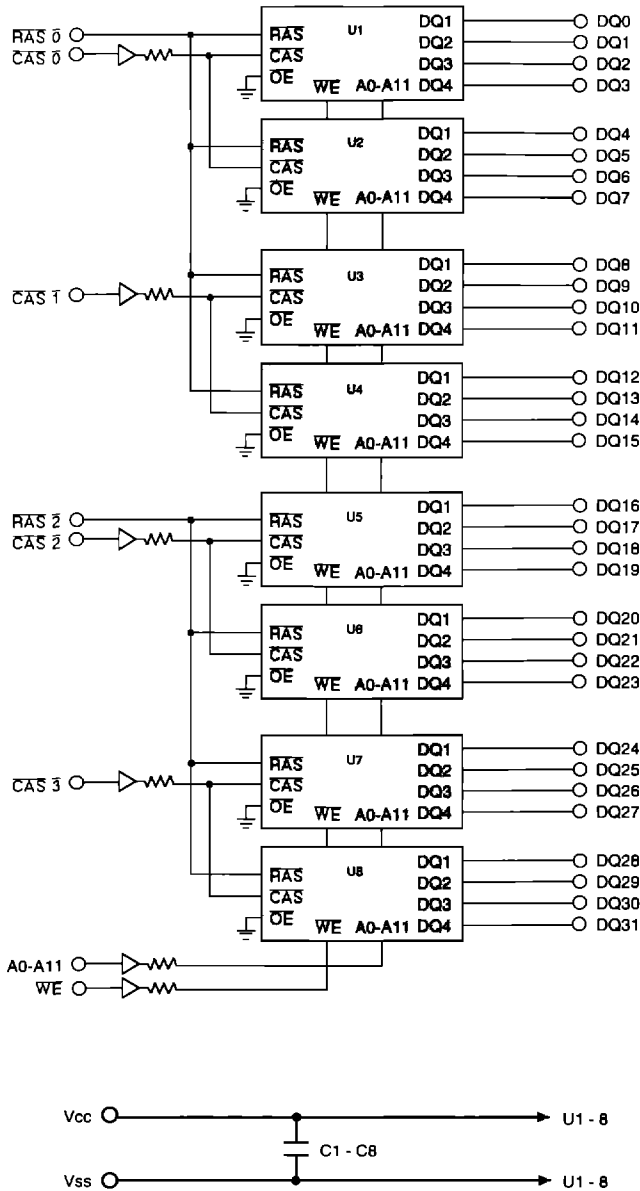
PIN CONNECTOR



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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Input Voltage on any pin relative to Vss : RAS pin	V _{IN1}	-0.3 to +3.6	V
Input Voltage on any pin relative to Vss : except RAS pin	V _{IN2}	-0.3 to V _{CC} +0.3	V
Output Voltage on any pin relative to Vss	V _{OUT}	-0.3 to +4.5	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to +4.5	V
Storage Temperature	T _{stg}	-20 to +70	°C
Power Dissipation	P _D	4.8	W
Short Circuit Output Current	I _{OS}	50	mA

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	-	0.8	V
Operating Temperature	T _A	0	-	55	°C

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DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Units
OPERATING CURRENT* (\overline{RAS} , \overline{CAS} , Address cycling @ $t_{RC}=\text{min.}$)	KMCMV5324000 - 7 KMCMV5324000 - 8	I_{CC1}	-	720 640	mA mA mA
STANDBY CURRENT($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	-	16	mA
RAS-ONLY REFRESH CURRENT* ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @ $t_{RC}=\text{min.}$)	KMCMV5324000 - 7 KMCMV5324000 - 8	I_{CC3}	-	720 640	mA mA mA
FAST PAGE MODE CURRENT* ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling: $t_{PC}=\text{min.}$)	KMCMV5324000 - 7 KMCMV5324000 - 8	I_{CC4}	-	560 480	mA mA mA
STAND BY CURRENT ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		I_{CC5}	-	2.4	mA
CAS-BEFORE-RAS REFRESH CURRENT* (\overline{RAS} and \overline{CAS} cycling @ $t_{RC}=\text{min.}$)	KMCMV5324000 - 7 KMCMV5324000 - 8	I_{CC6}	-	720 640	mA mA mA
BATTERY BACK UP CURRENT - only Low Power ver. ($\overline{CAS}=\overline{CAS}$ before \overline{RAS} cycling or 0.2V, $\overline{WE}/A0-A9=V_{CC}-0.2V$ or 0.2V, $D_{IN}=V_{CC}-0.2V$ or open, $t_{RC}=125\mu s$, $t_{RAS}=\text{min.} \sim 1\mu s$)		I_{CC7}	-	4.0	mA
INPUT LEAKAGE CURRENT (Any input $0 \leq V_{IN} \leq 3.6V$, all other pins not under test = 0 volts.)	\overline{RAS} pin	I_{IL}	-40	40	μA
	else \overline{RAS} pin		-1	1	
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 3.6V$)		I_{OL}	-10	10	μA
OUTPUT HIGH VOLTAGE LEVEL($I_{OH} = -2.0mA$)		V_{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL($I_{OL} = 2.0mA$)		V_{OL}	-	0.4	V

* NOTE I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC5} is specified as an average current.

CAPACITANCE (T = 25 °C)

Item	Symbol	Min	Max	Unit
Input capacitance : A0-A11	C_{IN1}	-	15	pF
Input capacitance WE	C_{IN2}	-	15	pF
Input capacitance : $\overline{RAS0}$, $\overline{RAS2}$	C_{IN3}	-	50	pF
Input capacitance : $\overline{CAS0}$ - $\overline{CAS3}$	C_{IN4}	-	15	pF
Input/Output capacitance DQ0-DQ31	C_{DO1}	-	10	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 55°C, Vcc = 3.3 ± 0.3V See notes 1,2)

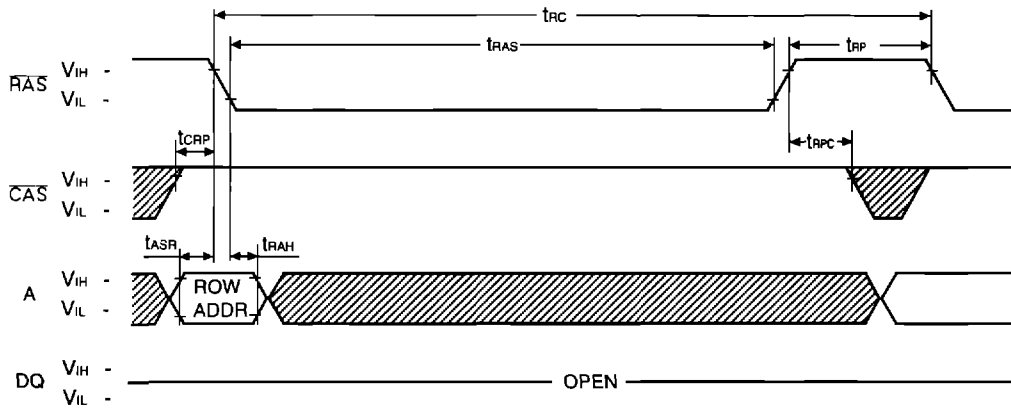
STANDARD OPERATION	Symbol	KMCV5324000-7		KMCV5324000-8		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	140		160		ns	
Access time from RAS	tRAC		70		80	ns	3,4
Access time from CAS	tCAC		27		27	ns	3,4,5
Access time from column address	tAA		42		47	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	27	0	27	ns	7
Transition time (rise and fall)	tT	3	50	3	50	ns	2
RAS precharge time	tRP	50		60		ns	
RAS pulse width	tRAS	70	10,000	80	10,000	ns	
RAS hold time	tRSH	27		27		ns	
CAS hold time	tCSH	70		80		ns	
CAS pulse width	tCAS	27	10,000	27	10,000	ns	
RAS to CAS delay time	tRCD	18	43	20	53	ns	4
RAS to column address delay time	tRAD	13	28	13	33	ns	11
CAS to RAS precharge time	tCRP	17		17		ns	
Row address set-up time	tASR	7		7		ns	
Row address hold time	tRAH	8		13		ns	
Column address set-up time	tASC	2		2		ns	
Column address hold time	tCAH	22		22		ns	
Column address hold referenced to RAS	tAR	55		60		ns	6
Column Address to RAS lead time	tRAL	42		47		ns	
Read command set-up time	tRCS	2		2		ns	
Read command hold referenced to CAS	tRCH	2		2		ns	9
Read command hold referenced to RAS	tRRH	2		2		ns	9
Write command hold time	tWCH	15		15		ns	
Write command hold referenced to RAS	tWCR	55		60		ns	6
Write command pulse width	tWP	15		15		ns	
Write command to RAS lead time	tRWL	27		27		ns	
Write command to CAS lead time	tCWL	20		20		ns	
Data-in set-up time	tDS	2		2		ns	10
Data-in hold time	tDH	22		22		ns	10
Data-in hold referenced to RAS	tDHR	55		60		ns	6
Refresh period	tREF		256		256	ms	
Write command set-up time	tWCS	2		2		ns	8
CAS setup time (C-B-R refresh)	tCSR	17		17		ns	
CAS hold time (C-B-R refresh)	tCHR	17		17		ns	
RAS precharge to CAS hold time	tRPC	22		22		ns	
Access time from CAS precharge	tCPA		47		52	ns	3
Fast Page mode cycle time	tPC	52		57		ns	
CAS precharge time (Fast page)	tCP	10		10		ns	
RAS pulse width (Fast page)	tRASP	70	100K	80	100K	ns	
W to RAS precharge time (C-B-R refresh)	tWRP	10		10		ns	
W to RAS hold time (C-B-R refresh)	tWRH	10		10		ns	
CAS precharge (C-B-R counter test)	tCPT	25		30		ns	

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NOTES

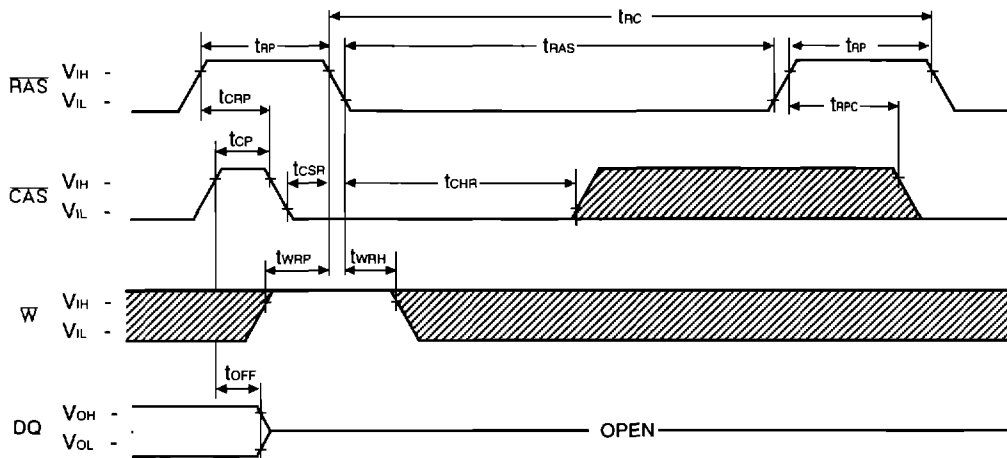
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. tWCS is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If tWCS \geq tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

RAS-ONLY REFRESH CYCLE




NOTE : \bar{W} = Don't care

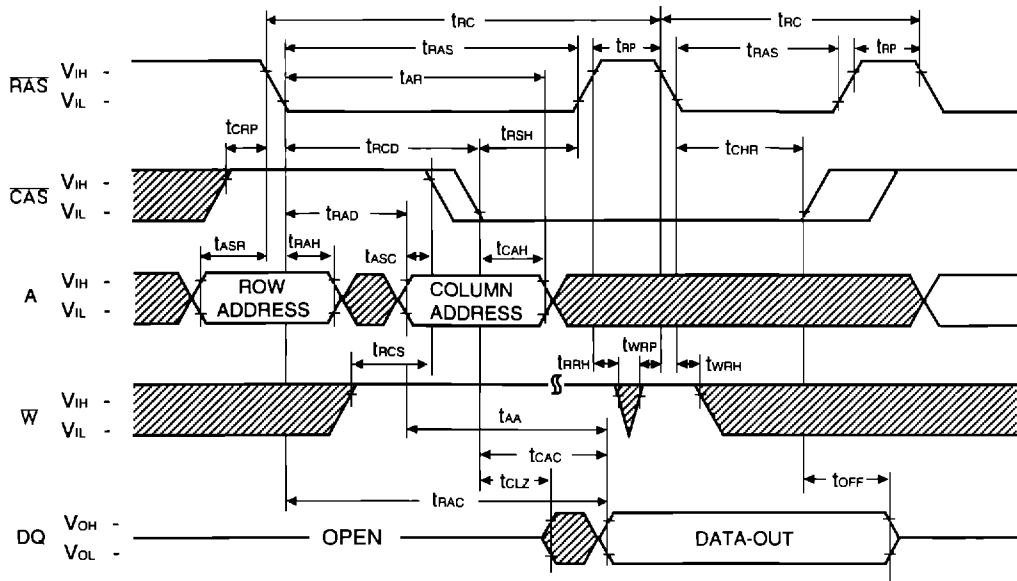
CAS-BEFORE-RAS REFRESH CYCLE



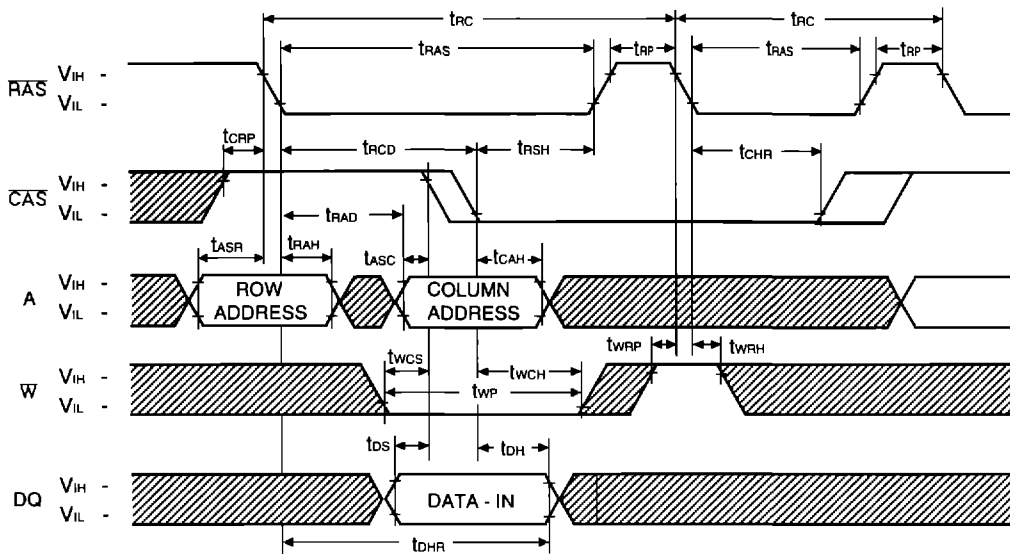
NOTE A = Don't Care

 Don't Care

HIDDEN REFRESH CYCLE (READ)

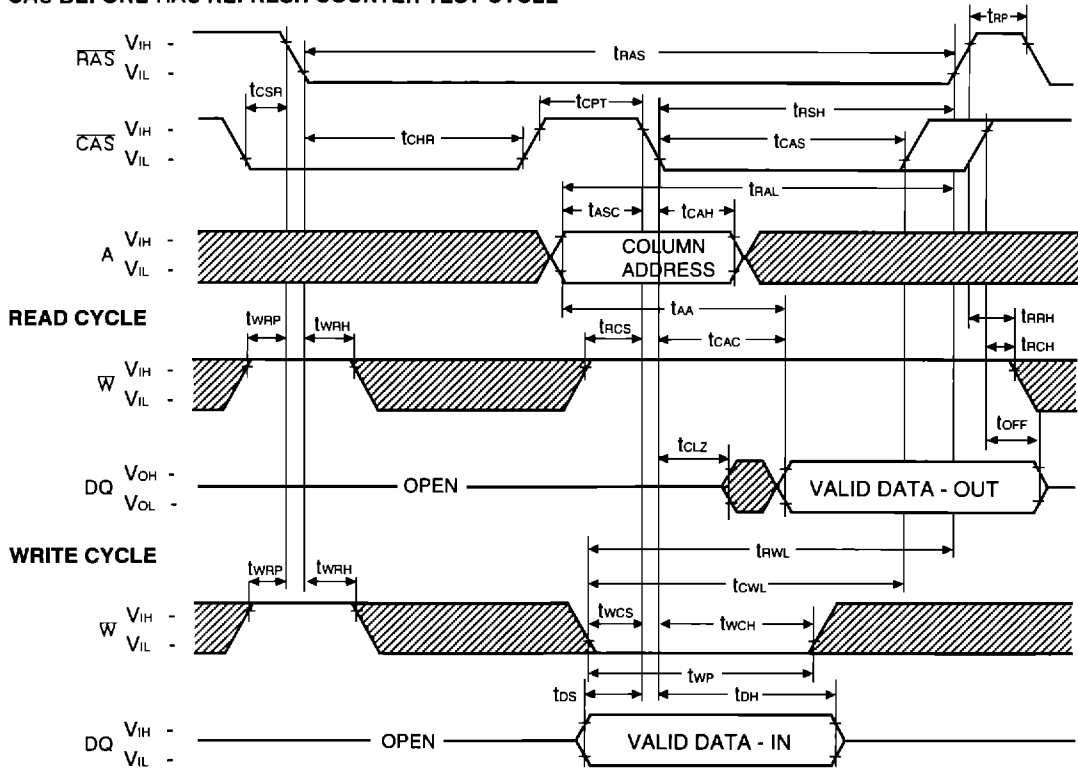


HIDDEN REFRESH CYCLE (WRITE)



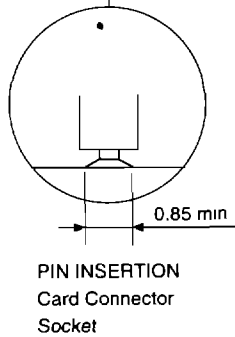
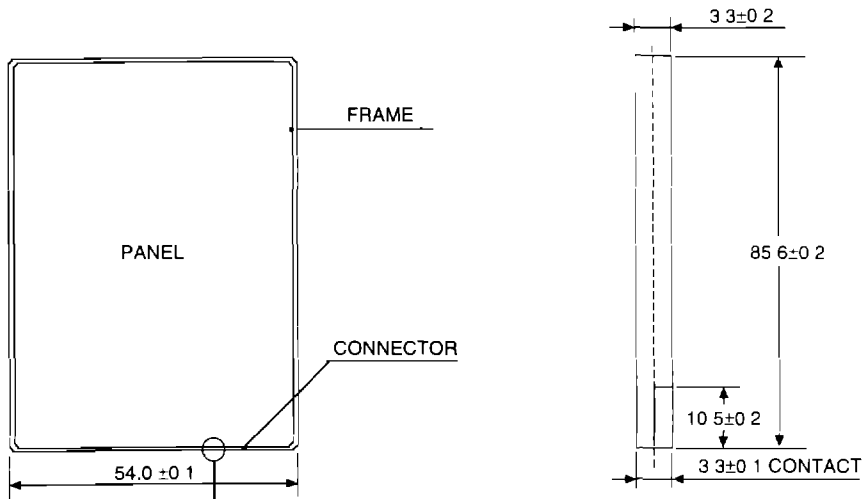
Don't Care

CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE

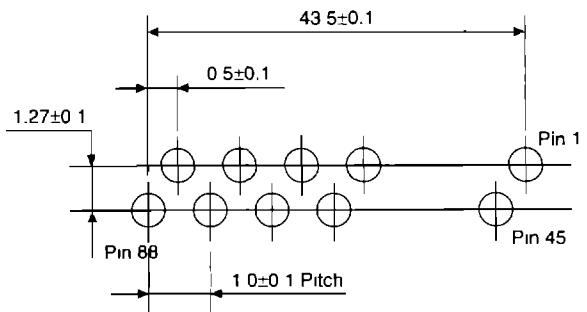


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PACKAGE DIMENSIONS



PIN LAYOUT 2 Row - 88 Pins



CONNECTOR

