QPro XQR18V04 Radiation Hardened 4Mbit QML ISP Configuration Flash PROM

Features

- Operating Temperature Range: –55° C to +100° C
- Latch-Up Immune to LET >120 MeV/cm^2/mg
- Guaranteed TID of 30 kRad(Si) per spec 1019.5
- Fabricated on Epitaxial Substrate
- Low-power advanced CMOS FLASH process memory cells immune to static single event upset
- Supports SEU Scrubbing for Virtex series FPGAs
- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
  - Endurance of 2,000 program/erase cycles
  - Program/erase over operational temperature range
- IEEE Std 1149.1 boundary-scan (JTAG) support
- Cascadable for storing longer or multiple bitstreams
- Dual configuration modes
  - Serial Slow/Fast configuration (up to 20 MHz)
  - Parallel (up to 160 Mbps at 20 MHz)
- 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
- 3.3V or 2.5V output capability
- Available in CC44 and VQ44 packages
- Design support using the Xilinx Alliance Series™ and Xilinx Foundation Series™ software packages
- JTAG command initiation of standard FPGA configuration

Description

Xilinx introduces the QPro™ XQR18V04 radiation hardened QML 4Mbit in-system programmable configuration Flash PROM. The XQR18V04 is a 3.3V latch-up immune, static SEU immune, rewritable PROM that provides a reliable non-volatile method for storing large Xilinx FPGA configuration bitstreams used in space flight systems.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising CCLK, data is available on the PROM DATA (D0) pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in SelectMAP mode (Slave), an external oscillator will generate the configuration clock that drives the PROM and the FPGA. After the rising CCLK edge, data are available on the PROMs DATA (D0-D7) pins. The data will be clocked into the FPGA on the following rising edge of the CCLK. See Figure 3.

Multiple devices can be cascaded by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. The XQR18V04 is compatible and can be cascaded with other configuration PROMs such as the XQR1701L and XQR17V16 one-time programmable configuration PROMs.

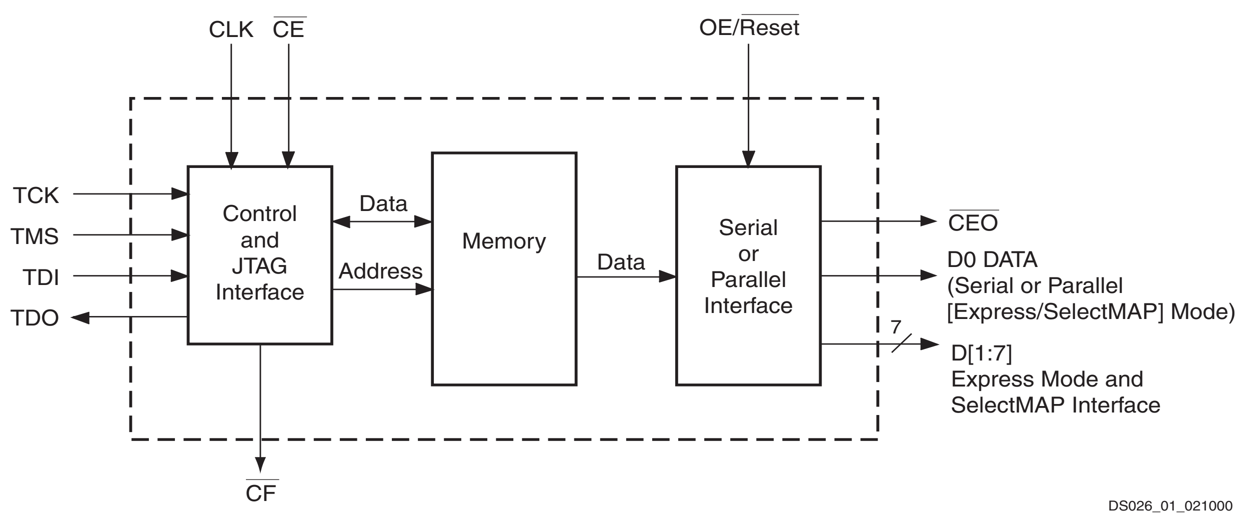


Figure 1: **XQR18V04 Series Block Diagram**

Radiation Tolerances

Table 1: **Guaranteed Radiation Tolerance Specifications**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose for data retention and data output port read (configuration) operations	-	30	krad(Si)
	Total Ionizing Dose for all JTAG ISP functions, data rewrite and data verify.	-	10	krad(Si)
SEL	Single Event Latch-Up (No Latch-Up observed for LET > 120 MeV-mg/cm^2)	-	0	cm^2
SEU	Static Memory Cell Saturation Bit Cross-Section (No Upset observed for LET > 120 MeV-mg/cm^2)	-	0	cm^2

Xilinx FPGAs and Compatible PROMs

Table 2: **FPGA Configuration Storage Requirements**

Device	Configuration Bits	XQR18V04 PROMs
XQVR300	1,751,808	1
XQVR600	3,607,968	1
XQVR1000	6,127,744	2
XQR2V1000	3,752,736	1
XQR2V3000	9,594,656	3
XQR2V6000	19,759,904	5

Capacity

Table 3: **PROM Storage Capacity**

Device	Configuration Bits
XQR18V04	4,194,304

Connecting Configuration PROMs

When connecting the FPGA device with the configuration PROM (see Figure 3):

- The DATA output(s) of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s) in Master Serial and Master SelectMAP modes.
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection ensures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of the first FPGA device, provided that DONE is not permanently grounded. $\overline{CE}$ also can be tied permanently Low, but this keeps the DATA output active and causes an unnecessary supply current of 20 mA maximum.
- D1-D7 remain in a high-impedance state and can be left unconnected when the PROM operates in serial mode.
- Express/SelectMap mode is similar to slave serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

Initiating FPGA Configuration

The XQR18V04 device incorporates a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses $\overline{CF}$ Low for 300 to 500 ns, which resets the FPGA and initiates configuration.

The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s) to use this feature.

The Xilinx iMPACT™ software can also issue a JTAG CONFIG command to initiate FPGA configuration through the "Load FPGA" setting.

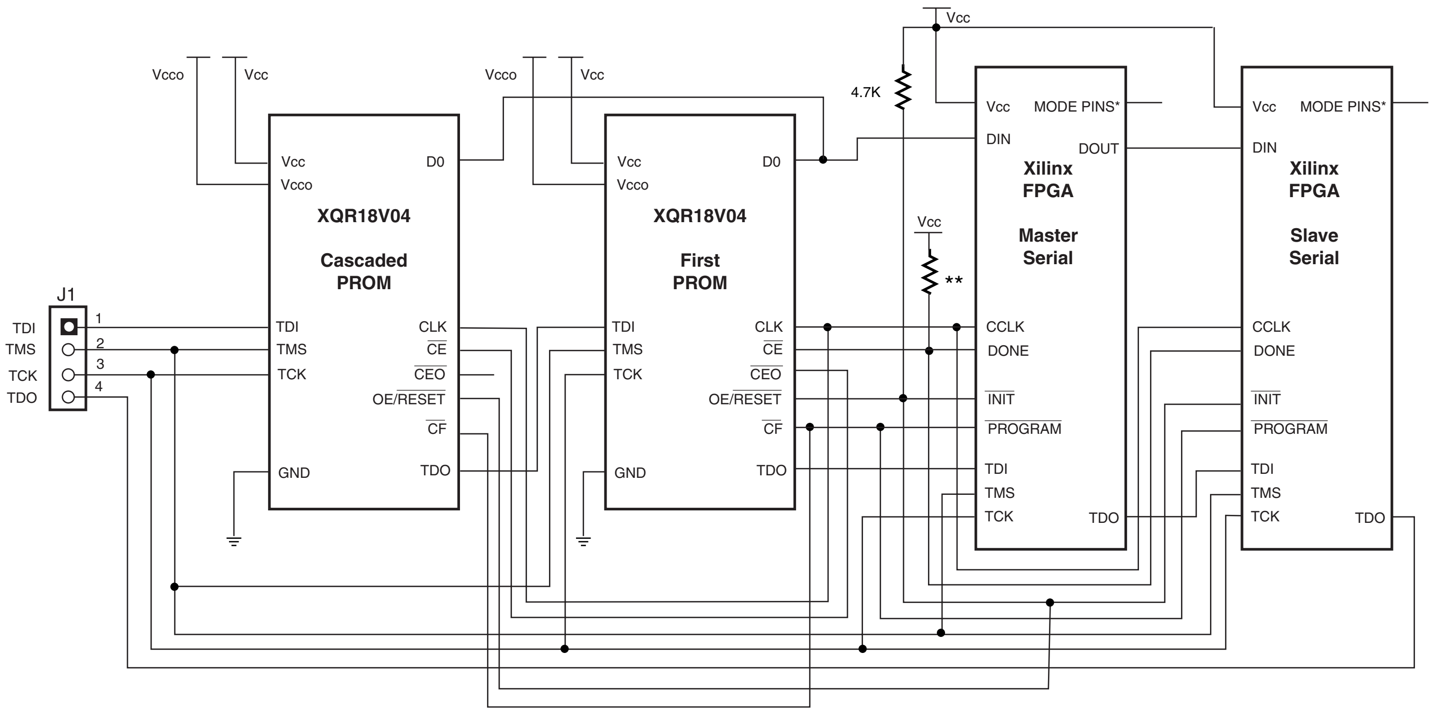
Selecting Configuration Modes

The XQR18V04 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XQR18V04 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx iMPACT software. Serial output is the default programming mode.

Cascading Configuration PROMs

For multiple FPGAs configured as a serial daisy-chain, or a single FPGA requiring larger configuration memories in a serial or SelectMAP configuration mode, cascaded PROMs provide additional memory (see Figure 2). Multiple XQR18V04 devices can be cascaded by using the CEO output to drive the CE input of the downstream device. The clock inputs and the data outputs of all the XQR18V04 devices in the chain are interconnected. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its CEO output Low and drives its DATA line to a high-impedance state. The second PROM recognizes the Low level on its CE input and enables its DATA output. See Figure 3.

After configuration is complete, the address counters of all cascaded PROMs are reset if the PROM OE/RESET pin goes Low.



* For Mode pin connections, refer to the appropriate FPGA data sheet.
** Resistor value is 300 ohms for Virtex and Virtex-E devices, and is 4.7Kohms for all other devices.

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Figure 2: **JTAG Chain for Configuring Devices in Master Serial Mode**

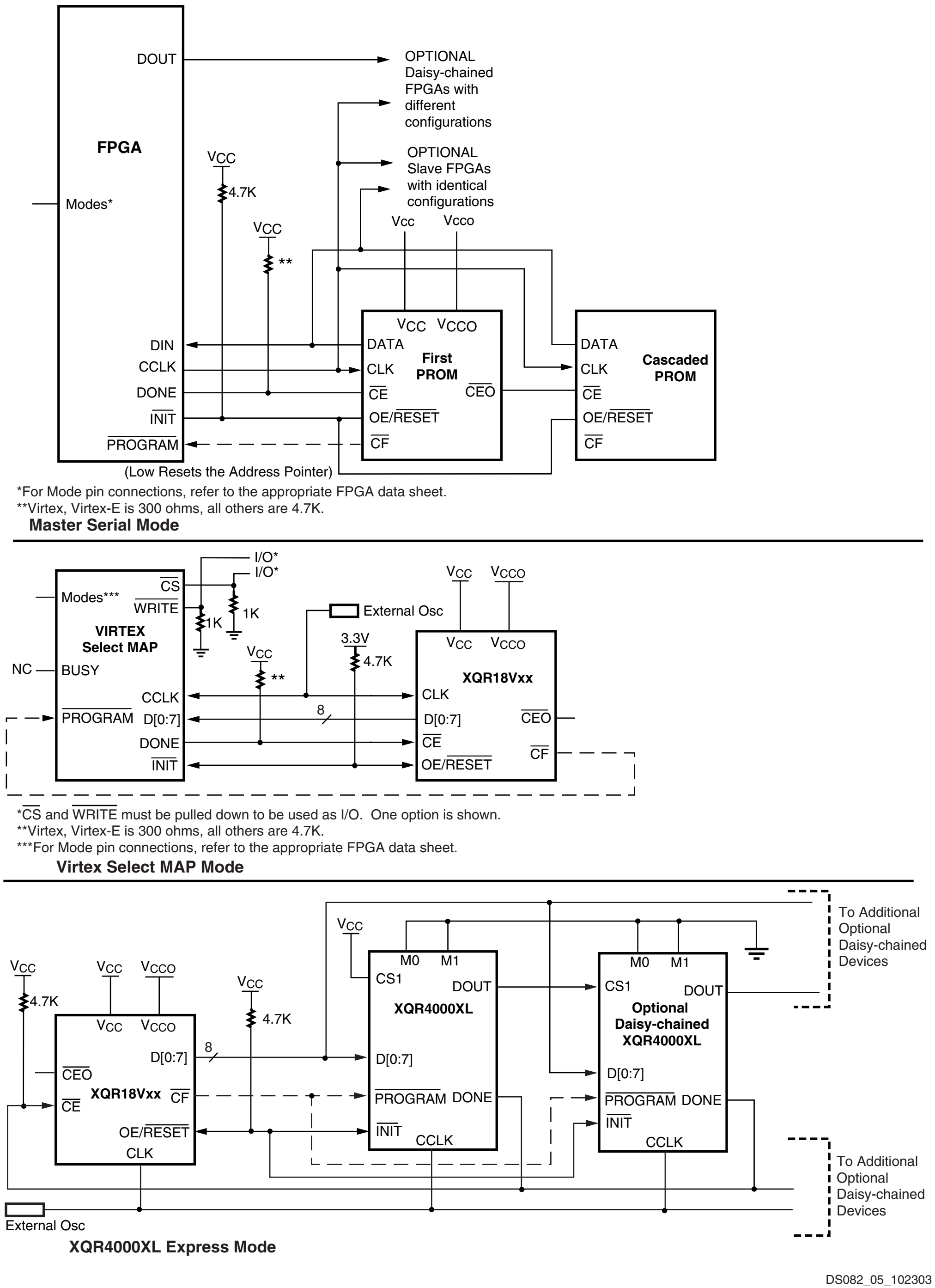

Figure 3: **(a) Master Serial Mode (b) Virtex SelectMAP Mode (c) XQR4000XL Express Mode**
(dotted lines indicate optional connection)

5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even through the core power supply is 3.3V. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V V_{CC} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CC}), and the output power supply (V_{CCO}) may have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

Reset Activation

On power up, OE/$\overline{\text{RESET}}$ is held Low until the XQR18V04 is active (1 ms) and is able to supply data after receiving a CCLK pulse from the FPGA. OE/$\overline{\text{RESET}}$ is connected to an external resistor to pull OE/$\overline{\text{RESET}}$ High releasing the FPGA $\overline{\text{INIT}}$ and allowing configuration to begin. OE/$\overline{\text{RESET}}$ is held Low until the XQR18V04 voltage reaches the operating voltage range. If the power drops below 2.0V, the PROM will reset. OE/$\overline{\text{RESET}}$ polarity is NOT programmable. See Figure 4 for power-on requirements.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. The output remains in a high-impedance state regardless of the state of the OE input. JTAG pins TMS, TDI, and TDO can be in a high-impedance state or High. See Table 4.

Customer Control Bits

The XQR18V04 PROMs have various control bits accessible by the customer. These can be set after the array has been programmed using “Skip User Array” in Xilinx iMPACT software. The iMPACT software can set these bits to enable the optional JTAG read security, parallel configuration mode, or CF-->D4 pin function.

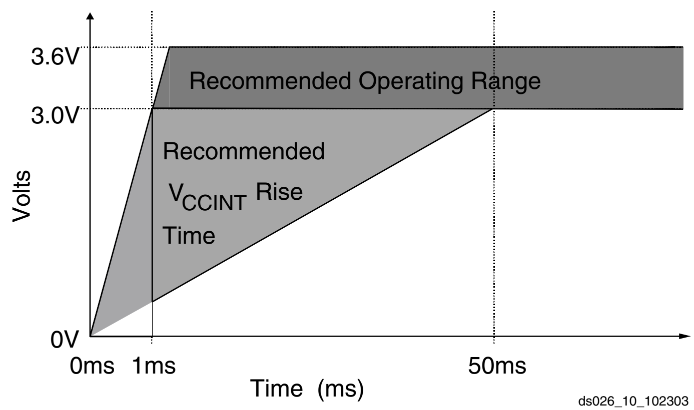

Figure 4: **VCCINT Power-On Requirements**

Table 4: **Truth Table for PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/$\overline{\text{RESET}}$	$\overline{\text{CE}}$		DATA	$\overline{\text{CEO}}$	I_{CC}
High	Low	If address ≤ TC(1): increment If address > TC(1): don't change	Active High-Z	High Low	Active Reduced
Low	Low	Held reset	High-Z	High	Active
High	High	Held reset	High-Z	High	Standby
Low	High	Held reset	High-Z	High	Standby

Notes:
1. TC = Terminal Count = highest address value. TC + 1 = address 0.

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 5. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx iMPACT software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format and with automatic test equipment.

All outputs are held in a high-impedance state or held at clamp levels during in-system programming.

OE/$\overline{\text{RESET}}$

The ISP programming algorithm requires issuance of a reset that will cause OE to go Low.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx HW-130, the Xilinx MultiPRO, or a third party device programmer. This provides the added flexibility of using pre-programmed devices in board design and boundary-scan manufacturing tools, with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 2,000 in-system program/erase cycles and a minimum data retention of ten years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading. Table 5 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set, it allows device erase. Erasing the entire device is the only way to reset the read security bit.

Table 5: **Data Security Options**

Default = Reset	Set
Read Allowed Program/Erase Allowed Verify Allowed	Read Inhibited via JTAG Program/Erase Allowed Verify Inhibited

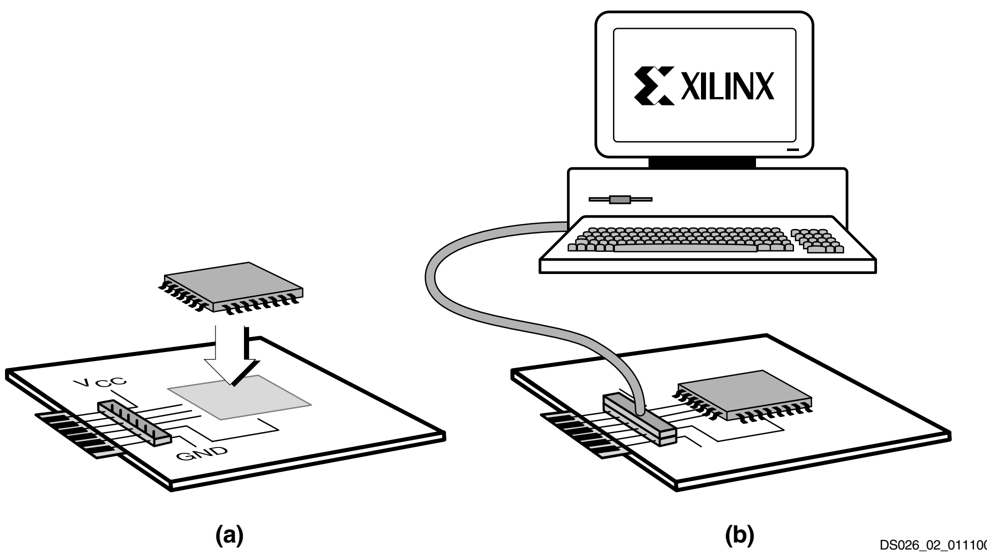

Figure 5: **In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

IEEE 1149.1 Boundary Scan (JTAG)

The XQR18V04 is fully compliant with the IEEE Std. 1149.1 Boundary Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary-scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the XQR18V04 device.

Table 6 lists the required and optional boundary-scan instructions supported in the XQR18V04. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Table 6: **Boundary Scan Instructions**

Boundary-Scan Command	Binary Code [7:0]	Description
Required Instructions		
BYPASS	11111111	Enables BYPASS
SAMPLE/ PRELOAD	00000001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables boundary-scan EXTEST operation
Optional Instructions		
CLAMP	11111010	Enables boundary-scan CLAMP operation
HIGHZ	11111100	All outputs in high-impedance state simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
XQR18V04 Specific Instructions		
CONFIG	11101110	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low

Instruction Register

The Instruction Register (IR) for the XQR18V04 is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 6.

The ISP Status field, IR[4], contains logic "1" if the device is currently in ISP mode; otherwise, it will contain logic "0". The Security field, IR[3], will contain logic "1" if the device has been programmed with the security option turned on; otherwise, it will contain logic "0".

	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	
TDI->	0 0 0	ISP Status	Security	0	0 1	->TDO

Notes:
1. IR[1:0] = 01 is specified by IEEE Std. 1149.1.

Figure 6: **Instruction Register Values Loaded into IR as Part of an Instruction Scan Sequence**

Boundary-Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the XQR18V04 has two register stages that contribute to the boundary-scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number

f = the family code (50h for the XQR18V04)

a = the ISP PROM product ID (26h for the XQR18V04)

c = the company code (49h for Xilinx)

Note: The LSB of the IDCODE register is always read as logic "1" as defined by IEEE Std. 1149.1

Table 7 lists the IDCODE register values for the XQR18V00 devices.

Table 7: **IDCODEs Assigned to XQR18V04 Devices**

ISP PROM	IDCODE
XQR18V04	05026093h

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the XQR18V04 device. If the device is blank or was not loaded during programming, the USERCODE register will contain FFFFFFFFh.

XQR18V04 TAP Characteristics

The XQR18V04 device performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the XQR18V04 TAP are described as follows.

TAP Timing

Figure 7 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

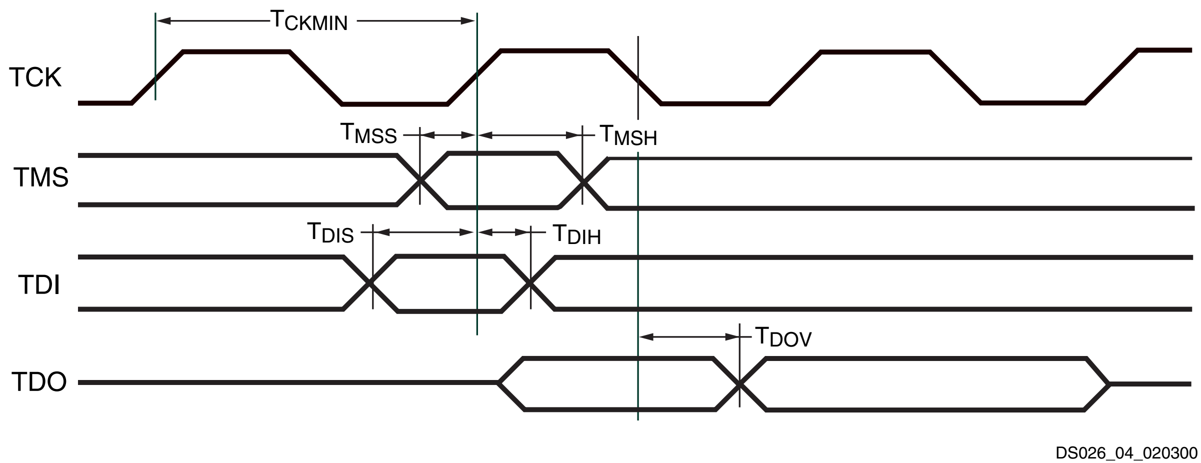

Figure 7: **Test Access Port Timing**

TAP AC Parameters

Table 8 shows the timing parameters for the TAP waveforms shown in Figure 7.

Table 8: **Test Access Port Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{CKMIN}	TCK minimum clock period	200	-	ns
T_{MSS}	TMS setup time	10	-	ns
T_{MSH}	TMS hold time	25	-	ns
T_{DIS}	TDI setup time	10	-	ns
T_{DIH}	TDI hold time	25	-	ns
T_{DOV}	TDO valid delay	-	25	ns

Absolute Maximum Ratings[1,2]

Table 9: **Absolute Maximum Ratings**

Symbol	Description		Value	Units
V_{CCINT}/V_{CCO}	Supply voltage relative to GND		–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND		–0.5 to +5.5	V
V_{TS}	Voltage applied to High-Z output		–0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature	Ceramic	+150	°C
		Plastic	+125	°C
T_{SOL}	Maximum soldering temperature		+220	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Table 10: **Recommended Operating Conditions**

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Internal voltage supply (T_C = –55°C to +100°C)	Ceramic	3.0	3.6	V
	Internal voltage supply (T_J = –55°C to +100°C)	Plastic	3.0	3.6	V
V_{CCO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCO}	V
T_{VCC}	VCCINT rise time from 0V to nominal voltage[1]		1	50	ms

Notes:

1. At power up, the device requires the VCCINT power supply to monotonically rise from 0V to nominal voltage within the specified VCCINT rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly.

Quality and Reliability Characteristics

Table 11: **Reliability Characteristics**

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	10	-	Years
N_{PE}	Program/erase cycles (Endurance)	2,000	-	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Table 12: **DC Characteristics**

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	-	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCO}	-	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{CC}	Supply current, active mode	25 MHz	-	50	mA
I_{CCS}	Supply current, standby mode		-	20	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO	$V_{CC =}$ MAX V_{IN} = GND	–100	-	µA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	Input and output High-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
C_{IN} and C_{OUT}	Input and output capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF

AC Characteristics Over Operating Conditions for XQR18V04

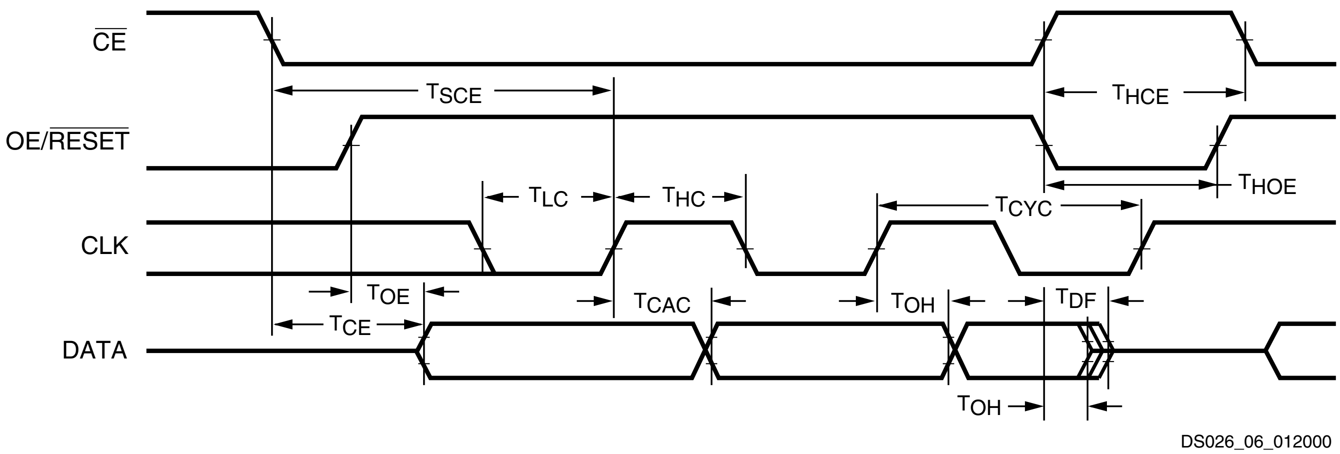

Figure 8: **Pin-to-Pin Timing Diagram**

Table 13: **AC Timing Characteristics for Single Device**

Symbol	Description	Min	Max	Units
T_{OE}	OE/RESET to data delay	-	10	ns
T_{CE}	CE to data delay	-	20	ns
T_{CAC}	CLK to data delay	-	20	ns
T_{OH}	Data hold from CE, OE/RESET, or CLK	0	-	ns
T_{DF}	CE or OE/RESET to data float delay(2)	-	25	ns
T_{CYC}	Clock periods	50	-	ns
T_{LC}	CLK Low time(3)	10	-	ns
T_{HC}	CLK High time(3)	10	-	ns
T_{SCE}	CE setup time to CLK (to guarantee proper counting)(3)	25	-	ms
T_{HCE}	CE High time (to guarantee proper counting)	2	-	µs
T_{HOE}	OE/RESET hold time (guarantees counters are reset)	25	-	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.

AC Characteristics Over Operating Conditions When Cascading for XQR18V04

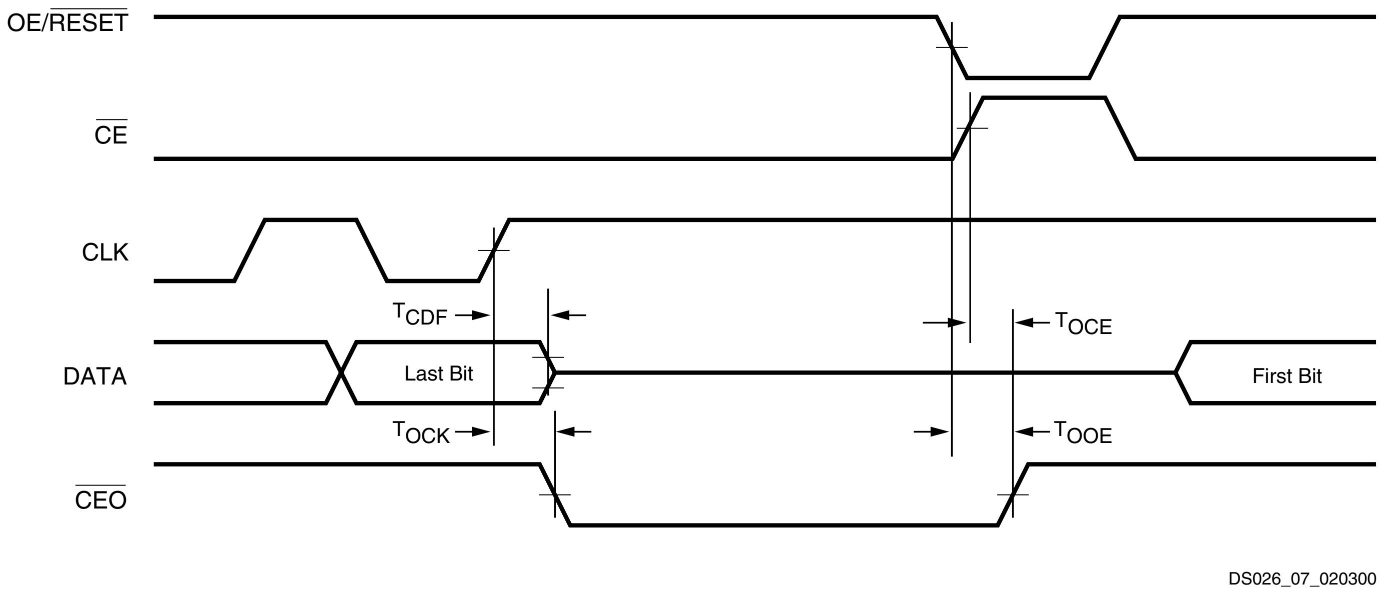

Figure 9: **Pin-to-Pin Timing Diagram for Cascaded Devices**

Table 14: **AC Timing Characteristics for Cascaded Devices**

Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	-	25	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	-	20	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	-	20	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3)	-	20	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Pinout and Pin Description

Table 15: **Pin Names and Descriptions (pins not listed are "no connect")**

Pin Name	Boundary Scan Order	Function	Pin Description	Pin Number	
				44-pin VQFP	44-pin CLCC
D0	4	DATA OUT	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.	40	2
	3	OUTPUT ENABLE			
D1	6	DATA OUT	D0-D7 are the output pins to provide parallel data for configuring a Xilinx FPGA in Express/SelectMap mode. D1-D7 remain in HIGHZ state and can be left unconnected when the PROM operates in serial mode.	29	35
	5	OUTPUT ENABLE			
D2	2	DATA OUT		42	4
	1	OUTPUT ENABLE			
D3	8	DATA OUT		27	33
	7	OUTPUT ENABLE			
D4	24	DATA OUT		9	15
	23	OUTPUT ENABLE			
D5	10	DATA OUT		25	31
	9	OUTPUT ENABLE			
D6	17	DATA OUT		14	20
	16	OUTPUT ENABLE			
D7	14	DATA OUT		19	25
	13	OUTPUT ENABLE			
CLK	0	DATA IN	Each rising edge on the CLK input increments the internal address counter if both $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High.	43	5
OE/$\overline{RESET}$	20	DATA IN	When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable.	13	19
	19	DATA OUT			
	18	OUTPUT ENABLE			
$\overline{CE}$	15	DATA IN	When $\overline{CE}$ is High, this pin puts the device into standby mode and resets the address counter. The DATA output pin is in a high-impedance state, and the device is in low-power standby mode.	15	21

Table 15: **Pin Names and Descriptions (pins not listed are "no connect")** ***(Continued)***

Pin Name	Boundary Scan Order	Function	Pin Description	Pin Number 44-pin VQFP	Pin Number 44-pin CLCC
$\overline{CF}$	22	DATA OUT	Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	10	16
	21	OUTPUT ENABLE			
$\overline{CEO}$	13	DATA OUT	Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. CEO returns to High when OE/RESET goes Low or CE goes High.	21	27
	14	OUTPUT ENABLE			
GND			GND is the ground connection.	6, 18, 28, 41	3, 12, 24, 34
TMS		TEST MODE SELECT	The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 Kohm resistive pull-up on it to provide a logic "1" to the device if the pin is not driven.	5	11
TCK		TEST CLOCK	This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	7	13
TDI		TEST DATA IN	This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 Kohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.	3	9
TDO		TEST DATA OUT	This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 Kohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.	31	37
V_{CCINT}			Positive 3.3V supply voltage for internal logic and input buffers.	17, 35, 38	23, 41, 44
V_{CCO}			Positive 3.3V or 2.5V supply voltage connected to the output voltage drivers.	8, 16, 26, 36	14, 22, 32, 42

Package Pin Diagrams

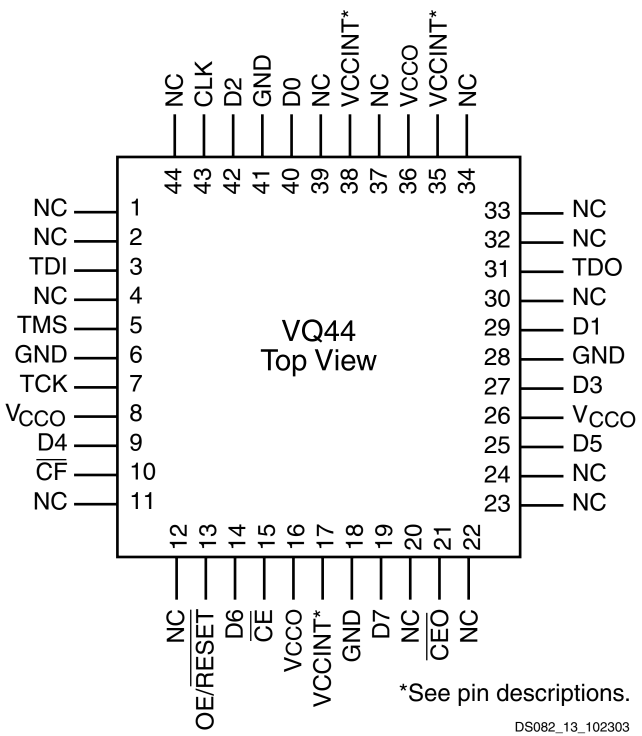

Figure 10: **Package Pinout for the XQR18V04VQ44**

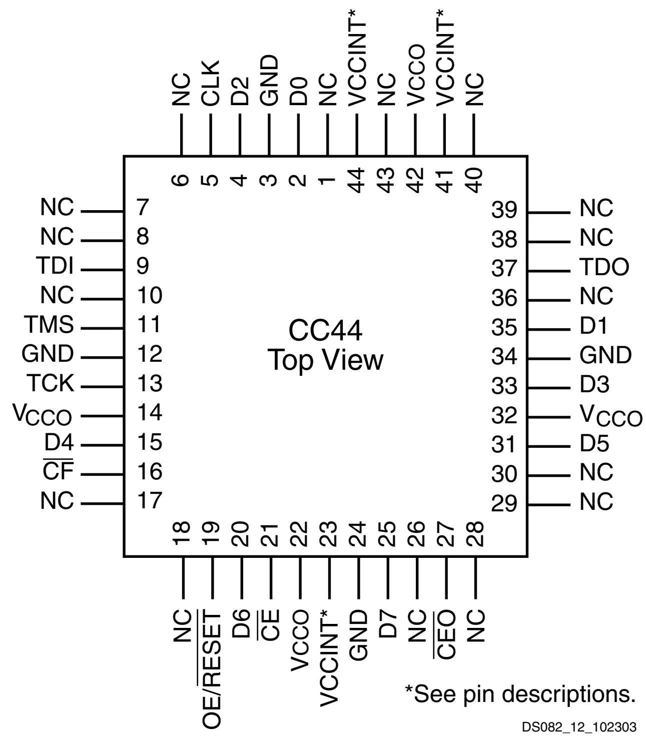

Figure 11: **Package Pinout for the XQR18V04CC44**

PROM Package Pinout Compatibility

Table 16: **PROM-to-PROM Pinout Compatibility for the CLCC44 Package**

CC44	XQR18V04	XQR17V16	XQR1701L
11	TMS	N/C	N/C
13	TCK	N/C	N/C
9	TDI	N/C	N/C
37	TDO	N/C	N/C
16	$\overline{CF}$	N/C	N/C
30	N/C	BUSY	N/C
12, 34	GND	GND	N/C
43	N/C	GND	N/C
41	V_{CCINT}	V_{PP}	V_{PP}
14, 22, 32, 42	V_{CCO}[1]	V_{CC}	N/C

1. The XQR18V04 supports 2.5-3.3V V_{CCO} operation. The XQR17V16 only supports 3.3V.

Table 17: **PROM-to-PROM Pinout Compatibility for the VQFP44 Package**

VQ44	XQR18V04	XQR17V16
5	TMS	N/C
7	TCK	N/C
3	TDI	N/C
31	TDO	N/C
10	$\overline{CF}$	N/C
24	N/C	BUSY
37	N/C	GND
35	V_{CCINT}	V_{PP}
8, 16, 26, 36	V_{CCO}[1]	V_{CC}

1. The XQR18V04 supports 2.5-3.3V V_{CCO} operation. The XQR17V16 only supports 3.3V.

Ordering Information

XQR18V04 CC44 V

Device Number — XQR18V04

Package Type — CC44

Manufacturing Grade — V

Device Ordering Options

Device Type
XQR18V04

Package	
CC44	44-pin Ceramic Chip Carrier Package
VQ44	44-pin Plastic Thin Quad Flat Package

Grade		
M	Military Ceramic	T_C = –55° C to +100° C
N	Military Plastic	T_J = –55° C to +100° C
V	QPro-Plus	T_C = –55° C to +100° C

Valid Ordering Combinations

XQR18V04
XQR18V04CC44M
XQR18V04CC44V
XQR18V04VQ44N

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
5/1/01	1.0	First publication of this early access specification
7/23/01	1.1	Preliminary publication supporting Full Mil Temp range and corrected write cycles
11/05/01	1.2	Added Class V to ordering combinations for Rad Hard version. Updated format.
6/18/02	1.3	Removed XQ18V04. Derated Temperature Range -55C to +100C. Removed SMD ordering information.
12/15/03	1.4	Updated TID and TCK specifications. Added table titles. Changed Product Description.