Signetics

FAST Products

FAST 74F1764/1765
74F1764-1/1765-1
1 Megabit DRAM Dual-Ported Controller

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing and refresh**
- **10 address output pins allow direct control of up to 1Mbit dynamic RAMs**
- **External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **74F1764/F1764-1 have on-chip 20-bit address input latch**
- **Allows control of dynamic RAMS with row access times down to 40ns**
- **74F1764/F1765 output drivers designed for incident wave switching**
- **74F1764-1/F1765-1 output drivers designed for first reflected wave switching**

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

ORDERING INFORMATION

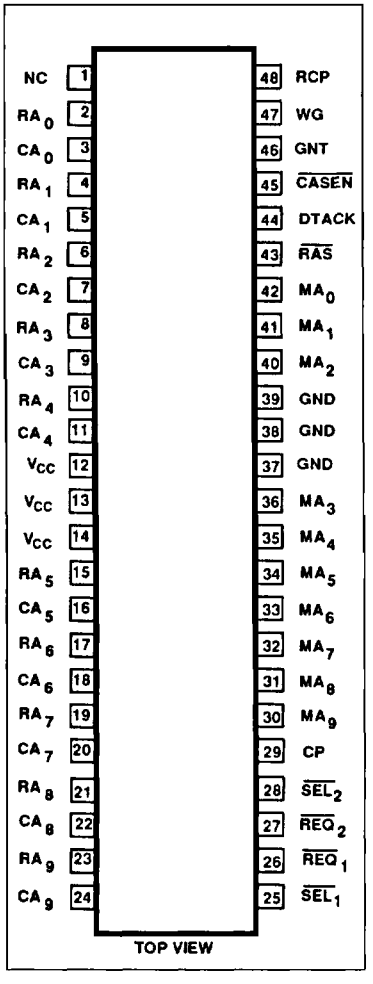
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

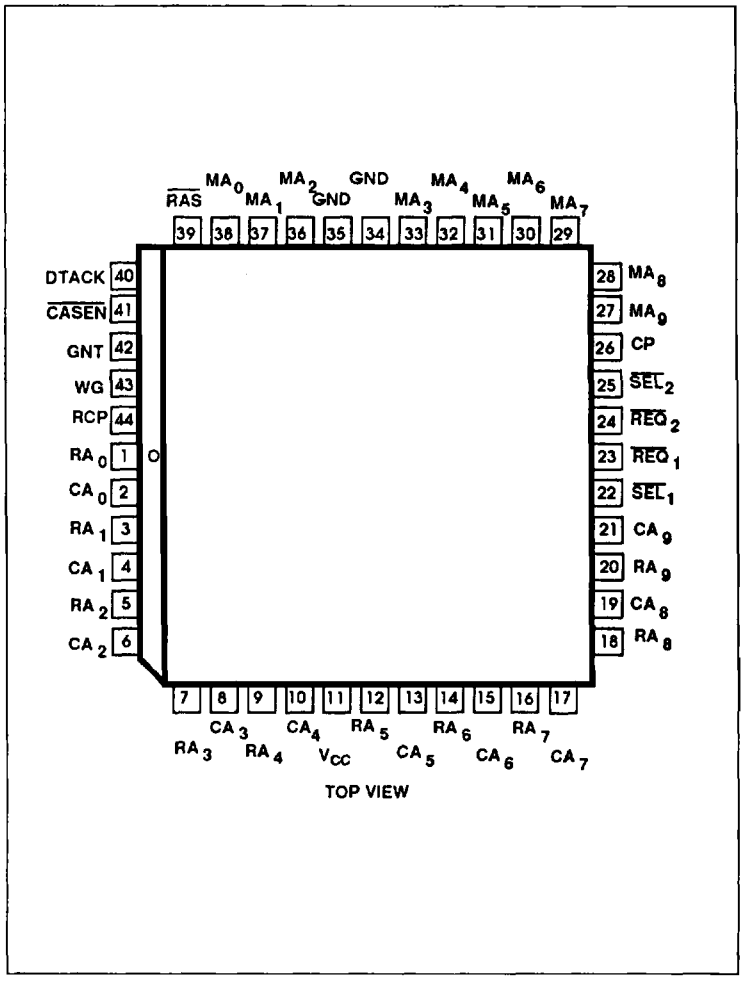
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_9		Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_9		Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{REQ_1}$, $\overline{REQ_2}$		Memory access request inputs	1.0/1.0	20µA/0.6mA
CP		Clock input	1.0/1.0	20µA/0.6mA
RCP		Refresh clock input	1.0/1.0	20µA/0.6mA
$\overline{SEL_1}$, $\overline{SEL_2}$	*F1764/1765	Select outputs	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3[1]	20.0mA/8mA
MA_0 - MA_9	*F1764/1765	Memory address outputs	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA
GNT	*F1764/1765	Grant output	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{RAS}$	*F1764/1765	Row address strobe output	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA
WG	*F1764/1765	Write gate output	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{CASEN}$	*F1764/1765	Column address strobe enable output	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA
DTACK	*F1764/1765	Data transfer acknowledge output	750/40	15.0mA/24mA
	*F1764-1/1765-1		1000/13.3	20.0mA/8mA

NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

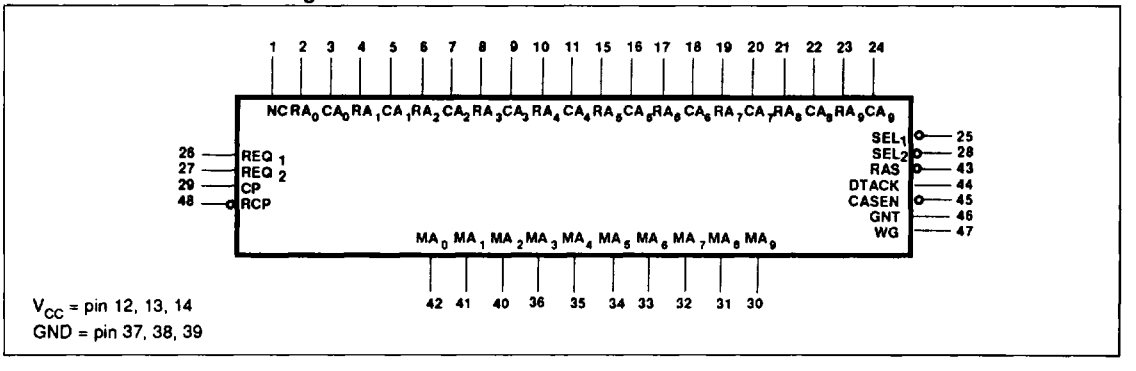
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



LOGIC SYMBOL for N Package



PIN DESCRIPTION

SYMBOL	PINS DIP	PINS PLCC	TYPE	NAME AND FUNCTION
RA_0	2	1	Inputs	Address inputs used to generate memory row address
RA_1	4	3		
RA_2	6	5		
RA_3	8	7		
RA_4	10	9		
RA_5	15	12		
RA_6	17	14		
RA_7	19	16		
RA_8	21	18		
RA_9	23	20		
CA_0	3	2	Inputs	Address inputs used to generate memory column address
CA_1	5	4		
CA_2	7	6		
CA_3	9	8		
CA_4	11	10		
CA_5	16	13		
CA_6	18	15		
CA_7	20	17		
CA_8	22	19		
CA_9	24	21		
$\overline{REQ}_1$	26	23	Input	Memory acess request from Microprocessor 1
$\overline{REQ}_2$	27	24	Input	Memory acess request from Microprocessor 2
CP	29	26	Input	Clock input which determines the master timing
RCP	48	44	Input	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	25	22	output	Select signal is activated in response to active REQ_1 input indicating selection of Microprocessor 1
$\overline{SEL}_2$	28	25	output	Select signal is activated in response to active REQ_2 input indicating selection of Microprocessor 2
MA_0	42	38	Outputs	Memory address outputs designed to drive address lines of the DRAM
MA_1	41	37		
MA_2	40	36		
MA_3	36	33		
MA_4	35	32		
MA_5	34	31		
MA_6	33	30		
MA_7	32	29		
MA_8	31	28		
MA_9	30	27		
$\overline{GNT}$	46	42	Output	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	43	39	Output	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the RAS inputs of the DRAMs)
WG	47	43	Output	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	45	41	Output	Column address Strobe Address Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	Output	Data Transfer Acknowledge indicates that the data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on differenrt edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figure 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:
(tras (of the DRAM) + 16-5)/4 plus any system guard-band required.

For the 74F1764-1/1765-1 the CP clock input period should be equal to:
(Tras (of the DRAM) + 22-10)/4 plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until the completion of the refresh cycle (see Figures 8 and 9).

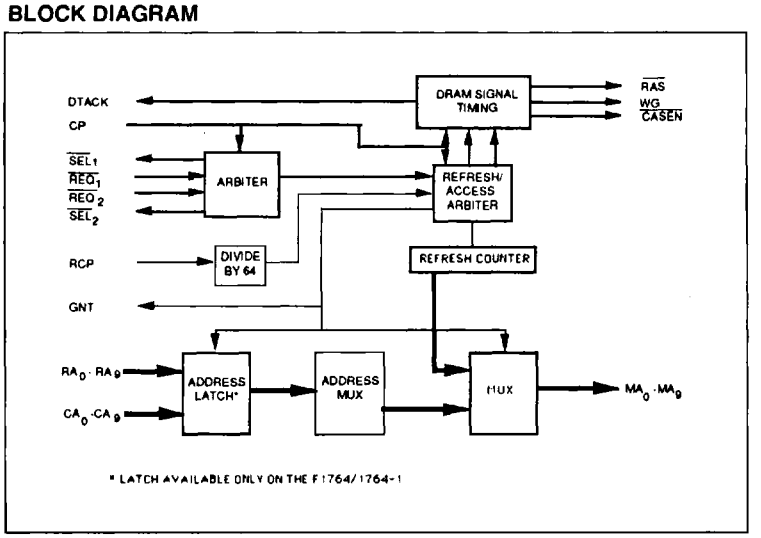
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will insure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If ,however, there are any pending refresh requests, assertion of the GNT output will be held OFF until the refresh has been serviced.

When GNT goes High, the RA_0-RA_9 and CA_0-CA_9 address input to the 'F1764/'F1764-1 are latched internally and the RA_0-RA_9 signals are propagated to the MA_0-MA_9 outputs. The address inputs are not latched by the 74F1765/F1765-1 and therefore, RA_0-RA_9 inputs propagate directly to the MA_0-MA_9 outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



One clock cycle later, the CA_0-CA_9 latch outputs on the 'F1764 and 'F1764-1 or CA_0-CA_9 inputs to the 'F1765 and 'F1765-1 are selected and propagated to the MA_0-MA_9 outputs. The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

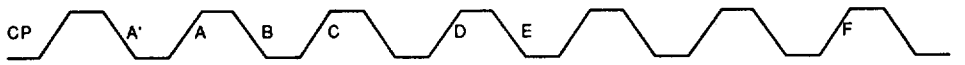
A half-clock cycle is again allowed for the CA_0-CA_9 signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with higher order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2 and one-half clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High.

When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 10 refresh counter address signals to the MA_0-MA_9 outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMS (see Figures 3 and 4).

TIMING SEQUENCE

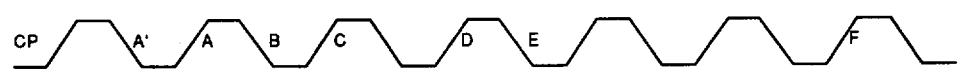


A' $\overline{REQ_2}$ sampled
A $\overline{REQ_1}$ sampled
SEL_1 triggered (SEL_1 triggered by $\overline{REQ_1}$ sample circuitry) ($\overline{REQ_2}$ disabled by SEL_1 circuitry)
B GNT triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 1. Sequence of Events for $\overline{REQ_1}$ Memory Access Cycle

TIMING SEQUENCE

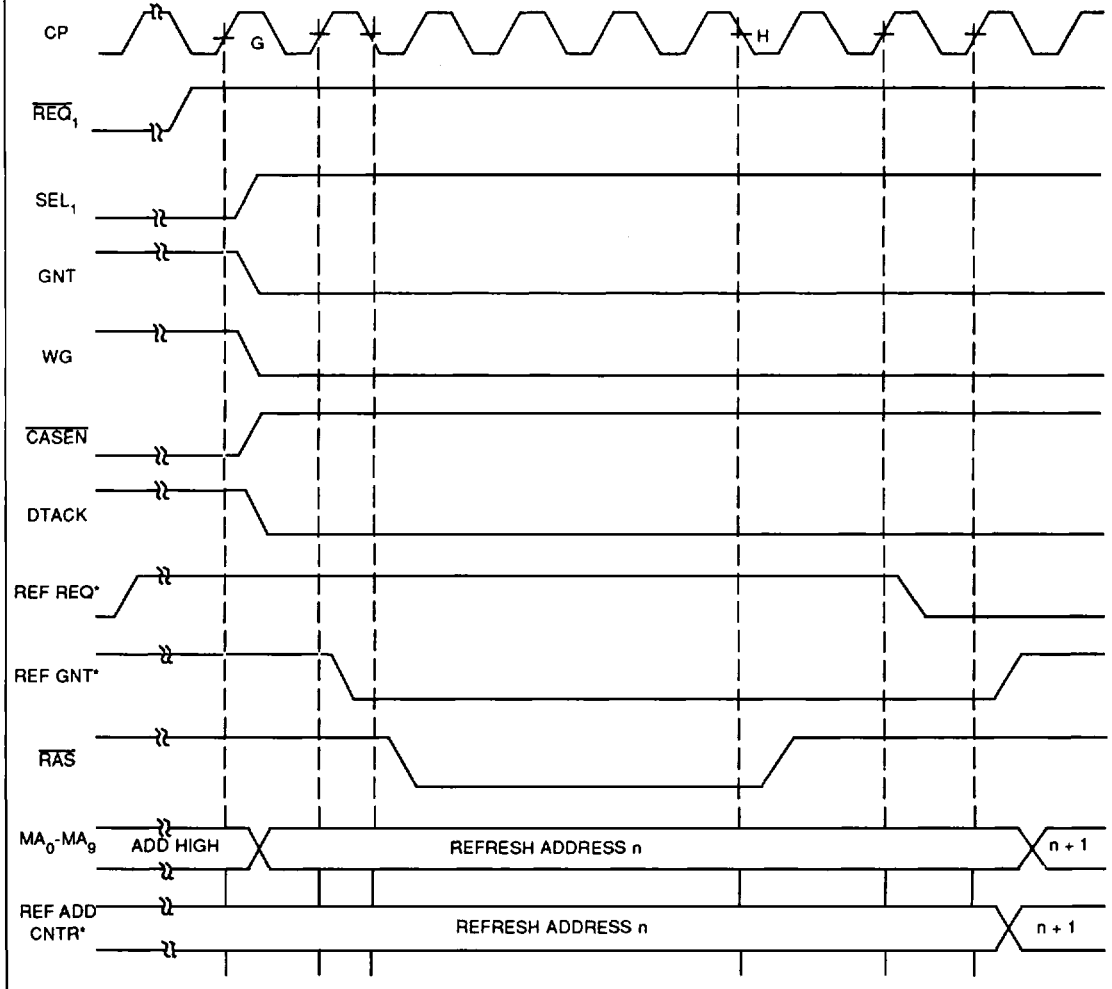


A' $\overline{REQ_2}$ sampled
SEL_1 triggered (SEL_2 triggered by $\overline{REQ_2}$ sampling circuitry)
A $\overline{REQ_1}$ is not sampled(disabled by SEL_2 circuitry)
B GNT triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 2. Sequence of Events for $\overline{REQ_2}$ Memory Access Cycle

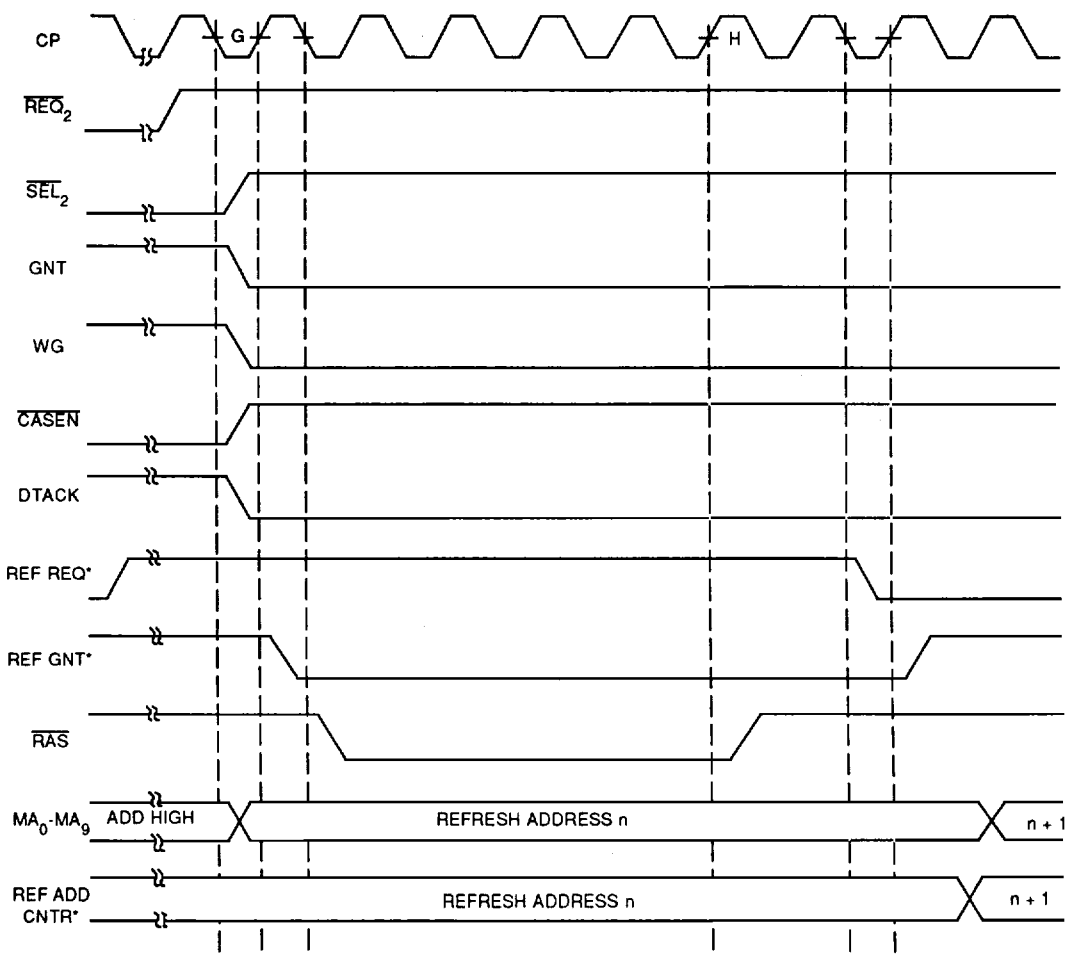
TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 3. Refresh Cycle Timing Following a $\overline{REQ}_1$ Memory Access Cycle

TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 4. Refresh Cycle Timing Following a $\overline{REQ}_2$ Memory Access Cycle

Using 74F1764/1765 AND 74F1764-1/ 1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address 4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However, it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.

APPLICATION

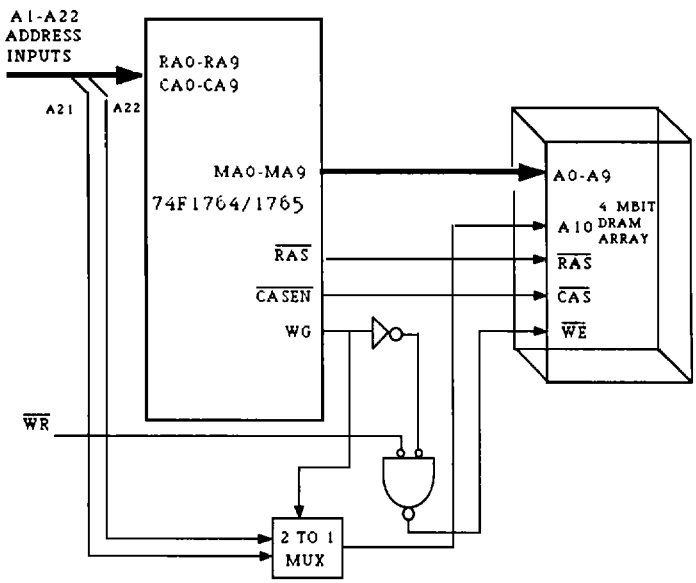


Figure 5. Using the Controller to Address 4Mbit DRAMS

TIMING DIAGRAM

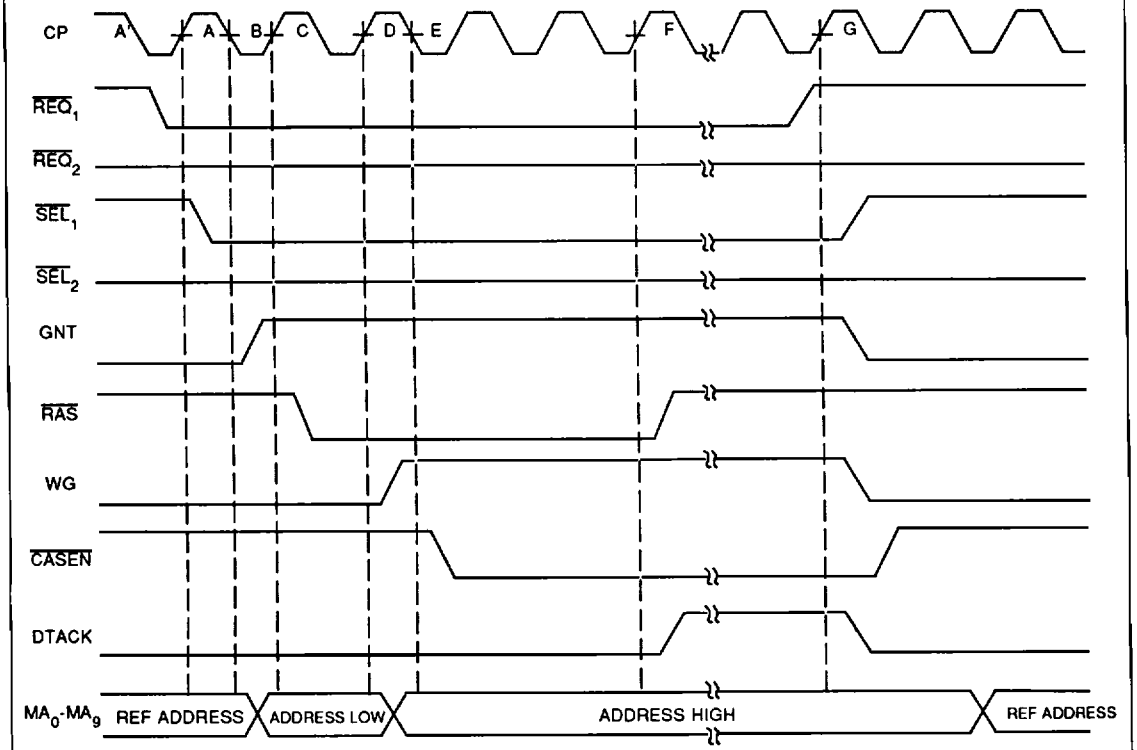


Figure 6. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing

TIMING DIAGRAM

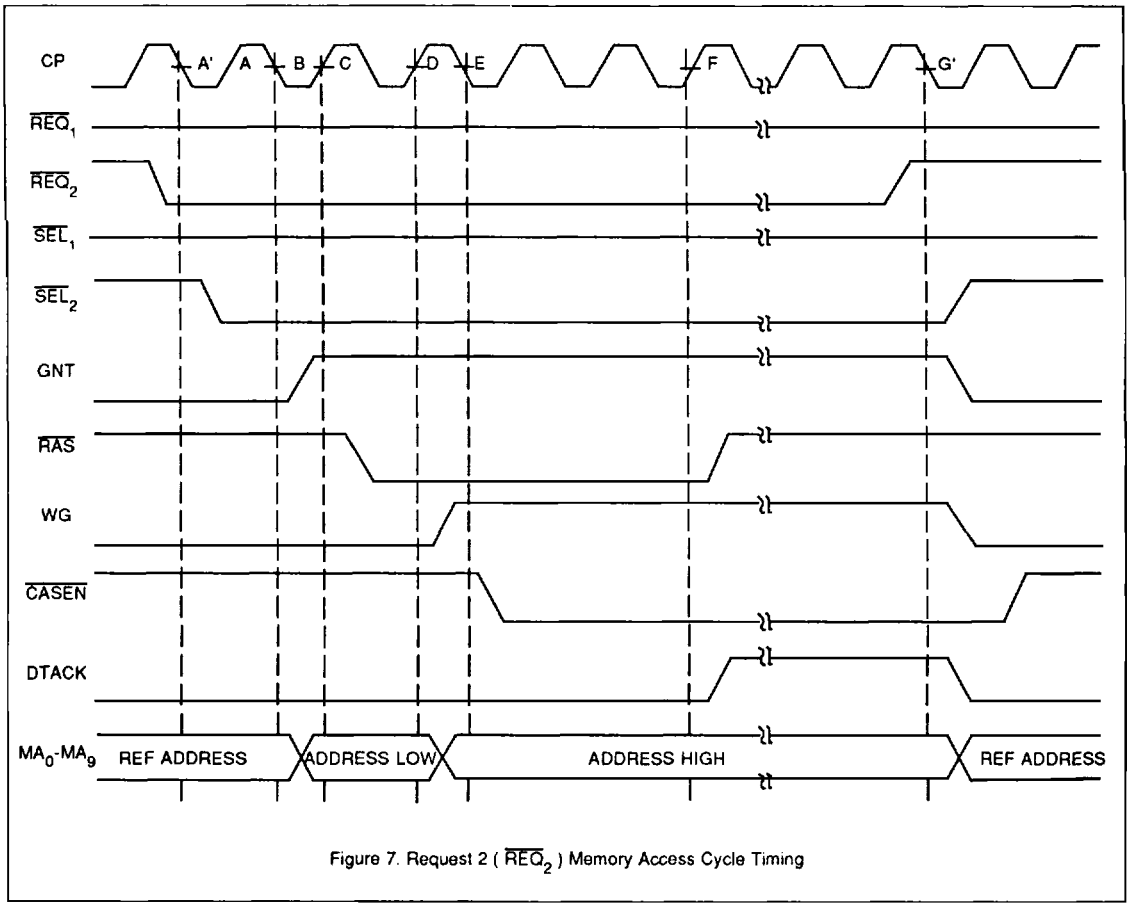


Figure 7. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing

TIMING DIAGRAM

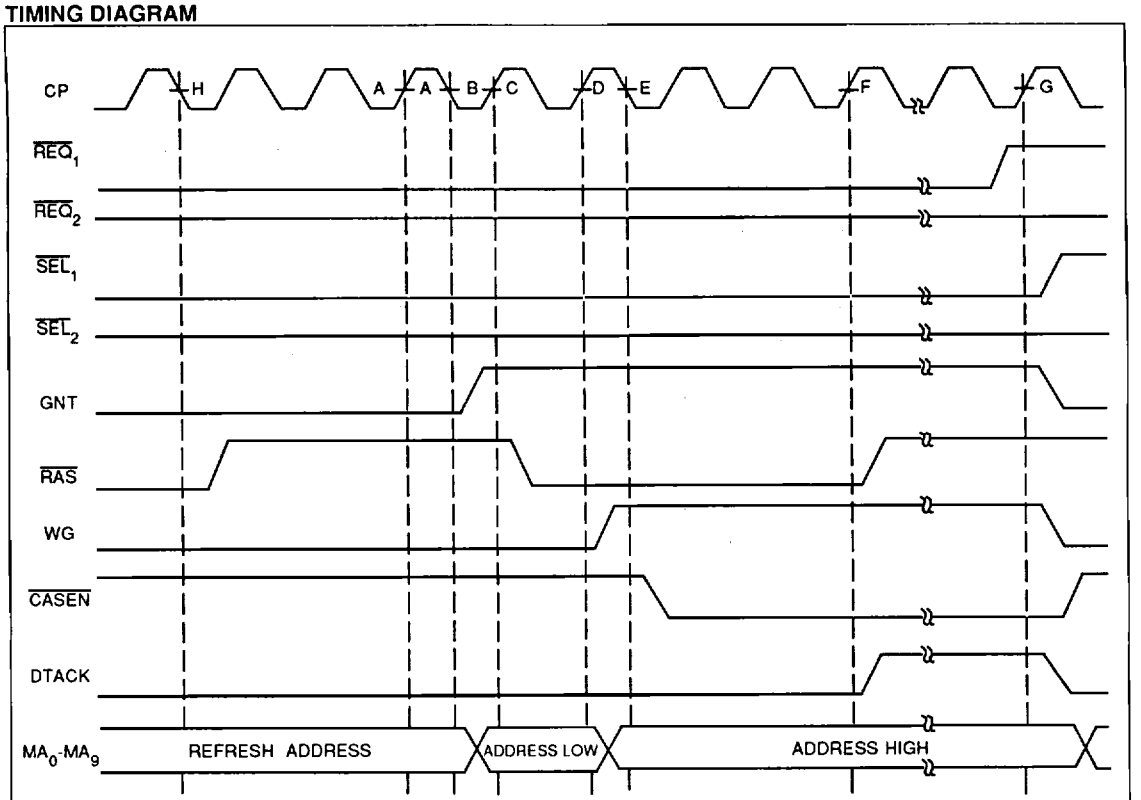


Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing Following a refresh Cycle

TIMING DIAGRAM

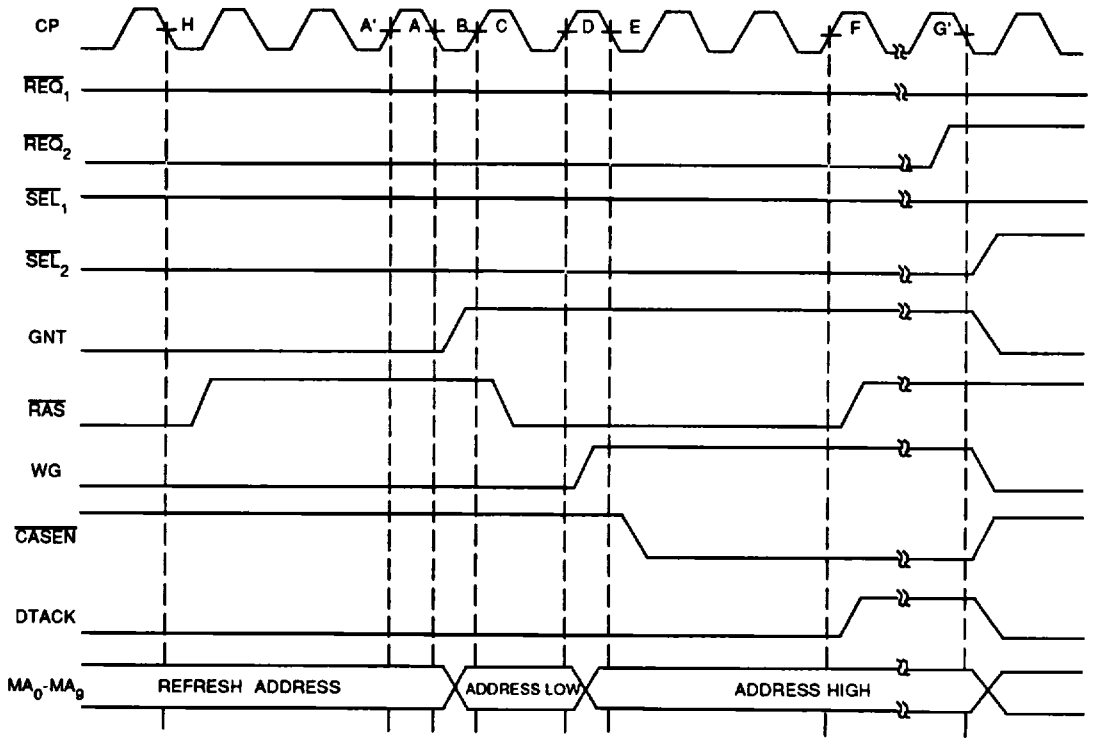


Figure 9. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing Following a refresh Cycle

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current[1]	74F1764/74F1765			-15	mA
		74F1764-1/74F1765-1			-20	mA
I_{OL}	Low-level output current[1]	74F1764/74F1765			24	mA
		74F1764-1/74F1765-1			8	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7			V
V_{OH2}[3]					I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}			74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-20mA	±10%V_{CC}	2.4	2.7		V
						±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
					I_{OL2}[4]=60mA	±5%V_{CC}		0.45	0.80	V
			74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=8mA	±10%V_{CC}		0.30	0.50	V
						±5%V_{CC}		0.30	0.50	V
V_{OH2}[3]					I_{OL2}[3]=75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[5]		74F1764 74F1765	V_{CC} =MAX			-100		-225	mA
			74F1764-1 74F1765-1	V_{CC} =MAX			-60	100	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F1764 74F1765	V_{CC} =MAX				150	200	mA
		I_{CCL}						165	210	mA
		I_{CCH}	74F1764-1 74F1765-1					120	165	mA
		I_{CCL}						125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		100	150		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		5.0	10.0	15.0	5.0	16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		5.0 5.0	12.0 11.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		8.0	13.0	17.0	8.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		5.0 5.0	12.0 10.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		7.0	17.0	23.0	7.0	25.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		6.0	13.0	17.0	5.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9 (74F1765 only)		4.0 2.0	7.0 5.0	12.0 8.0	4.0 4.0	13.0 9.0	ns

AC SETUP REQUIREMENTS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP		2.0 2.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764 only)		-4.0[1] -4.0			-5.0 -5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764 only)		5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	RCP Pulse width, High or Low		10.0 10.0			10.0 10.0		ns

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

AC ELECTRICAL CHARACTERISTICS for 74F1764-1/74F1765-1

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		150	175		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL}_1$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL}_1$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL}_2$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL}_2$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		9.0	12.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		20.0	23.0	26.0	17.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		11.0 14.0	14.0 18.0	17.0 22.0	10.0 13.0	19.0 24.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		11.0	14.0	16.0	10.0	18.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		13.0	17.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		9.0	11.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		20.0	23.0	26.0	19.0	26.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		12.0 14.0	14.0 18.0	17.0 21.0	11.0 13.0	19.0 23.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		14.0	17.0	20.0	12.0	22.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		14.0	16.0	19.0	13.0	21.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		10.0	12.0	15.0	9.0	17.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		20.0	23.0	26.0	19.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9	'F1765-1 only	9.0 9.0	11.0 12.0	14.0 15.0	8.0 8.0	16.0 17.0	ns

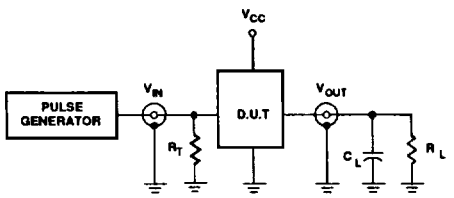
AC SETUP REQUIREMENTS for 74F1784-1/74F1765-1

SYMBOL	PARAMETER		TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP			3.0 3.0	1.0 1.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP			2.0 2.0	0 0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP	74F1764-1 only		0 0	-1.0[1] -1.0[1]		1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP	74F1764-1 only		5.0 5.0	3.0 3.0		6.0 6.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low			5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_w(H)$ $t_w(L)$	RCP Pulse width, High or Low			5.0 5.0			5.0 5.0		ns

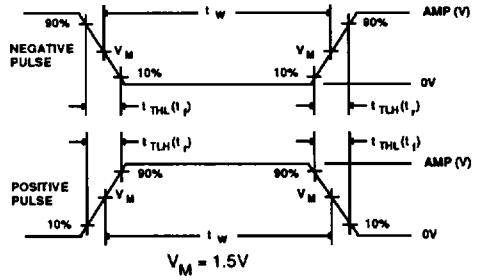
NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be deigned into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows two 68000 processors sharing a 4Meg X 8 (two banks each consisting of sixteen 1 Meg devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F 1765/'F1765-1 is appropriate.

Address bit (A21) from either the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes (UDS and LDS) from either of the two 68000 determine whether a byte or word transfer will take place. The additional circuitry is to ensure that DTACK to the 68000 is asserted only when it is selected.

Figure 11 shows two 8086 processors sharing 1 Mbyte (two banks each consisting of sixteen 256K X 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly Figure 12 shows two 6020 processors sharing 4Mbyte of memory.

APPLICATION

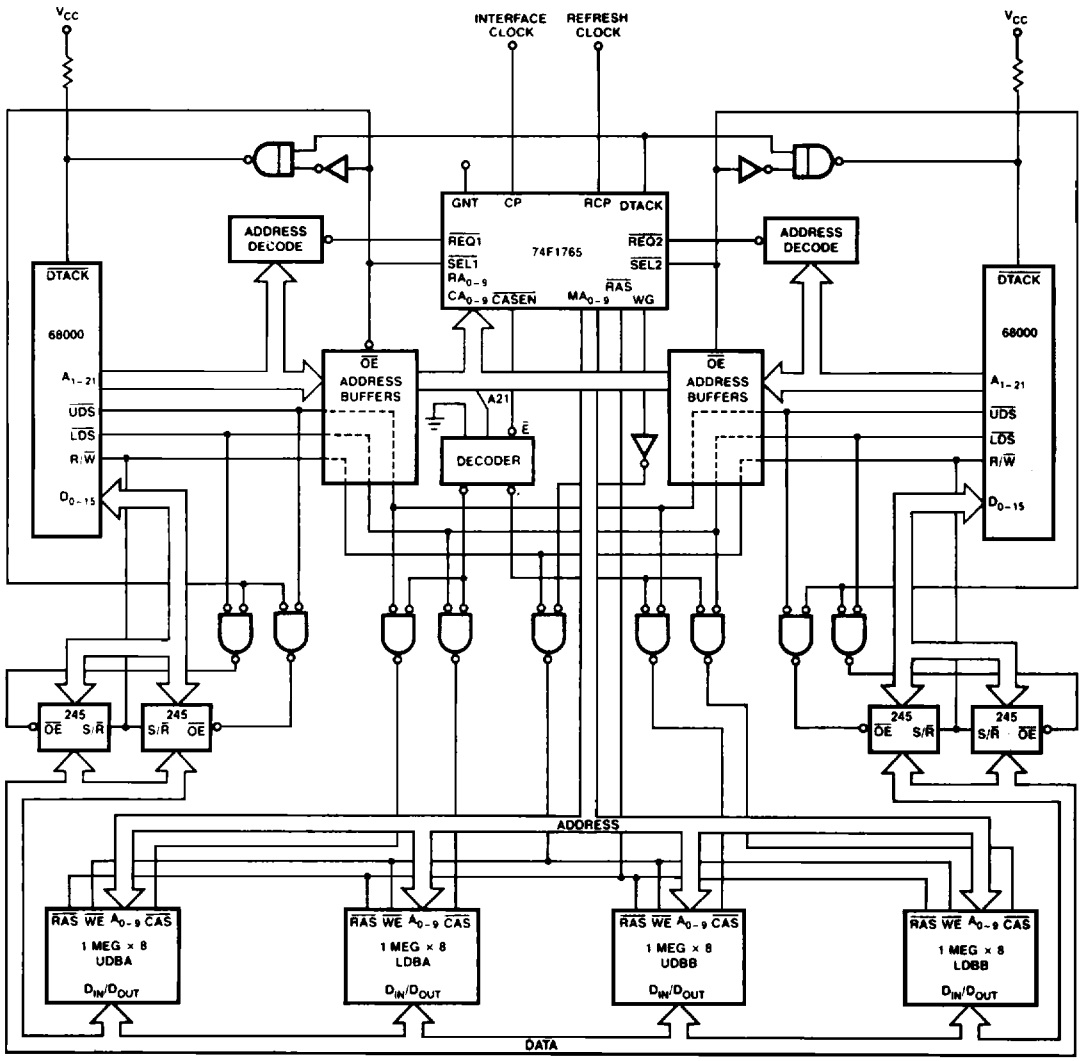
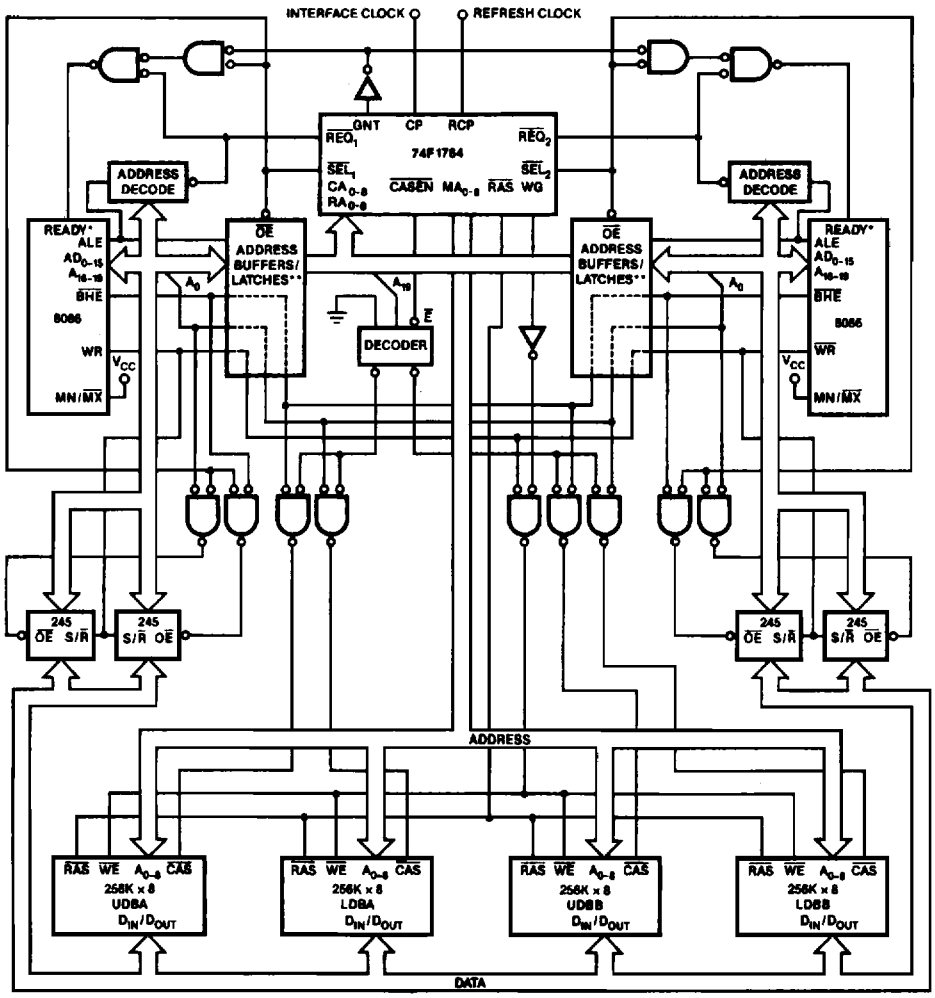


Figure 12. Two 68000 Processors Sharing 4Mbyte of DRAM

APPLICATION



Notes:
*= It might be necessary ti synchronize READY by the 8284A. Please refer to the 8086 data sheet.
**= Whether or not the 8086 address needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller

Figure 11. Two 8086 Processors Sharing 1Mbyte of DRAM

APPLICATION

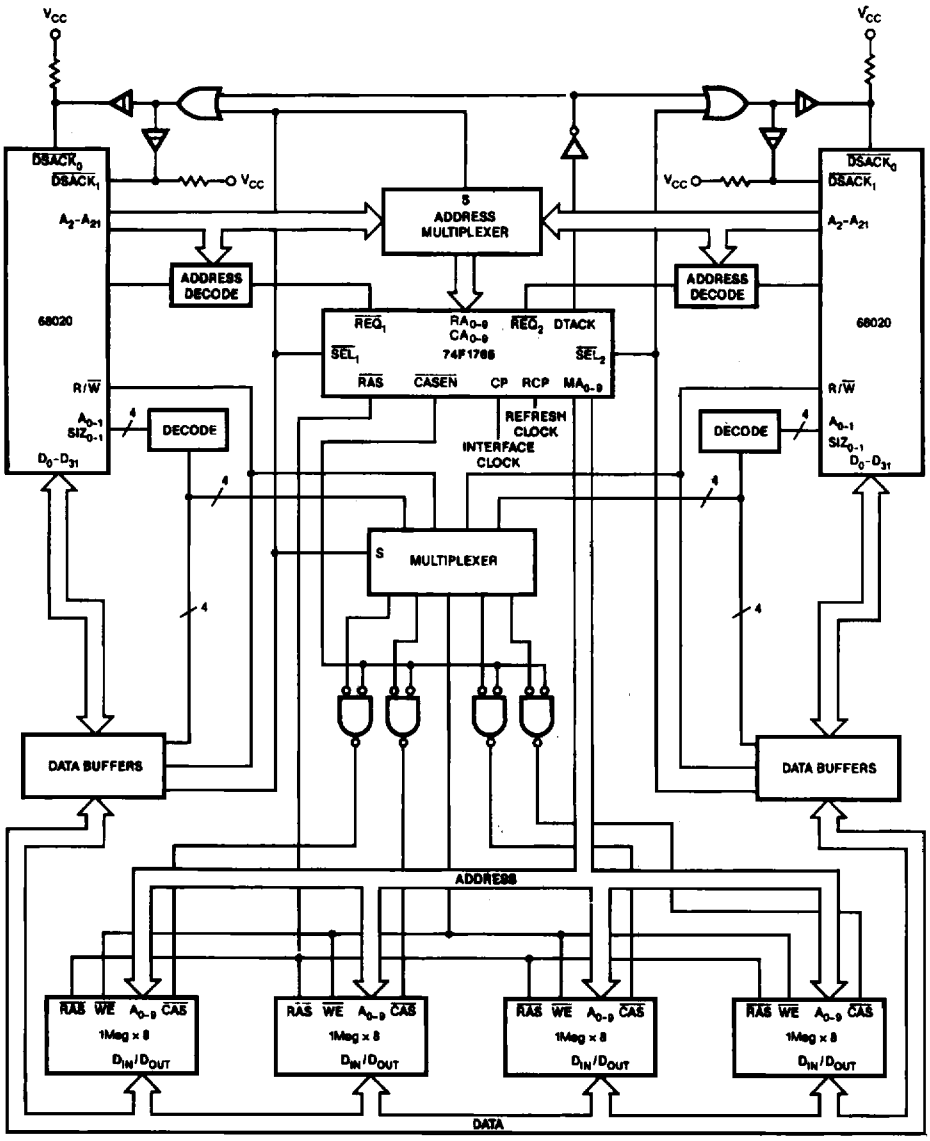


Figure 12. Two 68020 Processors Sharing 4Mbyte of DRAM

APPENDIX A

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide wave switching in dual-in package (DIP) or zig-zag in-line package (ZIP) housed memory arrays and first reflected wave switching in single in-line package (SIP) or single in-line module(SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristics impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4V and must be pulled down to 0.8V or less on the incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8V. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be swithced on the incidient wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady-state operation at these currents may result in electromigration).

Figures 1-4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F1764/1765 driving a dual in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, The Schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5-7 are double exposures showing the High to Low to High transitions while driving four banks of eight dual in-line packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300 pF to ground (the worst of the four branches is shown).

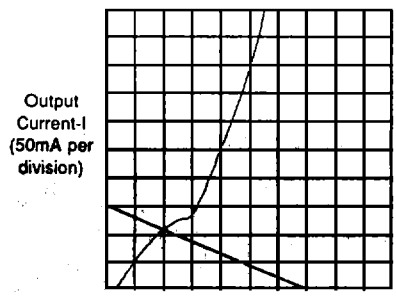


Figure 1.
I-V Output Characteristics of the 74F1764/1765 in the Low state. Light line is the I-V Curve of a 25Ω transmission line settled to 3.5V (typical for recommended termination). The High to Low incident wave on this line will typically be to 0.8V.

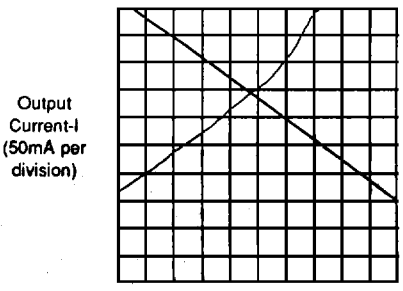


Figure 2.
I-V Output Characteristics of the 74F1764/1765 in the High state. Light line is the I-V Curve of a 35Ω transmission line settled to 0.25V . The incident wave on the Low to High transition will typically be to 2.4V on this line. Any line over 35Ω will typically be switched on the incident wave.

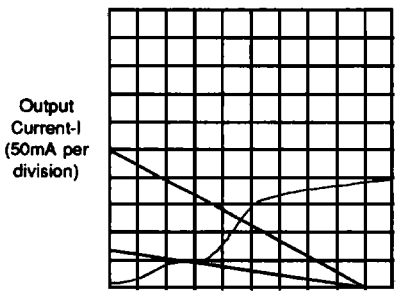


Figure 3.
I-V Output Characteristics of the 74F1764-1/1765-1 in the Low state. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs

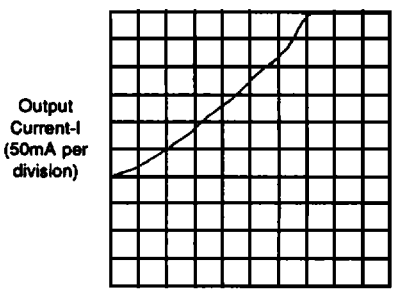


Figure 4.
I-V Output Characteristics of the 74F1764-1/1765-1 in the High state.

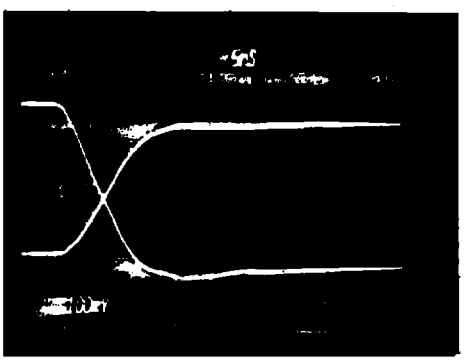


Figure 5.
74F1764-1/1765-1 Driving 32 DRAMS (Unterminated)

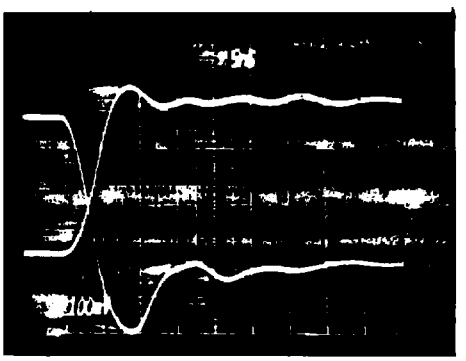


Figure 6.
74F1764/1765 Driving 32 DRAMS (Unterminated)

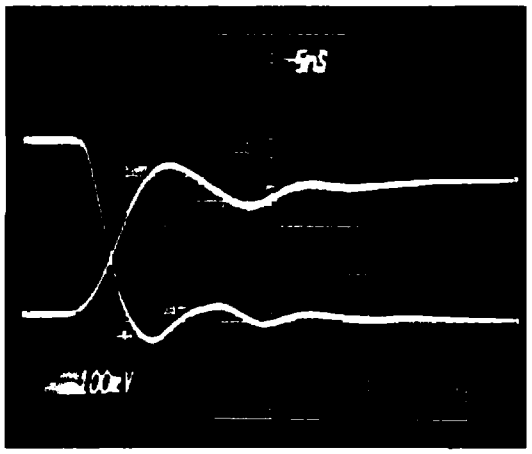


Figure 7.
74F1764/1765 Driving 32 DRAMS (Terminated as in Figure 8a)

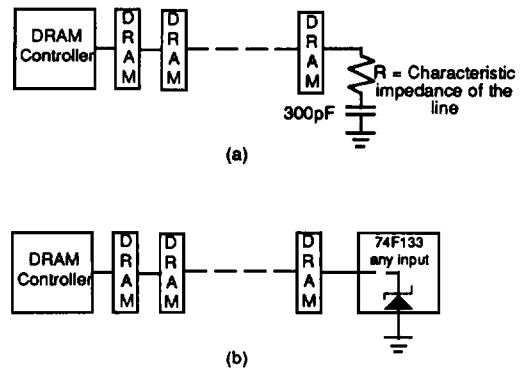


Figure 8.
74F1764/1765 Driving 32 DRAMS (Unterminated)