

DESCRIPTION

The HYM5V72A120A is a 1M x 72-bit Fast page mode CMOS DRAM module consisting of two HY51V4400B in 20/26 pin SOJ or TSOP-II, four HY51V18160B 42/42 pin SOJ or 44/50 pin TSOP-II and two 16-bit BiCMOS line driver in TSSOP on a 168 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM. The HYM5V72A120AXG/ASLXG/ATXG/ASLTXG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- Low power dissipation
 - Max. self-refresh 7.13mW (SL-part)
 - Max. battery back-up 8.57mW (L-part)
 - Max. CMOS standby 4.61mW (L-part)
22.32mW
 - Max. TTL standby 43.85mW

Max. operating

Speed	Power
60	3.13W
70	2.77W
80	2.41W

- Single power supply of 3.3V± 10%
- TTL compatible inputs and outputs
- Fast access time

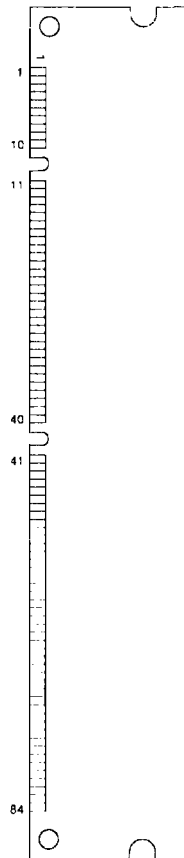
Speed	tRAC	tCAC	tPC
60	60ns	20ns	40ns
70	70ns	25ns	45ns
80	80ns	25ns	50ns

- Fast page mode operation
- CAS-before-RAS, RAS-only and Hidden refresh and Self-refresh
- 1024 refresh cycles / 256ms (SL-part)
1024 refresh cycles / 16ms
- Buffered inputs (except RAS and DQ)
- 4 Byte interleave enabled, Dual address inputs(A0,B0)

PIN DESCRIPTION

RAS0,RAS2	Row Address Strobe
CAS0,CAS4	Column Address Strobe
WE0,WE2	Write Enable
OE0,OE2	Output Enable
A0-A9,B0	Address Input
DQ0-DQ71	Data Input/Output
PD1-PD8	Presence Detect
PDE	Presence Detect Enable
ID0,ID1	ID Bit
Vcc	Power (+ 3.3V)
Vss	Ground

PIN CONNECTION



PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ36	128	NC
3	DQ1	45	RAS2	87	DQ37	129	NC
4	DQ2	46	CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	Vcc	48	WE2	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ28	111	NC	153	DQ64
28	CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0	72	DQ31	114	NC	156	DQ67
31	OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0(Vss)	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

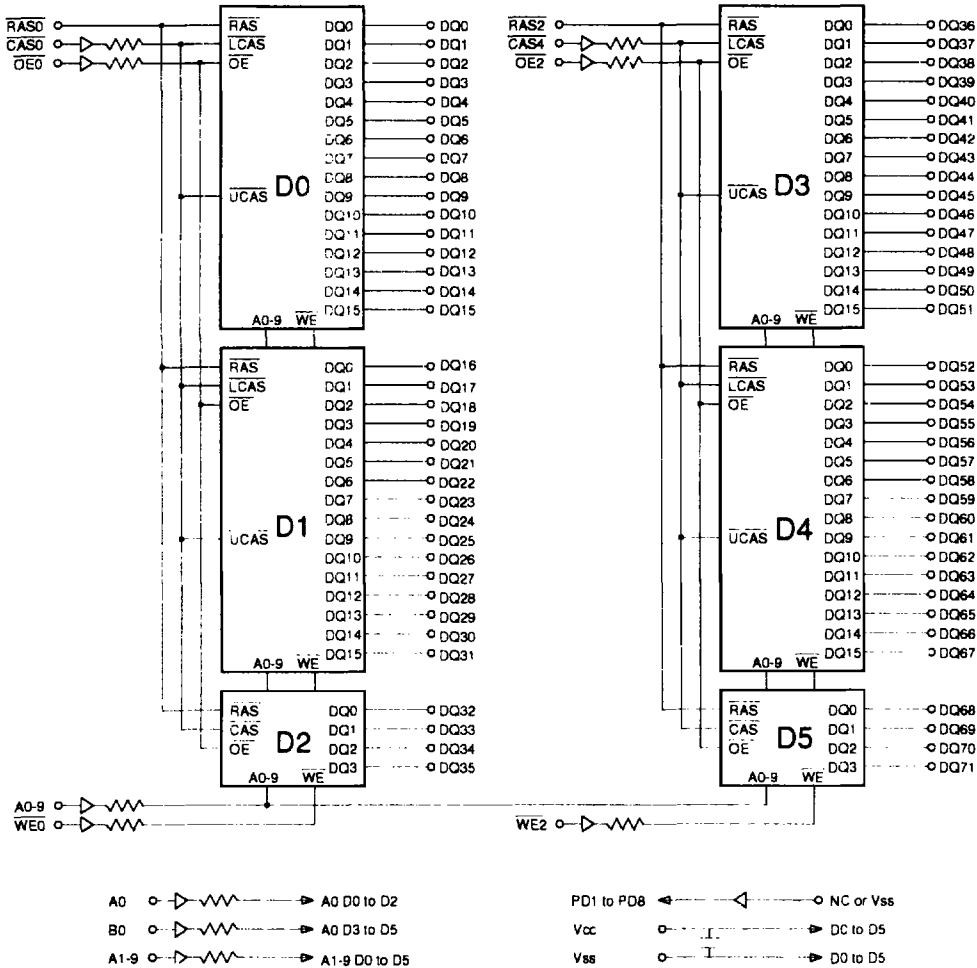
PRESENCE DETECT PINS

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
-60	Vss	Vss	NC	Vss	Vss	NC	NC	Vss	Vss	Vss or NC
-70	Vss	Vss	NC	Vss	Vss	Vss	NC	Vss	Vss	Vss or NC
-80	Vss	Vss	NC	Vss	Vss	NC	Vss	Vss	Vss	Vss or NC

NOTE :

1. PDs are either open NC or driven to Vss via on-board buffer circuits.
2. IDs are connected directly to Vss without a buffer.
3. ID1 will be either open NC for Self-Refresh or driven to Vss for Standard.

BLOCK DIAGRAM



NOTE : All resistors are 25 Ohm± 5%

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 4.6	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 4.6	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	6.3	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, other pins not under test= VSS	All but RAS RAS	-10 -30	10 30	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-20	20	μA	
Icc1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	870 770 670	mA	1,2,3
Icc2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	12.2	mA	
Icc3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	- - -	870 770 670	mA	1,3
Icc4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	60 70 80	- - -	570 510 450	mA	1,2,3
Icc5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	-	6.2 1.3	mA	
Icc6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	- - -	870 770 670	mA	1,3
Icc7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 250μs, tRAS ≤ 1μs CAS= CBR cycling or 0.2V OE & WE= VCC-0.2V, 3.2 A0-A9= VCC-0.2V, 0.2V DQ0-DQ71= 0.2V, VCC-0.2V or open		-	2.4	mA	1,4,5
Icc8	VCC Supply Current, Self-Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as Icc7		-	1.98	mA	5
VOL	Output Low Voltage	IOL= 2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2mA		2.4	-	V	

NOTE :

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4, and Icc6 depend on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. for Icc1, Icc3, and Icc6, address can be changed maximum two times while RAS= VIL for Icc4, address can be changed maximum once while CAS= VIH.
- Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operation.
- Icc5(max.)= 1.3mA and Icc7 are applied to SL-part only (HY5V72A120 ASLXG/ASLTXG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V72A120A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWc	Read-Modify-Write Cycle Time	163	-	178	-	208	-	ns	14,15
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	83	-	83	-	103	-	ns	13,15
5	tRAC	Access Time from $\overline{\text{RAS}}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{\text{CAS}}$	-	20	-	25	-	25	ns	4,9,15
7	tAA	Access Time from Column Address	-	36	-	41	-	46	ns	4,10,15
8	tCPA	Access Time from $\overline{\text{CAS}}$ Precharge	-	40	-	40	-	50	ns	4,15
9	tCLZ	$\overline{\text{CAS}}$ to Output Low Impedance	2	-	2	-	2	-	ns	4,13
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5,17
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3,12
12	tRP	$\overline{\text{RAS}}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{\text{RAS}}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{\text{RAS}}$ Hold Time	20	-	25	-	25	-	ns	15
16	tCSH	$\overline{\text{CAS}}$ Hold Time	58	-	68	-	78	-	ns	14
17	tCAS	$\overline{\text{CAS}}$ Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	13	40	18	45	18	55	ns	9,16
19	tRAD	$\overline{\text{RAS}}$ to Column Address Delay Time	13	24	13	29	13	34	ns	10,16
20	tCRP	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15	-	15	-	25	-	ns	15
21	tCP	$\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	6	-	6	-	6	-	ns	15
23	tRAH	Row Address Hold Time	8	-	8	-	8	-	ns	14
24	tASC	Column Address Set-up Time	2	-	2	-	2	-	ns	13
25	tCAH	Column Address Hold Time	17	-	17	-	17	-	ns	13
26	tAR	Column Address Hold Time from $\overline{\text{RAS}}$	52	-	57	-	57	-	ns	14
27	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	36	-	41	-	46	-	ns	15
28	tRCS	Read Command Set-up Time	2	-	2	-	2	-	ns	13
29	tRCH	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	2	-	2	-	2	-	ns	6,13
30	tRRH	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	-2	-	-2	-	-2	-	ns	6,14
31	tWCH	Write Command Hold Time	17	-	17	-	17	-	ns	13
32	tWCR	Write Command Hold Time from $\overline{\text{RAS}}$	47	-	52	-	57	-	ns	14
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{\text{RAS}}$ Lead Time	25	-	25	-	25	-	ns	15
35	tCWL	Write Command to $\overline{\text{CAS}}$ Lead Time	22	-	22	-	22	-	ns	13
36	tDS	Data-In Set-up Time	-2	-	-2	-	-2	-	ns	7,14
37	tDH	Data-In Hold Time	20	-	20	-	20	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to $\overline{\text{RAS}}$	43	-	53	-	58	-	ns	14
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	18
		SL-part	-	256	-	256	-	256		
40	tWCS	Write Command Set-up Time	2	-	2	-	2	-	ns	8,13

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V72A120A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tcWD	CAS to WE Delay Time	55	-	60	-	60	-	ns	8,15
42	trWD	RAS to WE Delay Time	88	-	98	-	108	-	ns	8,14,15
43	tAWD	Column Address to WE Delay Time	64	-	69	-	74	-	ns	8,14,15
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	15
45	tCHR	CAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	14
46	trPC	RAS to CAS Precharge Time	-2	-	-2	-	-2	-	ns	14
47	tcPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	trOH	RAS Hold Time Referenced to OE	15	-	15	-	15		ns	15
49	toEA	OE Access Time	-	20	-	25	-	25	ns	15
50	toED	OE to Data Delay	20	-	25	-	25	-	ns	15
51	toEZ	Output Buffer Turn Off Delay Time from OE	2	20	2	20	2	20	ns	5,17
52	toEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tcPWD	WE Delay Time from CAS Precharge	63	-	73	-	83	-	ns	8,14,15
54	trHCP	RAS Hold Time from CAS Precharge	42	-	42	-	52	-	ns	13
55	tWRP	WE to RAS Precharge Time (CBR Cycle)		8	-	8	-	8	-	ns
56	tWRH	WE to RAS Hold Time (CBR Cycle)		10	-	10	-	10	-	ns
57	tPD	PDE to Valid Presence Detect Data	-	10	-	10	-	10	ns	11
58	tPDOFF	PDE Inactive to Presence Detects Inactive	2	-	2	-	2	-	ns	12

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM5V72A120A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with VCC during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY51V4400B and HY51V18160B data sheet for detailed information.
4. Measured at VOH= 2.4V and VOL= 0.4V with a load equivalent to 1 TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS \geq twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. tPDOFF(max.) is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent SIMM position.
13. A + 2ns timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
14. A -2ns timing skew from the DRAM to the DIMM resulted from the addition of buffers (DRAM loading may add to skew).
15. A + 5ns (CAS, WE, OE) or + 6ns (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
16. A -2ns min and a -5ns (CAS, WE, OE) or -6ns (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
17. A + 2ns min and a + 5ns (CAS, WE, OE) or + 6ns (address) max timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add to skew).
18. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms after exiting self refresh (for SL-part).

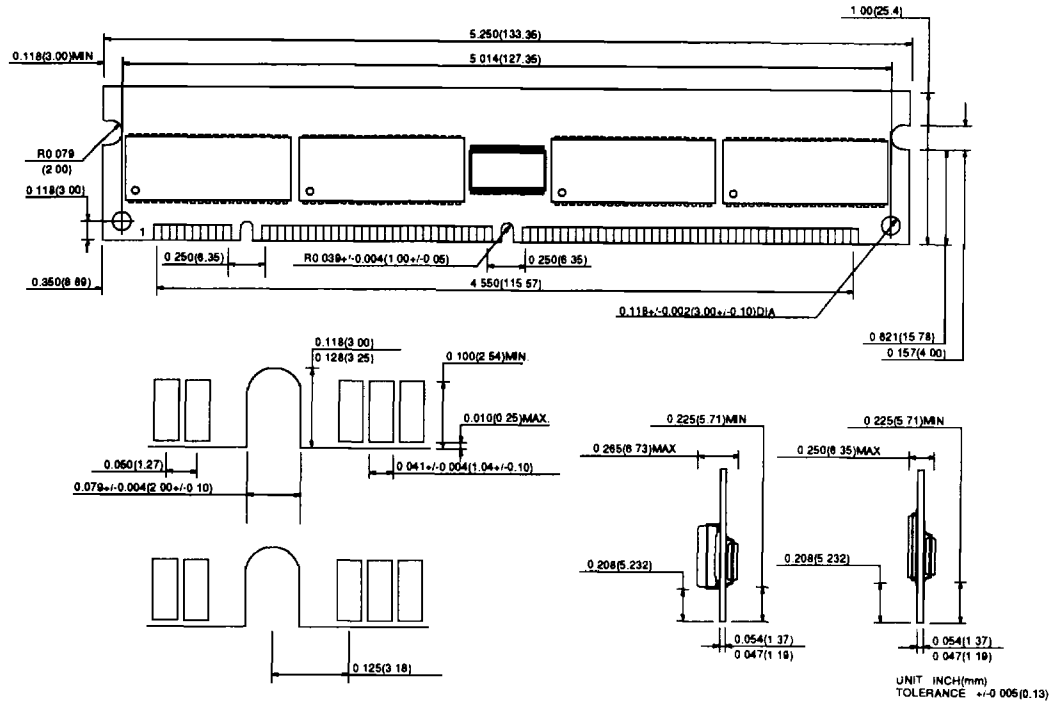
CAPACITANCE

(TA= 25°C, VcC= 3.3V \pm 10%, Vss= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9,B0)	-	20	pF
CIN2	Input Capacitance (RAS0,RAS2)	-	40	pF
CIN3	Input Capacitance (CAS0,CAS4,WE0,WE2,OE0,OE2)	-	20	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ71)	-	15	pF

PACKAGE INFORMATION

168 pin Dual In-line Memory Module (XG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V72A120AXG	60/70/80		DIMM	Gold
HYM5V72A120ASLXG	60/70/80	SL-part	DIMM	Gold
HYM5V72A120ATXG	60/70/80		DIMM	Gold
HYM5V72A120ASLTXG	60/70/80	SL-part	DIMM	Gold