TMC2250A

Matrix Multiplier

12 x 10 bit, 50 MHz

Features

- Four user-selectable filtering and transformation functions:
  - Triple dot product (3 x 3) matrix multiply
  - Cascadeable 9-tap systolic FIR filter
  - Cascadeable 3 x 3-pixel image convolver
  - Cascadeable 4 x 2-pixel image convolver
- 50 MHz (20ns) pipelined throughput
- 12-bit input and output data, 10-bit coefficients
- 6-bit cascade input and output ports in all filter modes
- Onboard coefficient storage, with three-cycle updating of all nine coefficients

Applications

- Image filtering and manipulation
- Video effects generation
- Video standards conversion and encoding/decoding
- Three-dimensional image manipulation
- Medical image processing
- Edge detection for object recognition
- FIR filtering for communications systems

Description

The TMC2250A is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 50 MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

The 3 x 3 matrix multiply or color conversion configuration can perform video standard conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 50 MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250A is fabricated in a sub-micron CMOS process and operates at clock speeds of up to 50 MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in 121-pin plastic pin grid array (PGA) packages as well as a 120-lead plastic quad flatpack (PQFP). All input and output signals are TTL compatible.

Functional Description

The TMC2250A is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) a cascadeable 9-tap FIR filter, a 3 x 3-pixel convolver, or a 4 x 2-pixel convolver all in one monolithic circuit. With a 50MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11) the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. Table 1 details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250A can implement four different digital filter architectures. Upon selection of the desired function by the user ($MODE_{1-0}$), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC and ZC) are configured in all filter modes a 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O function configurations for all four modes are shown in Table 1.

Definitions

The calculations performed by the TMC2250A in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)
Indicates the data word presented to that input port during the specified clock rising edge(x). Applies to all input ports A_{11-0}, B_{11-0}, C_{11-0}, and $CASIN_{15-0}$.

KA1(1), KB3(4)
Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).

X(1), Y(4), Z(6), CASOUT (6)
Indicated data available at that output port t_{DO} after that specified clock rising edge (x). Applies to all output ports X_{11-0}, Y_{11-0}, Z_{11-0}, and $CASOUT_{15-0}$.

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250A. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom". The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in Table 2, the TMC2250A's matched input and output data formats accommodate 0dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Table 1. Data Port Formatting by Mode

	Inputs						Inputs/Output		Outputs		
Mode	**A_{11-0}**	**B_{11-0}**	**C_{11-0}**	**KA_{9-0}**	**KB_{9-0}**	**KC9-0**	**XC_{11-0}**	**YC_{11-8}**	**Y_{7-4}**	**YC3-0**	**ZC_{11-0}**
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC9-0	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC9-0	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC9-0	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC9-0	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

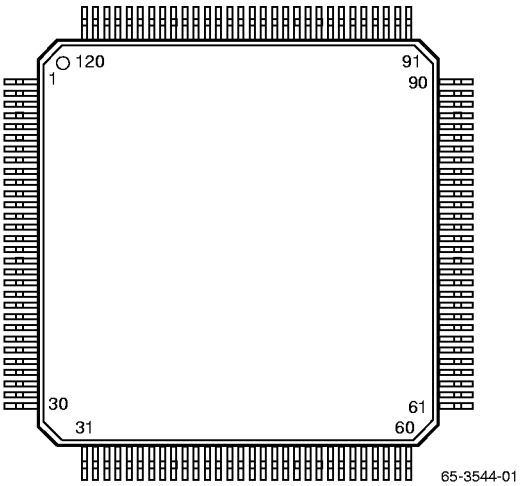
Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-CI_{15}$	CI_{14}	CI_{13}	CI_{12}	CI_{11}	CI_{10}	CI_9	CI_8	CI_7	CI_6	CI_5	CI_4	.	CI_3	CI_2	CI_1	CI_0					
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									
Modes 01, 10, 11 CASOUT	$-CO_{15}$	CO_{14}	CO_{13}	CO_{12}	CO_{11}	CO_{10}	CO_9	CO_8	CO_7	CO_6	CO_5	CO_4	.	CO_3	CO_2	CO_1	CO_0					

Note: A minus sign indicates a two's complement sign bit.

Pin Assignments

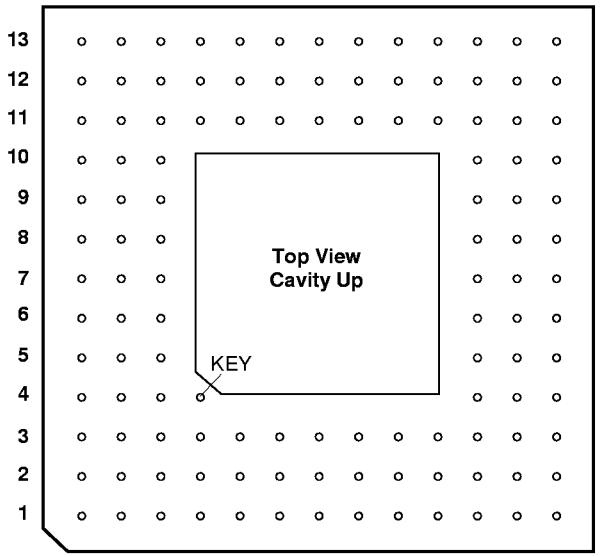
120 Pin Plastic Quad Flat Pack (MQFP), KE Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	XC_6	31	ZC_6	61	KA_1	91	B_5
2	XC_5	32	ZC_7	62	KA_2	92	B_6
3	XC_4	33	ZC_8	63	KA_3	93	B_7
4	XC_3	34	GND	64	KA_4	94	B_8
5	XC_2	35	ZC_9	65	KA_5	95	B_9
6	XC_1	36	ZC_{10}	66	KA_6	96	B_{10}
7	XC_0	37	ZC_{11}	67	KA_7	97	B_{11}
8	GND	38	KC_0	68	KA_8	98	C_0
9	YC_{11}	39	KC_1	69	KA_9	99	C_1
10	YC_{10}	40	KC_2	70	CWE_1	100	C_2
11	YC_9	41	KC_3	71	CWE_0	101	C_3
12	V_{DD}	42	GND	72	GND	102	V_{DD}
13	YC_8	43	KC_4	73	A_0	103	C_4
14	Y_7	44	KC_5	74	A_1	104	C_5
15	Y_6	45	KC_6	75	A_2	105	C_6
16	GND	46	V_{DD}	76	A_3	106	GND
17	Y_5	47	KC_7	77	A_4	107	C_7
18	Y_4	48	KC_8	78	A_5	108	C_8
19	YC_0	49	KC_9	79	A_6	109	C_9
20	V_{DD}	50	KB_0	80	A_7	110	C_{10}
21	YC_1	51	KB_1	81	A_8	111	C_{11}
22	YC_2	52	KB_2	82	A_9	112	$MODE_1$
23	YC_3	53	KB_3	83	A_{10}	113	$MODE_0$
24	GND	54	KB_4	84	A_{11}	114	GND
25	ZC_0	55	KB_5	85	B_0	115	XC_{11}
26	ZC_1	56	KB_6	86	B_1	116	XC_{10}
27	ZC_2	57	KB_7	87	B_2	117	XC_9
28	ZC_3	58	KB_8	88	CLK	118	V_{DD}
29	ZC_4	59	KB_9	89	B_3	119	XC_8
30	ZC_5	60	KA_0	90	B_4	120	XC_7

Pin Assignments (continued)

120 Pin Plastic Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC_7	C5	GND	G11	A_3	L10	KB_8
A2	XC_9	C6	C_{10}	G12	A_2	L11	KA_1
A3	XC_{10}	C7	GND	G13	A_3	L12	KA_5
A4	$MODE_0$	C8	V_{DD}	H1	Y_4	L13	KA_6
A5	C_{11}	C9	C_0	H2	YC_0	M1	ZC_2
A6	C_8	C10	B_8	H3	V_{DD}	M2	ZC_7
A7	C_7	C11	B_5	H11	GND	M3	ZC_9
A8	C_5	C12	B_3	H12	A_0	M4	ZC_{11}
A9	C_3	C13	B_1	H13	A_1	M5	KC_2
A10	C_1	D1	YC_{11}	J1	YC_1	M6	KC_4
A11	B_{10}	D2	XC_0	J2	YC_2	M7	KC_6
A12	B_7	D3	XC_0	J3	GND	M8	KC_9
A13	B_4	D11	CLK	J11	KA_8	M9	KB_2
B1	XC_4	D12	B_0	J12	CWE_1	M10	KB_5
B2	XC_5	D13	A_{10}	J13	CWE_0	M11	KB_9
B3	XC_8	E1	YC_9	K1	YC_3	M12	KA_2
B4	XC_{11}	E2	YC_{10}	K2	ZC_0	M13	KA_3
B5	$MODE_1$	E3	GND	K3	ZC_3	N1	ZC_5
B6	C_9	E11	A_{11}	K11	KA_4	N2	ZC_8
B7	C_6	E12	A_9	K12	KA_7	N3	ZC_{10}
B8	C_4	E13	A_8	K13	KA_9	N4	KC_1
B9	C_2	F1	Y_7	L1	ZC_1	N5	KC_3
B10	B_{11}	F2	YC_8	L2	ZC_4	N6	KC_5
B11	B_9	F3	V_{DD}	L3	ZC_6	N7	KC_7
B12	B_6	F11	A_7	L4	GND	N8	KC_8
B13	B_2	F12	A_6	L5	KC_0	N9	KB_1
C1	XC_1	F13	A_5	L6	GND	N10	KB_3
C2	XC_2	G1	Y_5	L7	V_{DD}	N11	KB_6
C3	XC_6	G2	Y_6	L8	KB_0	N12	KB_7
C4	V_{DD}	G3	GND	L9	KB_4	N13	KA_0

Pin Descriptions

Pin Name	Pin Number PGA	Pin Number MQFP	Function	Pin Description
Power				
V_{DD}	F3, H3, L7, C8, C4	12, 20, 46, 102, 118	Supply Voltage	The TMC2250A operates from a single +5V supply. All pins must be connected.
GND	E3, G3, J3, L4, L6, H11, C7, C5	8, 16, 24, 34, 42, 72, 106, 114	Ground	The TMC2250A operates from a single +5V supply. All pins must be connected.
Clock				
CLK	D11	88	System Clock	The TMC2250A operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.
Controls				
$MODE_{1,0}$	B4, A4	112, 113	Mode Control	The TMC2250A will switch to the configuration selected by the user (as shown in Table 3) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.
$CWE_{1,0}$	J12, J13	70, 71	Coefficient Write Enable	Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See Table 4 and the Functional Block Diagram.
Input/Output				
A_{11-0}	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12	84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73	Data Input A	Data presented to the 12-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (Table 3). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.
B_{11-0}	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12	97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85	Data Input B	
C_{11-0}	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9	111, 110, 109, 108, 107, 105, 104, 103, 101, 100, 99, 98	Data Input C	

Pin Descriptions (continued)

Pin Name	Pin Number PGA	Pin Number MQFP	Function	Pin Description
KA_{9-0}	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13	69, 68, 67, 66, 65, 64, 63, 62, 61, 60	Coefficient Input A1, A2, A3	Data presented to the 10-bit registered coefficient input ports KA, KB and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in Table 4.
KB_{9-0}	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	59, 58, 57, 56, 55, 54, 53, 52, 51, 50	Coefficient Input B1, B2, B3	
KC_{9-0}	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5	49, 48, 47, 45, 44, 43, 41, 40, 39, 38	Coefficient Input B1, B2, B3	
XC_{11-0}	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2	115, 116, 117, 119, 120, 1, 2, 3, 4, 5, 6, 7	$CASIN_{15-4}$/ Output X	In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port $CASIN_{15-0}$. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B and C). In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y AND Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.$CASOUT_{15-0}$ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port $CASOUT_{15-0}$.
YC_{11-8}	D1, E2, E1, F2	9, 10, 11, 13	$CASIN_{3-0}$/ Output Y_{11-0}	
Y_{7-4}	F1, G2, G1, H1	14, 15, 17, 18	$Output_{7-4}$ only	
YC_{3-0}	K1, J2, J1, H2	23, 22, 21, 19	$CASOUT_{3-0}$/ Output Y_{3-0}	
ZC_{11-0}	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	37, 36, 35, 33, 32, 31, 30, 29, 28, 27, 26, 25	$CASOUT_{15-4}$/Output Z_{11-0}	

Notes:

1. The output ports X, Y, Z and CASOUT, and input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.
2. The output drivers on pins XC_{11-0} and YC_{11-8} are not necessarily disabled until after the first rising edge of CLK following power-up. If these pins are to be tied to other output drivers, to each other, or to ground or V_{DD}, the user should ensure that a clock pulse arrives within a few seconds of power-up, to avoid bus contention.

Table 3. Configuration Mode Word

$MODE_{1,0}$	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One Dimensional FIR
10	3 x 3 -Pixel Convolver
11	4 x 2 -Pixel Convolver

Table 4. Coefficient Write Enable Word

$CWE_{1,0}$	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product", in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words half-LSB rounded to 12 bits are then available every clock cycle.

$$X(5)=A(1)KA1(1)+B(1)KB1(1)+C(1)KC1(1)$$
$$Y(5)=A(1)KA2(1)+B(1)KB2(1)+C(1)KC2(1)$$
$$Z(5)=A(1)KA3(1)+B(1)KB3(1)+C(1)KC3(1)$$

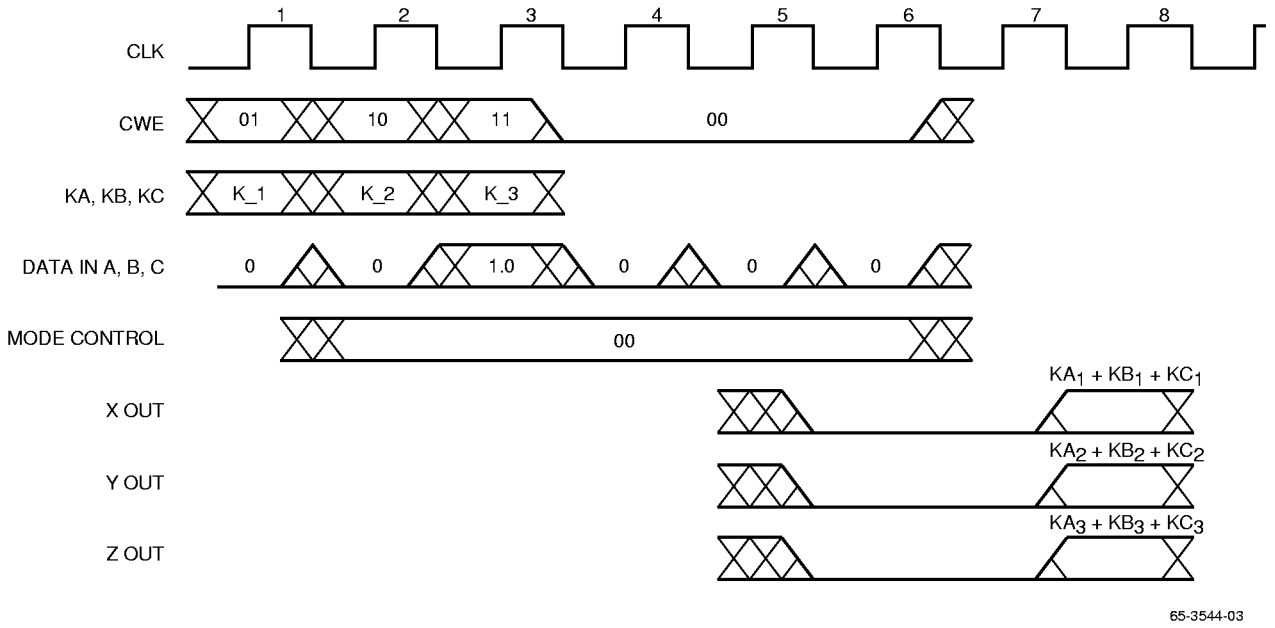


Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

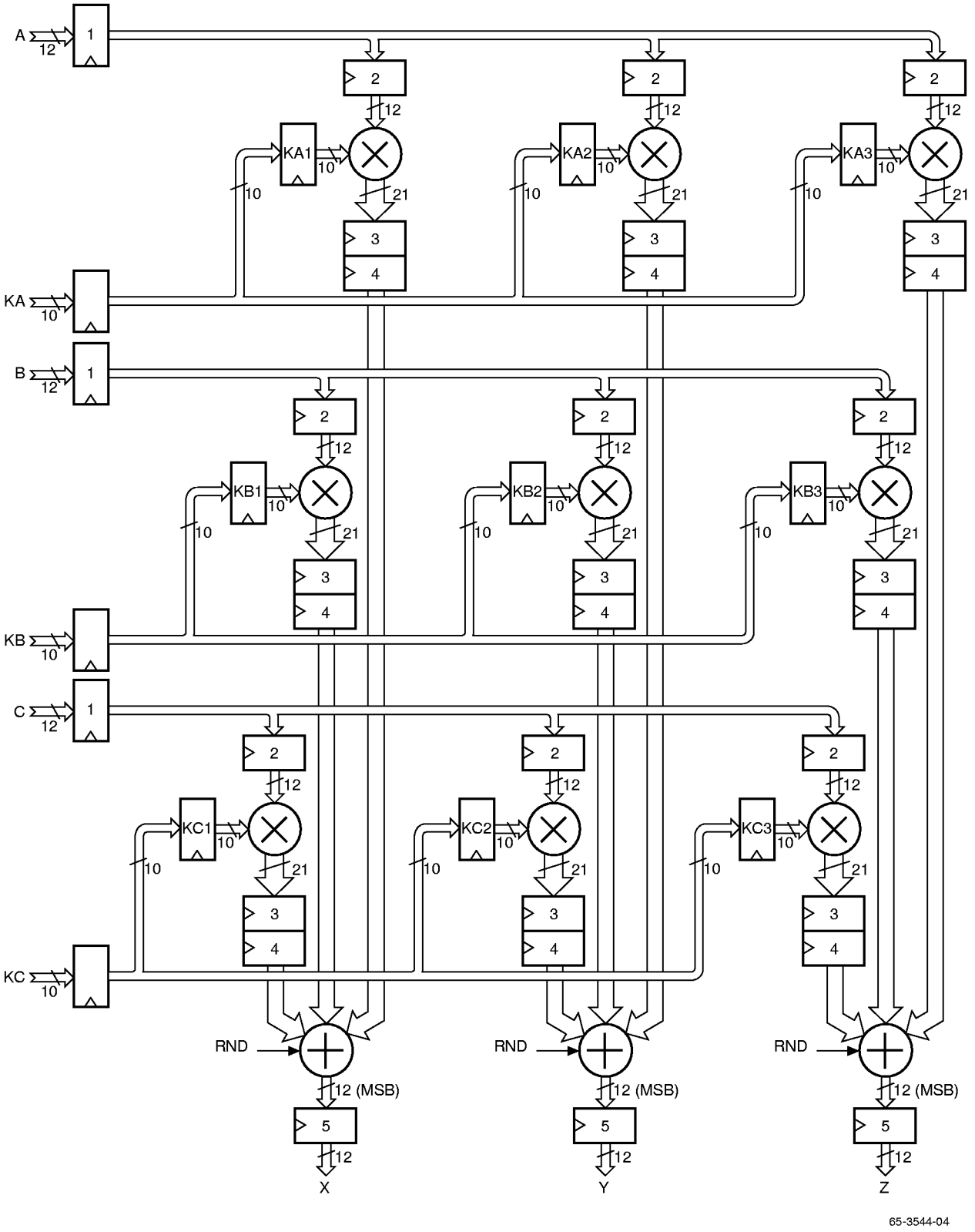


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)

9-Tap FIR Filter Mode (01)

The architecture for this configuration is shown in Figure 4. The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle.

The figure shows that the input data are automatically right-shifted by one position through the row of multiplier input registers on every clock in anticipation of a new input data word.

CASOUT(13) =
A(9)KA3(9)+A(8)KA2(8)+A(7)KA1(7)
+B(6)KB3(9)+B(5)KB2(8)+B(4)KB1(7)
+B(3)KC3(9)+B(2)KC2(8)+B(1)KC1(7)
+CASIN(10)

Latency: Impulse in to center of 9-tap response =9 registers. Cascade In to Cascade Out=4 registers.

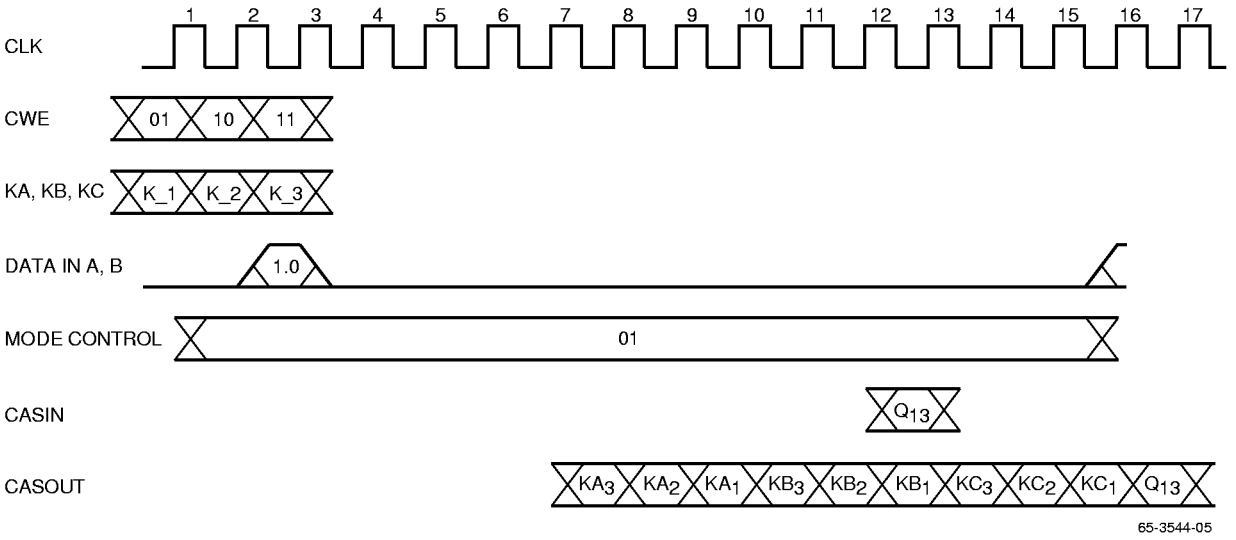


Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

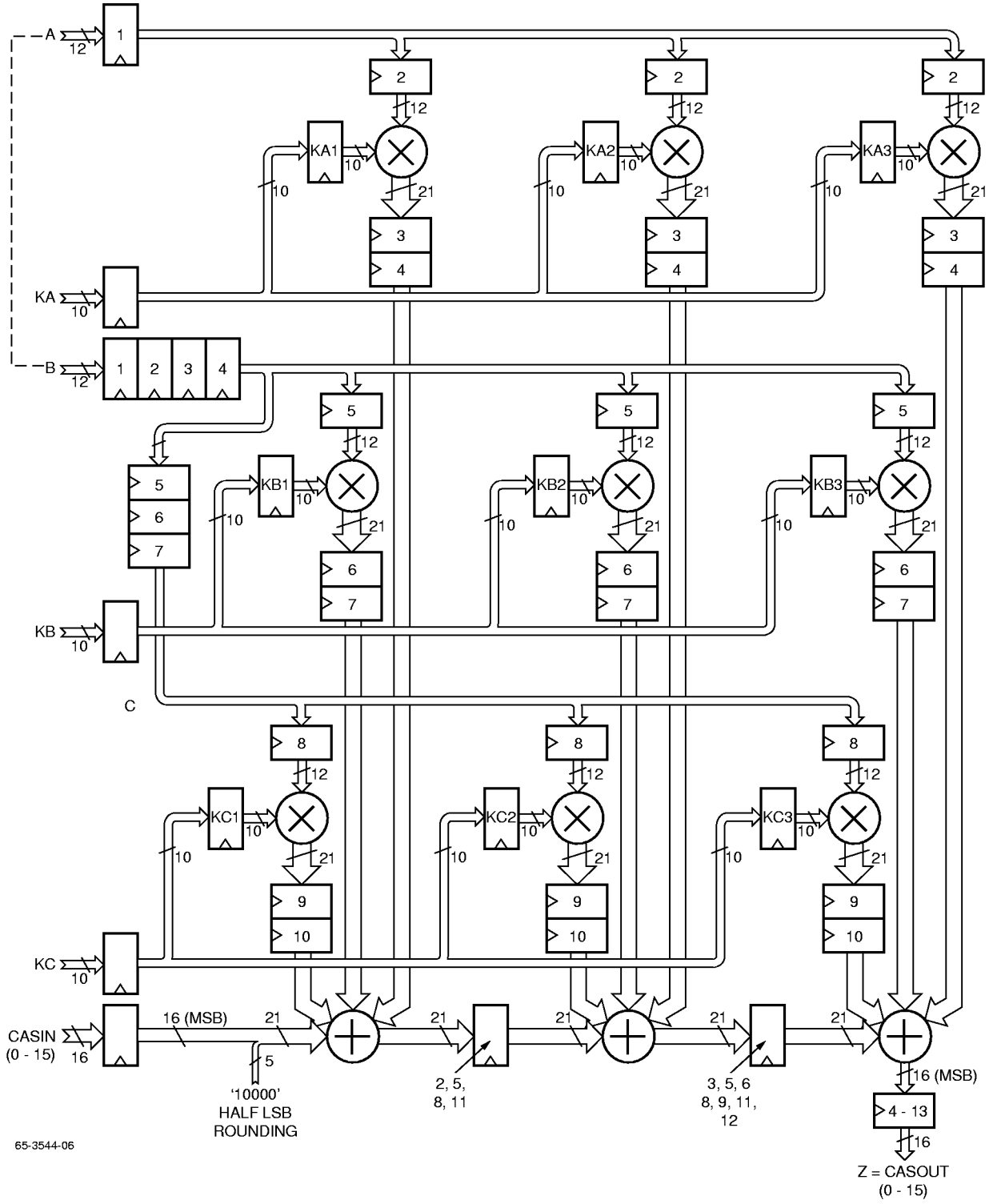


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)

3 x 3 Pixel Convolver (Mode 10)

This filter configuration accepts a 3 pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5 to 7 clocks later, with a new output available on every clock cycle.

The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

CASOUT(7)=
A(3)KA3(3)+A(2)KA2(2)+A(1)KA1(1)
+B(3)KB3(3)+B(2)KB2(2)+B(1)KB1(1)
+C(3)KC3(3)+C(2)KC2(2)+C(1)KC1(1)
+CASIN(4)

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out=4 registers.

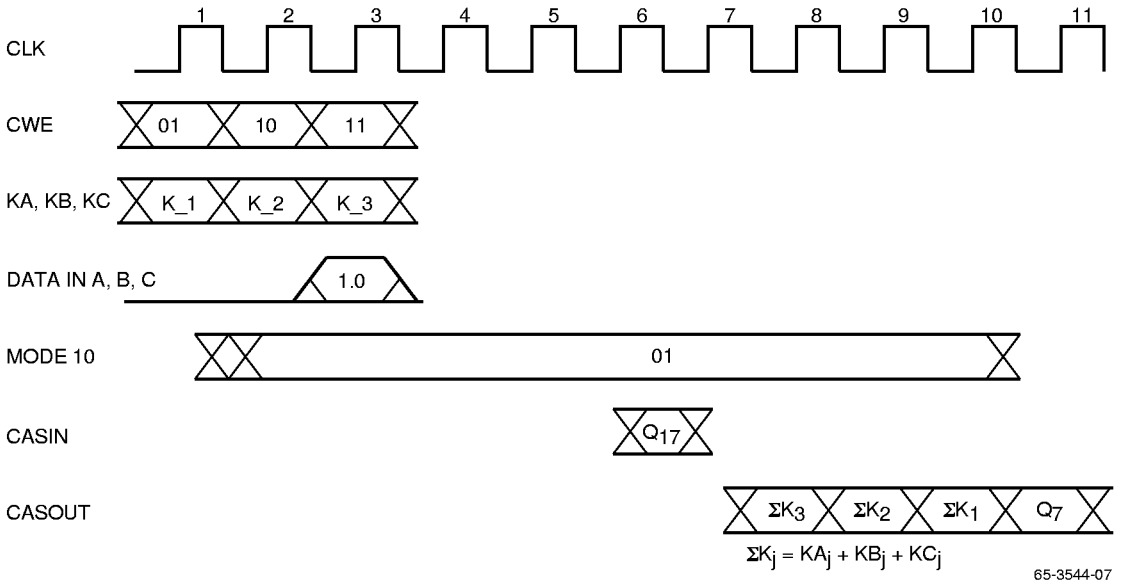


Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

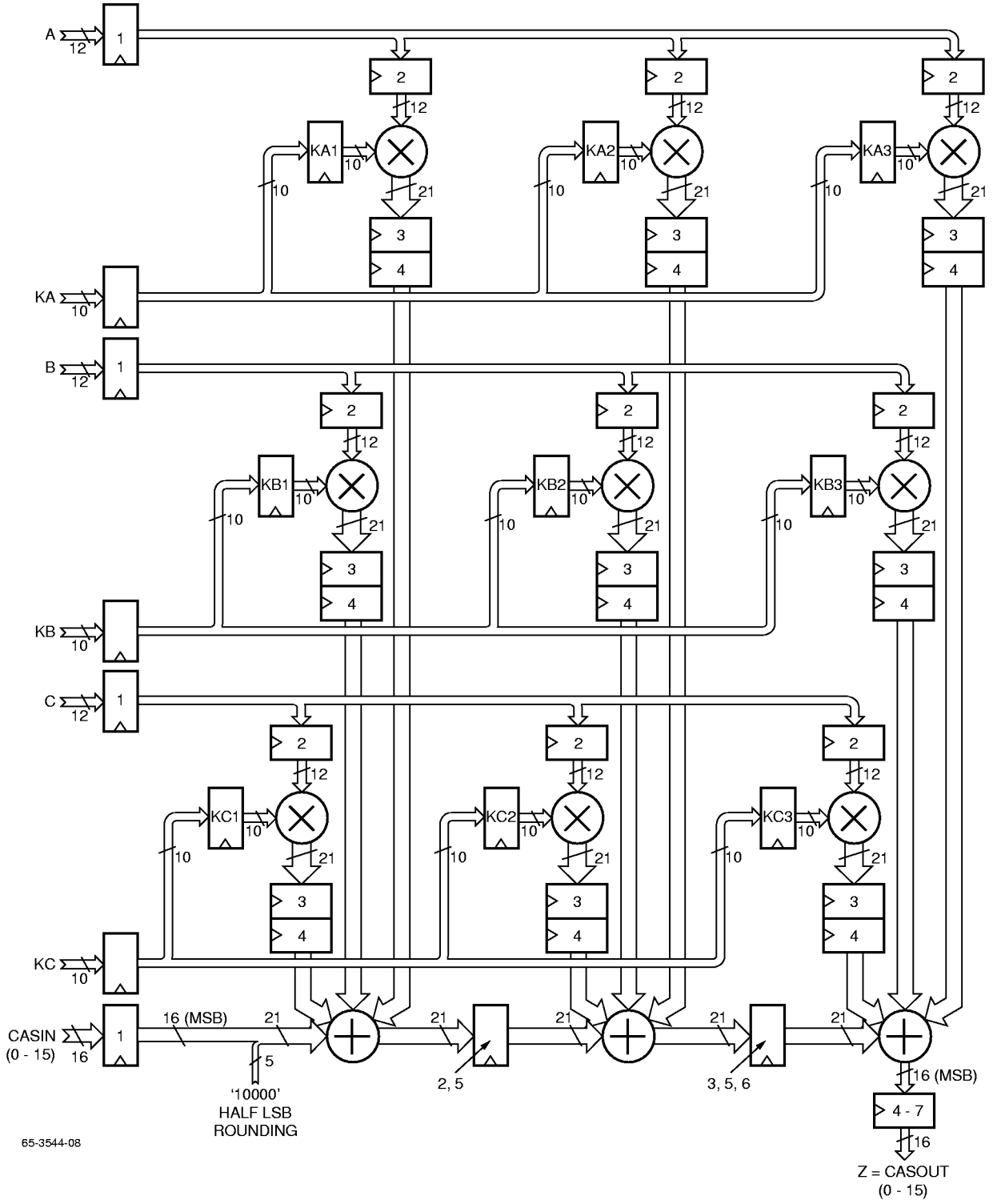


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)

4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2 -Pixel convolver allows the use to perform full-speed cubic convolution with only two TMC2250A devices and the TMC2111A Pipeline Delay Register to synchronize the cascade ports (see the Applications Discussion section).

Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored.

As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

CASOUT(8)=
A(4)KA3(4)+A(3)KA2(3)+A(2)KA1(2)
+A(1)KB3(4)+B(4)KB3(4)+B(3)KB2(3)
+B(2)KB1(2)+B(1)KC1(2)+CASIN(5)

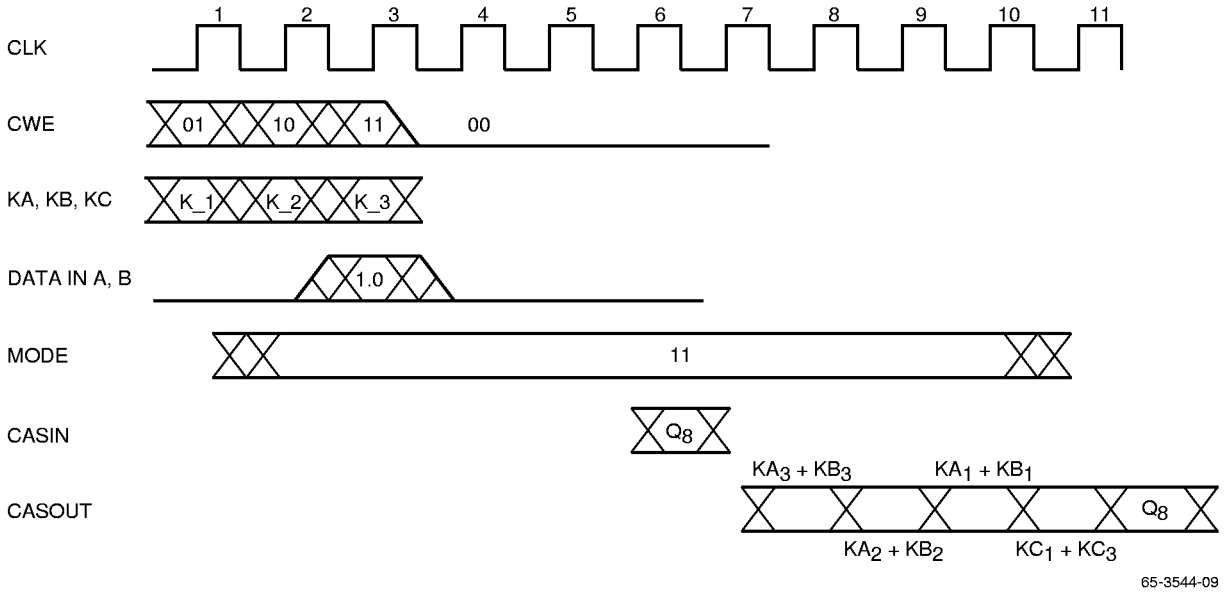


Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

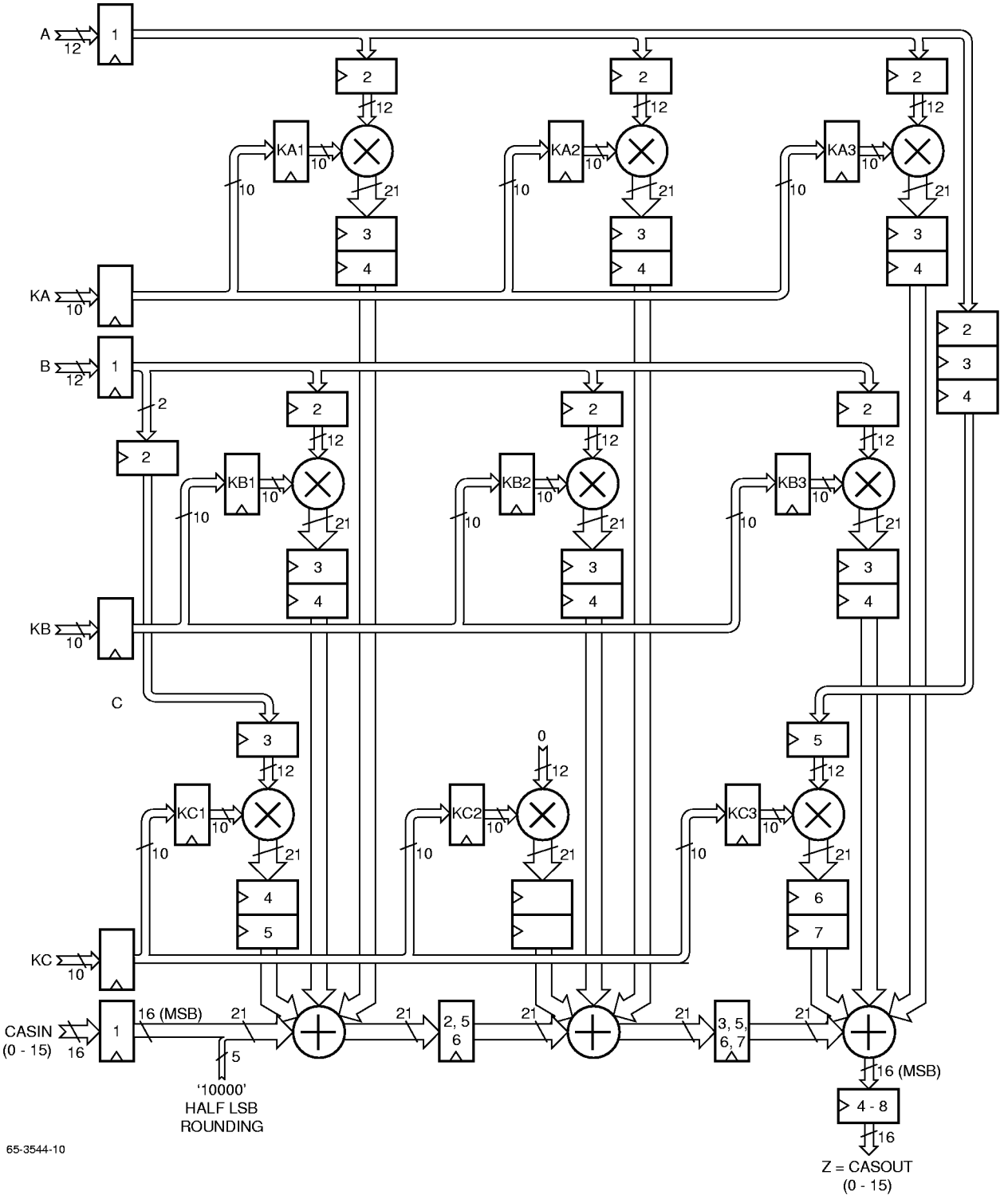


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)

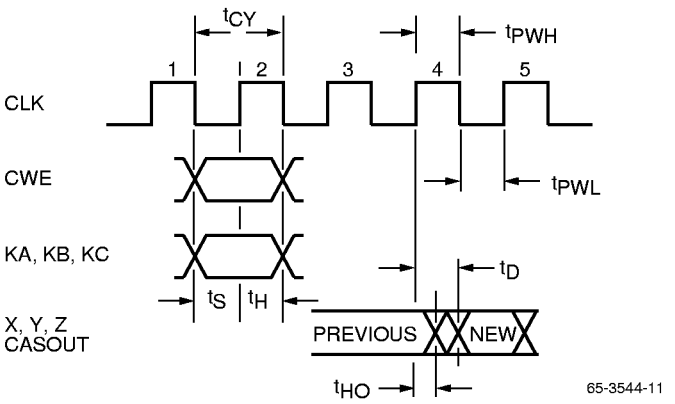
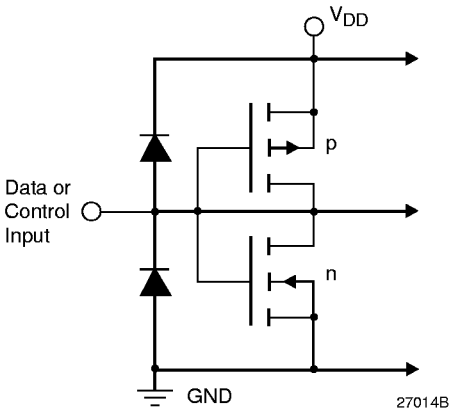


Figure 9. Input/Output Timing Diagram



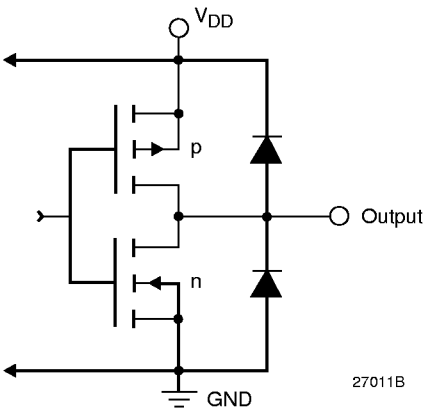


Figure 10. Equivalent Digital Input Circuit Figure 11. Equivalent Digital Output Circuit

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		V_{DD} + 0.5	V
Applied Voltage[2]	-0.5		V_{DD} + 0.5	V
Externally Forced Current[3,4]	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock Frequency	TMC2250A			30	MHz
		TMC2250A-2			40	MHz
		TMC2250A-3			50	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		8			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		2			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2250A			125	mA
		TMC2250A-2			140	mA
		TMC2250A-3			155	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK}=Max				
		TMC2250A			120	mA
		TMC2250A-2			135	mA
		TMC2250A-3			150	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			12	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH[1]	V_{DD} = Max, V_{IN} = V_{DD}			±5	µA
I_{IL}	Input Current, LOW[1]	V_{DD} = Max, V_{IN} = 0 V			±5	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH[2]	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW[2]	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	I_{OH} = Max, V_{DD} = Min	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max, V_{DD} = Min			0.4	V

Notes:

1. Except pins XC_{11-0}, YC_{11-8}.
2. Pins XC_{11-0}, YC_{11-8}.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns

Application Notes

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250A allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. Figure 12 illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution.

This example utilizes the TMC2011A Variable-Length Shift Register to compensate for the internal latency of each TMC2250A. Alternatively, some applications may utilize RAM, FIFO's, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

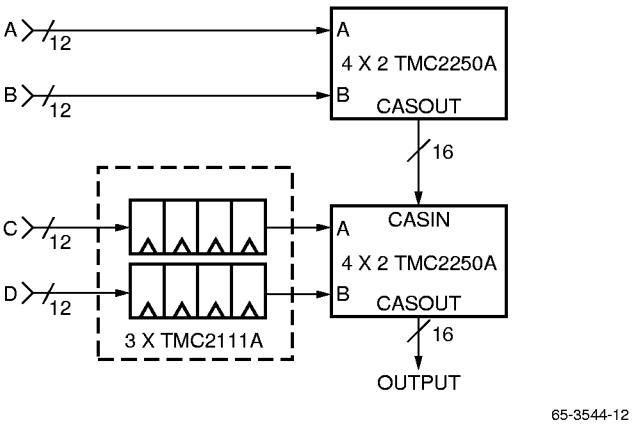


Figure 12. Performing Cubic Convolution with Two TMC2250A's

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302 Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter

Notes:

Notes:

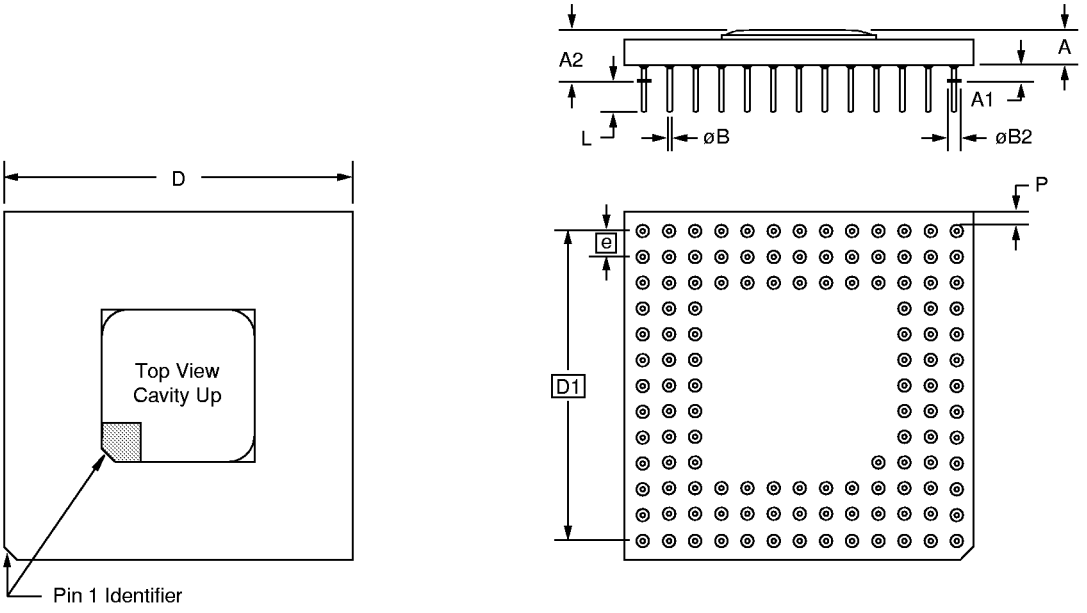
Mechanical Dimensions

121-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



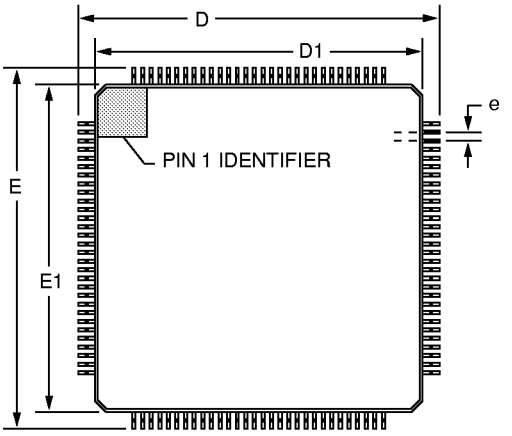
Mechanical Dimensions (continued)

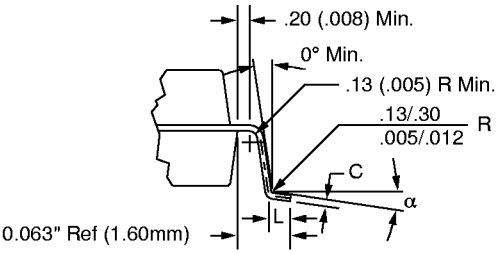
120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

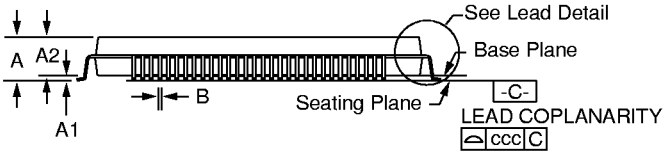
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2250AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C
TMC2250AH5C2	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C2
TMC2250AH5C3	0°C to 70°C	50 MHz	Commercial	120 Pin Plastic Pin Grid Array	2250AH5C3
TMC2250AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC
TMC2250AKEC2	0°C to 70°C	40 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC2
TMC2250AKEC3	0°C to 70°C	50 MHz	Commercial	120 Lead Plastic Quad Flatpack	2250AKEC3