# UCS-4401H AND UCS-4801H
# HERMETIC BiMOS LATCHED DRIVERS
## MIL-STD-883 Compliant

### FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- High-Reliability Screening to MIL-STD-883, Class B

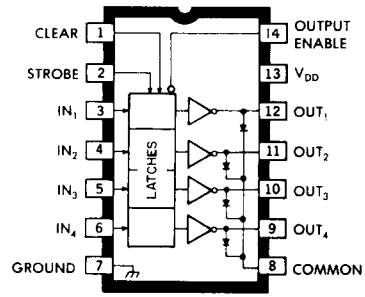
HIGH-VOLTAGE, HIGH-CURRENT interface for military, aerospace and related applications is supplied by these latched drivers. Type UCS-4401H contains four pairs of latches and drivers; Type UCS-4801H has eight pairs of latches and drivers.

The integrated circuits' CMOS inputs work with standard CMOS, PMOS and NMOS logic levels and (with appropriate pull-up resistors) with TTL or DTL circuits. The bipolar open-collector outputs can be used with relays, solenoids, motors, LED or incandescent displays, and other high-power loads.

The output transistors can sink 500 mA and will withstand a $V_{CE}$ of 50 V in the OFF state. Outputs can be paralleled for higher current capability. Because of limitations on package power dissipation, simultaneous operation of all drivers at maximum rated current can only be accomplished with a reduction of duty cycle.

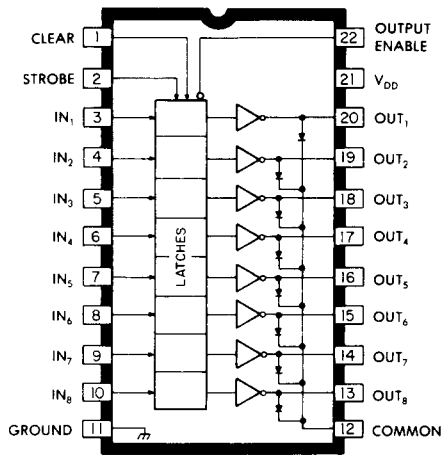
Type UCS-4401H, the four-latch device, is furnished in a standard 14-pin side-brazed hermetic package. Type UCS-4801H, the eight-latch device, is furnished in a 22-pin side-brazed hermetic package with row centers 0.400-inch (10.16 mm) apart.

Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.




Dwg. No. A-10,499B

**UCS-4401H**

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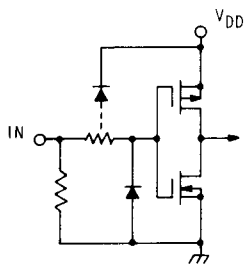
**UCS-4801H**

## ABSOLUTE MAXIMUM RATINGS

Output Voltage, $V_{CE}$ . . . . . 50 V
Supply Voltage, $V_{DD}$ . . . . . 18 V
Input Voltage Range, $V_{IN}$ . . . . . $-0.3$ V to $V_{DD} + 0.3$ V
Continuous Collector Current, $I_C$ . . . . . 500 mA
Package Power Dissipation, $P_D$ . . . . . See Graph
Operating Ambient Temperature Range, $T_A$ . . . . . $-55°C$ to $+125°C$
Storage Temperature Range, $T_S$ . . . . . $-65°C$ to $+150°C$

*CAUTION: Sprague CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.*

### TYPICAL INPUT CIRCUIT

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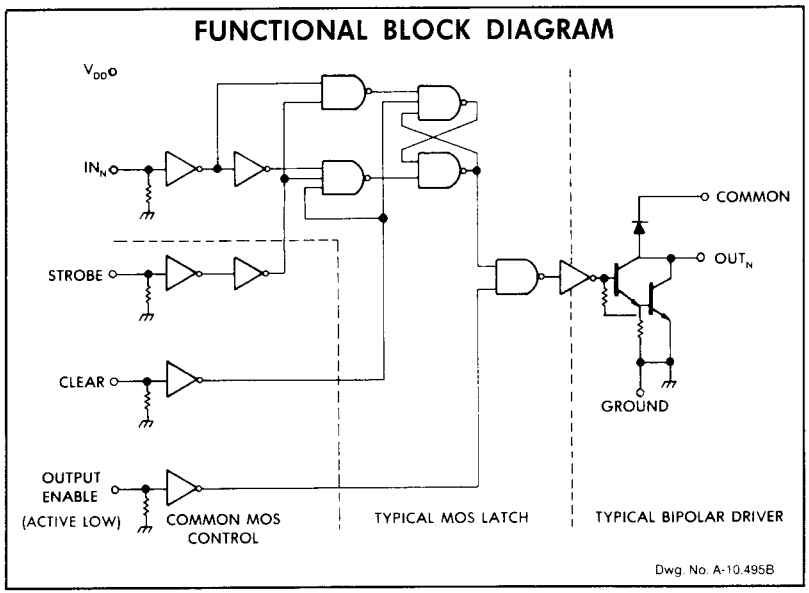
### FUNCTIONAL BLOCK DIAGRAM

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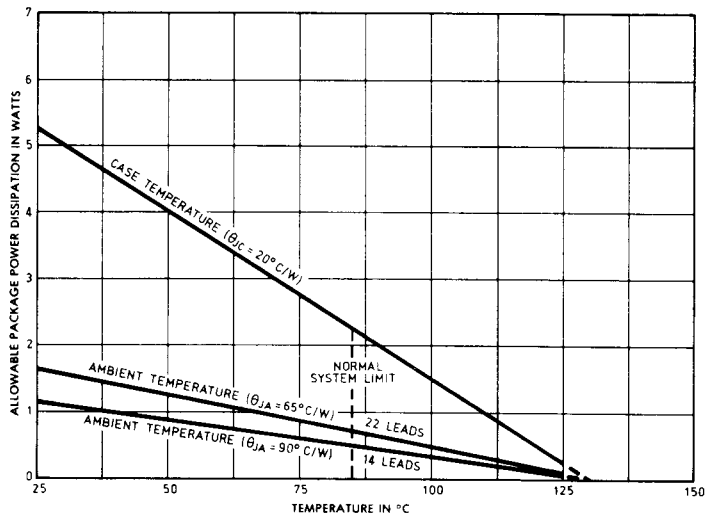
## ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE




Dwg. No. A-11,464

## ELECTRICAL CHARACTERISTICS at $T_A$ = +25°C, $V_{DD}$ = 5 V (unless otherwise specified)

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| Output Leakage Current | $I_{CEX}$ | $V_{CE}$ = 50 V | — | — | 50 | µA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$ = 100 mA | — | 0.9 | 1.1 | V |
| | | $I_C$ = 200 mA | — | 1.1 | 1.3 | V |
| | | $I_C$ = 350 mA, $V_{DD}$ = 7.0 V | — | 1.3 | 1.6 | V |
| Input Voltage | $V_{IN(0)}$ | | — | — | 1.0 | V |
| | $V_{IN(1)}$ | $V_{DD}$ = 15 V | 13.5 | — | — | V |
| | | $V_{DD}$ = 10 V | 8.5 | — | — | V |
| | | $V_{DD}$ = 5.0 V (See note) | 3.5 | — | — | V |
| Input Resistance | $R_{IN}$ | $V_{DD}$ = 15 V | 50 | 200 | — | kΩ |
| | | $V_{DD}$ = 10 V | 50 | 300 | — | kΩ |
| | | $V_{DD}$ = 5.0 V | 50 | 600 | — | kΩ |
| Supply Current | $I_{DD(ON)}$ (Each stage) | $V_{DD}$ = 15 V, Outputs Open | — | 1.0 | 2.0 | mA |
| | | $V_{DD}$ = 10 V, Outputs Open | — | 0.9 | 1.7 | mA |
| | | $V_{DD}$ = 5.0 V, Outputs Open | — | 0.7 | 1.0 | mA |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{IN}$ = 0 V | — | 50 | 100 | µA |
| | | All Drivers OFF, $V_{IN}$ = 0 V, $V_{DD}$ = 15 V | — | — | 200 | µA |
| Clamp Diode Leakage Current | $I_R$ | $V_R$ = 50 V | — | — | 50 | µA |
| Clamp Diode Forward Voltage | $V_F$ | $I_F$ = 350 mA | — | 1.7 | 2.0 | V |

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

## ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| Output Leakage Current | $I_{CEX}$ | $V_{CE} = 50\ V$ | — | — | 50 | μA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 100\ mA$ | — | — | 1.3 | V |
| | | $I_C = 200\ mA$ | — | — | 1.5 | V |
| | | $I_C = 350\ mA$, $V_{DD} = 7.0\ V$ | — | — | 1.8 | V |
| Input Voltage | $V_{IN(0)}$ | | — | — | 1.0 | V |
| | $V_{IN(1)}$ | $V_{DD} = 15\ V$ | 14 | — | — | V |
| | | $V_{DD} = 10\ V$ | 9.0 | — | — | V |
| | | $V_{DD} = 5.0\ V$ (See note) | 3.6 | — | — | V |
| Input Resistance | $R_{IN}$ | $V_{DD} = 15\ V$ | 35 | — | — | kΩ |
| | | $V_{DD} = 10\ V$ | 35 | — | — | kΩ |
| | | $V_{DD} = 5.0\ V$ | 35 | — | — | kΩ |
| Supply Current | $I_{DD(ON)}$ (Each stage) | $V_{DD} = 15\ V$, Outputs Open | — | 1.0 | 2.5 | mA |
| | | $V_{DD} = 10\ V$, Outputs Open | — | 0.9 | 1.9 | mA |
| | | $V_{DD} = 5.0\ V$, Outputs Open | — | 0.7 | 1.2 | mA |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{IN} = 0\ V$ | — | 50 | 100 | μA |
| | | All Drivers OFF, $V_{IN} = 0\ V$, $V_{DD} = 15\ V$ | — | — | 200 | μA |
| Clamp Diode Leakage Current | $I_R$ | $V_R = 50\ V$ | — | — | 50 | μA |
| Clamp Diode Forward Voltage | $V_F$ | $I_F = 350\ mA$ | — | — | 2.1 | V |

## ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

| Characteristic | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Units |
| Output Leakage Current | $I_{CEX}$ | $V_{CE} = 50\ V$ | — | — | 500 | μA |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C = 100\ mA$* | — | — | 1.3 | V |
| | | $I_C = 200\ mA$* | — | — | 1.5 | V |
| | | $I_C = 350\ mA$, $V_{DD} = 7.0\ V$* | — | — | 1.8 | V |
| Input Voltage | $V_{IN(0)}$ | | — | — | 1.0 | V |
| | $V_{IN(1)}$ | $V_{DD} = 15\ V$ | 13.5 | — | — | V |
| | | $V_{DD} = 10\ V$ | 8.5 | — | — | V |
| | | $V_{DD} = 5.0\ V$ (See note) | 3.5 | — | — | V |
| Input Resistance | $R_{IN}$ | $V_{DD} = 15\ V$ | 50 | — | — | kΩ |
| | | $V_{DD} = 10\ V$ | 50 | — | — | kΩ |
| | | $V_{DD} = 5.0\ V$ | 50 | — | — | kΩ |
| Supply Current | $I_{DD(ON)}$ (Each stage) | $V_{DD} = 15\ V$, Outputs Open | — | 1.0 | 2.0 | mA |
| | | $V_{DD} = 10\ V$, Outputs Open | — | 0.9 | 1.7 | mA |
| | | $V_{DD} = 5.0\ V$, Outputs Open | — | 0.7 | 1.0 | mA |
| | $I_{DD(OFF)}$ | All Drivers OFF, $V_{IN} = 0\ V$ | — | 50 | 100 | μA |
| | | All Drivers OFF, $V_{IN} = 0\ V$, $V_{DD} = 15\ V$ | — | — | 200 | μA |
| Clamp Diode Leakage Current | $I_R$ | $V_R = 50\ V$ | — | — | 500 | μA |
| Clamp Diode Forward Voltage | $V_F$ | $I_F = 350\ mA$* | — | — | 2.0 | V |

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1"
*Pulsed test.

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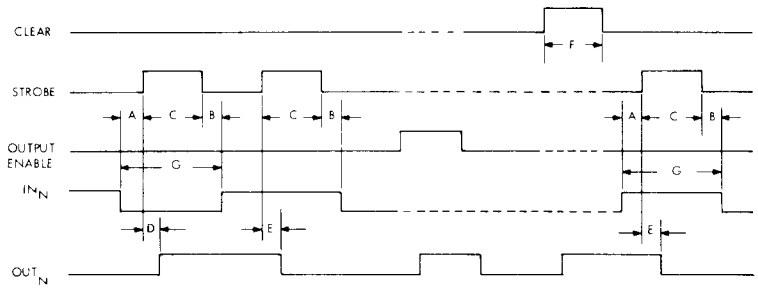
## TIMING CONDITIONS

$T_A$ = +25°C; Logic Levels are $V_{DD}$ and Ground




A. Minimum data active time before strobe enabled (data set-up time) . . . . . 100 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 100 ns
C. Minimum strobe pulse width . . . . . 300 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

### TRUTH TABLE

| $IN_n$ | STROBE | CLEAR | OUTPUT ENABLE | $OUT_n$ t-1 | $OUT_n$ t |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | X | OFF |
| 1 | 1 | 0 | 0 | X | ON |
| X | X | 1 | X | X | OFF |
| X | X | X | 1 | X | OFF |
| X | 0 | 0 | 0 | ON | ON |
| X | 0 | 0 | 0 | OFF | OFF |

X = irrelevant
t-1 = previous output state
t = present output state