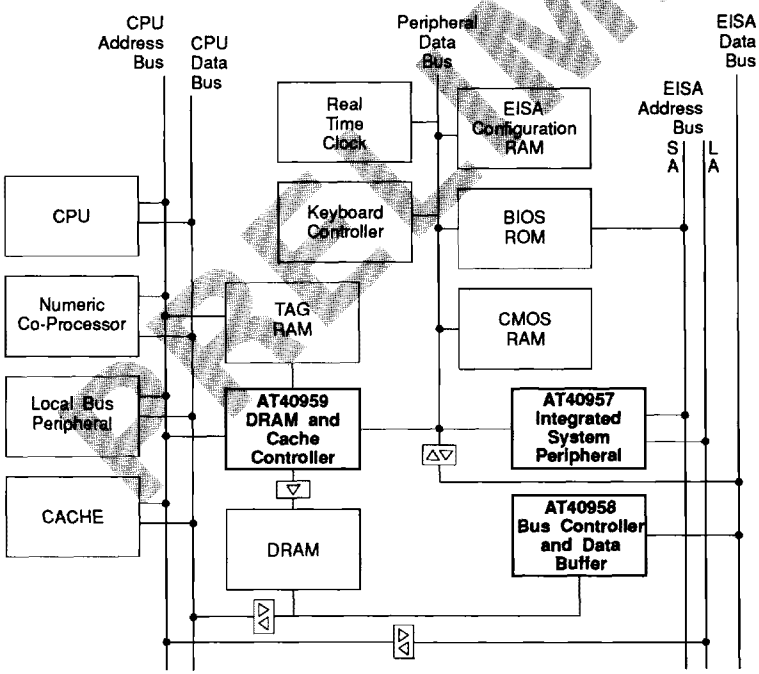
Features

- Three-Chip EISA/ISA Compatible Chip Set for 80386/80486 Systems Operating up to 66 MHz
- One 160-Pin and Two 184-Pin Quad Flatpacks
  - AT40957 Integrated System Peripheral
  - AT40958 Bus Controller and Data Buffer
  - AT40959 DRAM and Cache Controller
- On-Chip Support for Direct-Mapped Write-Back Cache Sizes up to 1 Mbyte
- Asynchronous or Synchronous Cache SRAM
- On-Chip Tag Comparator
- Page Mode Platform Memory Sizes up to 256 Mbytes
- Posted Write Buffer for Write Miss Cycles
- BIOS Shadow and Cache Option
- Staggered Refresh to Reduce Power System Noise
- Hidden Refresh
- Eight ISA DMA Channels
- Six EISA Master Channels
- Fourteen Interrupt Channels
- Local Bus Peripheral Support

EISA/ISA PC/AT Chip Set

Preliminary

Block Diagram



Description

The AT40957/AT40958/AT40959 chip set is an IBM PC/AT EISA/ISA compatible chip set for 80386 and 80486 based systems operating up to 66 MHz. The high integration and on-chip direct-mapped write-back cache controller design allows maximum system performance while requiring a minimum number of components to implement a complete motherboard.

The AT40957 integrated system peripheral incorporates the DMA controller, bus arbitrator, interrupt controller, numeric coprocessor interface, and EISA address latches and buffers. The DMA controller supports Type A, B, and C burst transfers at data rates up to 33 Mbytes/second and byte and word transfers for seven EISA DMA channels. The interrupt controller provides two 8259A-compatible interrupt controllers with 14 independently programmable channels for level- or edge-triggered interrupts. NMI logic includes a fail-safe timer.

The AT40958 bus controller and data buffer interfaces data to the CPU, DMA, master, and slave devices. Byte swaps, bus conversions, and data alignments are all done automatically. The AT40958 also includes parity generation and checking logic, as well as timers for watchdog, refresh, and speaker control.

The AT40959 DRAM and cache controller incorporates system reset logic, cache control, paged mode DRAM control, and BIOS interface logic. The cache controller is direct-mapped write-back with a 16-byte line and a maximum size of 1 Mbyte. An on-chip posted write buffer for write misses is included. The page mode DRAM controller generates and checks memory parity and supports up to eight banks of memory for memory sizes up to 128 Mbytes using 4-Mbit DRAMs, and 256 Mbytes using 16-Mbit DRAMs. The AT40959 also supports two non-cacheable areas in main memory and includes BIOS shadow and cache capabilities.

Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
33	5 V ± 5%	AT40957-33 AT40958-33 AT40959-33	184Q 184Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40957-50 AT40958-50 AT40959-50	184Q 184Q 160Q	Commercial (0°C to 70°C)
66	5 V ± 5%	AT40957-66 AT40958-66 AT40959-66	184Q 184Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)
184Q	185 Lead, Plastic Gull Wing Quad Flat Package (PQFP)