

## 240pin Unbuffered DDR2 SDRAM MODULE

Based on 64Mx8 DDR2 SDRAM

### Features

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 64Mx64 and 128Mx64 DDR2 Unbuffered DIMM based on 64Mx8 DDR2 SDRAM
- Performance:

	PC2-3200	PC2-4200	PC2-5300	
Speed Sort	5A	37B	3C	Unit
DIMM $\overline{\text{CAS}}$ Latency	3	4	5	
f CK Clock Frequency	200	266	333	MHz
t CK Clock Cycle	5	3.7	3	ns
f DQ DQ Burst Frequency	400	533	667	MHz

- Intended for 200 MHz, 266MHz, and 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8\text{Volt} \pm 0.1$
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble

- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - Device  $\overline{\text{CAS}}$  Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/bank) – M1U51264TU88A0F
- 14/10/2 Addressing (row/column/bank) – M1U1G64TU8HA0F
- 7.8  $\mu\text{s}$  Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 84-ball FBGA Package

### Description

M1U51264TU88A0F, M1U51264TU88A0B, M1Y51264TU88A0B, M1U1G64TU8HA0F, M1U1G64TU8HA0B, M1Y1G64TU8HA0B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one-rank 64Mx64 and two ranks 128Mx64 high-speed memory array. Modules use eight 64Mx8 (M1U51264TU88A0F) and sixteen 64Mx8 (M1U1G64TU8HA0F) DDR2 SDRAMs in FBGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 200 MHz (266MHz and 333MHz) clock speeds and achieves high-speed data transfer rates of up to 400 MHz (533MHz and 667MHz). Prior to any access operation, the device  $\overline{\text{CAS}}$  latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)  
M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Ordering Information**

Part Number	Speed			Organization	Leads	Power	Note
M1U51264TU88A0F-5A	200MHz (5ns @ CL = 3)	DDR2-400	PC2-3200	64Mx64	Gold	1.8V	84-ball
M1U51264TU88A0B-5A							60-ball
M1Y51264TU88A0B-5A							Green
M1U51264TU88A0F-37B	266MHz (3.7ns @ CL = 4)	DDR2-533	PC2-4200				84-ball
M1U51264TU88A0B-37B							60-ball
M1Y51264TU88A0B-37B							Green
M1U51264TU88A0F-3C	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300				84-ball
M1U51264TU88A0B-3C							60-ball
M1Y51264TU88A0B-3C							Green
M1U1G64TU8HA0F-5A	200MHz (5ns @ CL = 3)	DDR2-400	PC2-3200	128Mx64	Gold	1.8V	84-ball
M1U1G64TU8HA0B-5A							60-ball
M1Y1G64TU8HA0B-5A							Green
M1U1G64TU8HA0F-37B	266MHz (3.7ns @ CL = 4)	DDR2-533	PC2-4200				84-ball
M1U1G64TU8HA0B-37B							60-ball
M1Y1G64TU8HA0B-37B							Green
M1U1G64TU8HA0F-3C	333MHz (3.7ns @ CL = 5)	DDR2-667	PC2-5300				84-ball
M1U1G64TU8HA0B-3C							60-ball
M1Y1G64TU8HA0B-3C							Green

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Pin Description**

CK0, $\overline{\text{CK0}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	CB0-CB7	ECC Check Bit Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	DQS0-DQS8	Bidirectional data strobes
$\overline{\text{CAS}}$	Column Address Strobe	DM0-DM8/DQS9-17	Input Data Mask/High Data Strobes
$\overline{\text{WE}}$	Write Enable	$\overline{\text{DQS0-DQS17}}$	Differential data strobes
$\overline{\text{CS0}}, \overline{\text{CS1}}$	Chip Selects	V <sub>DD</sub>	Power (1.8V)
A0-A9, A11-A13	Address Inputs	V <sub>REF</sub>	Ref. Voltage for SSTL_18 inputs
A10/AP	Column Address Input/Auto-precharge	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
BA0, BA1	SDRAM Bank Address Inputs	V <sub>SS</sub>	Ground
$\overline{\text{RESET}}$	Reset pin	SCL	Serial Presence Detect Clock Input
ODT0, ODT1	Active termination control lines	SDA	Serial Presence Detect Data input/output
NC	No Connect	SA0-2	Serial Presence Detect Address Inputs

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64



Unbuffered DDR2 SDRAM DIMM

**Pinout**

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>REF</sub>	42	NC	82	V <sub>SS</sub>	123	DQ5	164	NC	204	V <sub>SS</sub>
2	V <sub>SS</sub>	43	NC	83	$\overline{\text{DQS4}}$	124	V <sub>SS</sub>	165	NC	205	DQ38
3	DQ0	44	V <sub>SS</sub>	84	DQS4	125	DM0, DQS9	166	V <sub>SS</sub>	206	DQ39
4	DQ1	45	NC	85	V <sub>SS</sub>	126	$\overline{\text{DQS9}}$	167	NC	207	V <sub>SS</sub>
5	V <sub>SS</sub>	46	NC	86	DQ34	127	V <sub>SS</sub>	168	NC	208	DQ44
6	$\overline{\text{DQS0}}$	47	V <sub>SS</sub>	87	DQ35	128	DQ6	169	V <sub>SS</sub>	209	DQ45
7	DQS0	48	NC	88	V <sub>SS</sub>	129	DQ7	170	V <sub>DDQ</sub>	210	V <sub>SS</sub>
8	V <sub>SS</sub>	49	NC	89	DQ40	130	V <sub>SS</sub>	171	CKE1	211	DM5
9	DQ2	50	V <sub>SS</sub>	90	DQ41	131	DQ12	172	V <sub>DD</sub>	212	NC
10	DQ3	51	V <sub>DDQ</sub>	91	V <sub>SS</sub>	132	DQ13	173	NC	213	V <sub>SS</sub>
11	V <sub>SS</sub>	52	CKE0	92	$\overline{\text{DQS5}}$	133	V <sub>SS</sub>	174	NC	214	DQ46
12	DQ8	53	V <sub>DD</sub>	93	DQS5	134	DM1, DQS10	175	V <sub>DDQ</sub>	215	DQ47
13	DQ9	54	NC	94	V <sub>SS</sub>	135	$\overline{\text{DQS10}}$	176	A12	216	V <sub>SS</sub>
14	V <sub>SS</sub>	55	NC	95	DQ42	136	V <sub>SS</sub>	177	A9	217	DQ52
15	$\overline{\text{DQS1}}$	56	V <sub>DDQ</sub>	96	DQ43	137	CK1	178	V <sub>DD</sub>	218	DQ53
16	DQS1	57	A11	97	V <sub>SS</sub>	138	$\overline{\text{CK1}}$	179	A8	219	V <sub>SS</sub>
17	V <sub>SS</sub>	58	A7	98	DQ48	139	V <sub>SS</sub>	180	A6	220	CK2
18	NC	59	V <sub>DD</sub>	99	DQ49	140	DQ14	181	V <sub>DDQ</sub>	221	$\overline{\text{CK2}}$
19	NC	60	A5	100	V <sub>SS</sub>	141	DQ15	182	A3	222	V <sub>SS</sub>
20	V <sub>SS</sub>	61	A4	101	SA2	142	V <sub>SS</sub>	183	A1	223	DM6
21	DQ10	62	V <sub>DDQ</sub>	102	NC	143	DQ20	184	V <sub>DD</sub>	224	NC
22	DQ11	63	A2	103	V <sub>SS</sub>	144	DQ21	KEY		225	V <sub>SS</sub>
23	V <sub>SS</sub>	64	V <sub>DD</sub>	104	$\overline{\text{DQS6}}$	145	V <sub>SS</sub>	185	CK0	226	DQ54
24	DQ16	KEY		105	DQS6	146	DM2	186	$\overline{\text{CK0}}$	227	DQ55
25	DQ17	65	V <sub>SS</sub>	106	V <sub>SS</sub>	147	NC	187	V <sub>DD</sub>	228	V <sub>SS</sub>
26	V <sub>SS</sub>	66	V <sub>SS</sub>	107	DQ50	148	V <sub>SS</sub>	188	A0	229	DQ60
27	$\overline{\text{DQS2}}$	67	V <sub>DD</sub>	108	DQ51	149	DQ22	189	V <sub>DD</sub>	230	DQ61
28	DQS2	68	NC	109	V <sub>SS</sub>	150	DQ23	190	BA1	231	V <sub>SS</sub>
29	V <sub>SS</sub>	69	V <sub>DD</sub>	110	DQ56	151	V <sub>SS</sub>	191	V <sub>DDQ</sub>	232	DM7
30	DQ18	70	A10/AP	111	DQ57	152	DQ28	192	$\overline{\text{RAS}}$	233	NC
31	DQ19	71	BA0	112	V <sub>SS</sub>	153	DQ29	193	$\overline{\text{CS0}}$	234	V <sub>SS</sub>
32	V <sub>SS</sub>	72	V <sub>DDQ</sub>	113	$\overline{\text{DQS7}}$	154	V <sub>SS</sub>	194	V <sub>DDQ</sub>	235	DQ62
33	DQ24	73	$\overline{\text{WE}}$	114	DQS7	155	DM3	195	ODT0	236	DQ63
34	DQ25	74	$\overline{\text{CAS}}$	115	V <sub>SS</sub>	156	NC	196	A13	237	V <sub>SS</sub>
35	V <sub>SS</sub>	75	V <sub>DDQ</sub>	116	DQ58	157	V <sub>SS</sub>	197	V <sub>DD</sub>	238	V <sub>DDSPD</sub>
36	$\overline{\text{DQS3}}$	76	$\overline{\text{CS1}}$	117	DQ59	158	DQ30	198	V <sub>SS</sub>	239	SA0
37	DQS3	77	ODT1	118	V <sub>SS</sub>	159	DQ31	199	DQ36	240	SA1
38	V <sub>SS</sub>	78	V <sub>DDQ</sub>	119	SDA	160	V <sub>SS</sub>	200	DQ37		
39	DQ26	79	V <sub>SS</sub>	120	SCL	161	NC	201	V <sub>SS</sub>		
40	DQ27	80	DQ32	121	V <sub>SS</sub>	162	NC	202	DM4		
41	V <sub>SS</sub>	81	DQ33	122	DQ4	163	V <sub>SS</sub>	203	NC		

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**



512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

**Input/Output Functional Description**

Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$ , $\overline{CK1}$ , $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$ , $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ define the operation to be executed by the SDRAM.
V <sub>REF</sub>	Supply		Reference voltage for SSTL-18 inputs
V <sub>DDQ</sub>	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63 CB0 – CB7	(SSTL)	Active High	Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations.
V <sub>DD</sub> , V <sub>SS</sub>	Supply		Power and ground for the DDR SDRAM input buffers and core logic
$\overline{DQS0} - \overline{DQS8}$ $\overline{DQS0} - \overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V <sub>DD</sub> or V <sub>SS</sub> on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V <sub>DD</sub> to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V <sub>DD</sub> to act as a pull-up.
V <sub>DDSPD</sub>	Supply		Serial EEPROM positive power supply.

# M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green) M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)

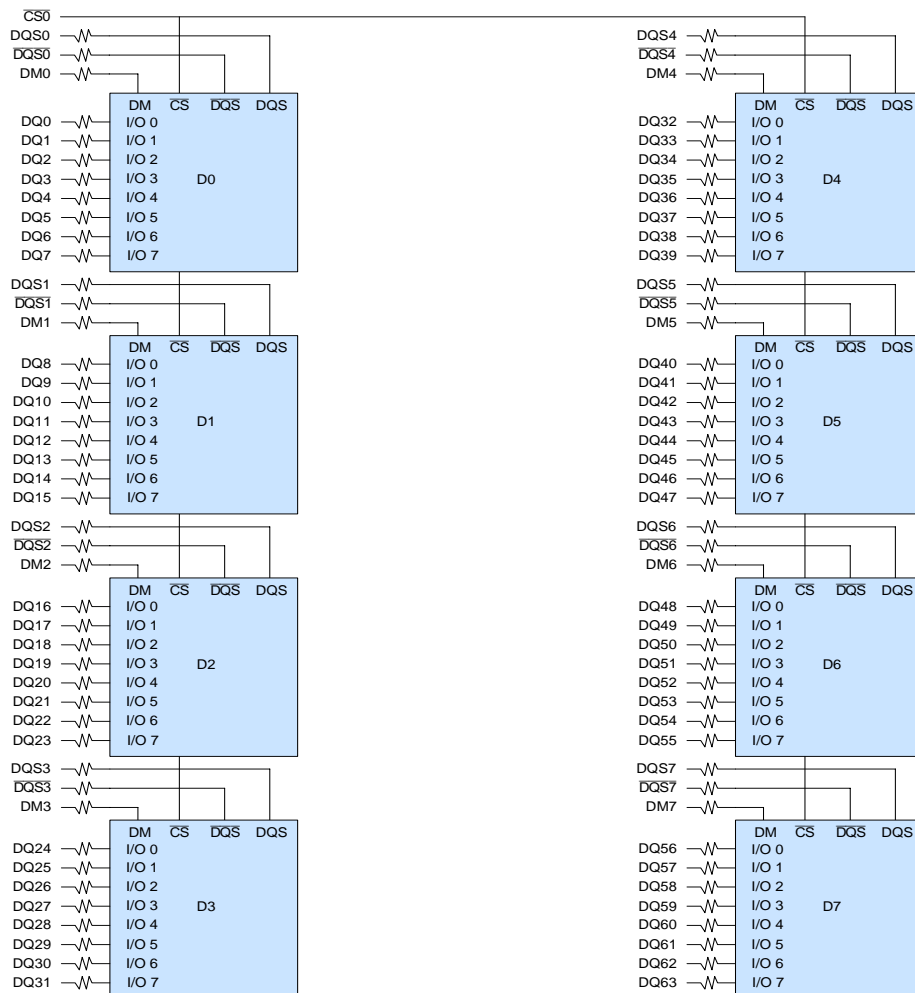


512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

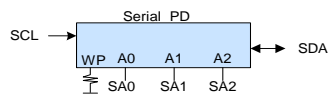
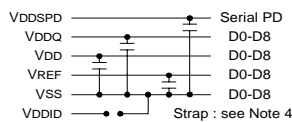
## Functional Block Diagram

(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)



BA0-BA1 — BA0-BA1 : SDRAMs D0-D8  
A0-A13 — A0-A13 : SDRAMs D0-D8  
RAS — RAS : SDRAMs D0-D8  
CAS — CAS : SDRAMs D0-D8  
WE — WE : SDRAMs D0-D8  
CKE0 — CKE : SDRAMs D0-D8  
ODT0 — ODT : SDRAMs D0-D8

- Notes :
1. DQ-to-I/O wiring may be changed within a byte.
  2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
  3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
  4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
  5. Address and control resistors are 22 Ohms +/- 5%



# M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green) M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)

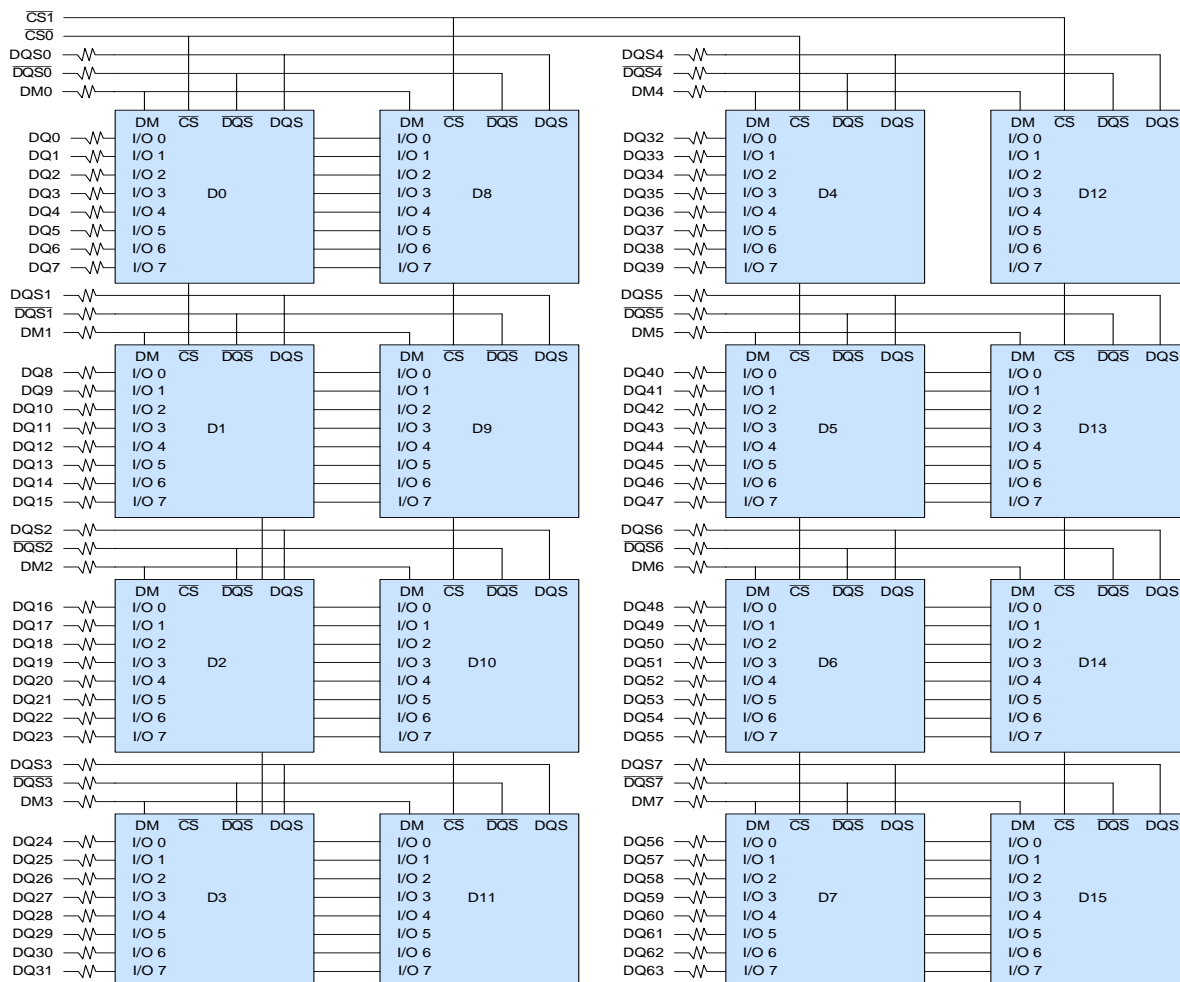


512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

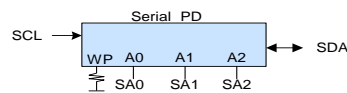
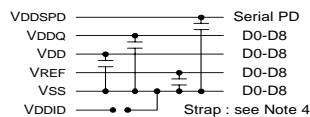
## Functional Block Diagram

(1GB, 2 Rank, 64Mx8 DDR2 SDRAMs)



BA0-BA1 — BA0-BA1 : SDRAMs D0-D17  
A0-A13 — A0-A13 : SDRAMs D0-D17  
RAS — RAS : SDRAMs D0-D17  
CAS — CAS : SDRAMs D0-D17  
WE — WE : SDRAMs D0-D17  
CKE0 — CKE : SDRAMs D0-D8  
CKE1 — CKE : SDRAMs D9-D17  
ODT0 — ODT : SDRAMs D0-D8  
ODT1 — ODT : SDRAMs D9-D17

- Notes :
1. DQ-to-I/O wiring may be changed within a byte.
  2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
  3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
  4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
  5. Address and control resistors are 22 Ohms +/- 5%



**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Serial Presence Detect – Part 1 of 2 (512MB)**

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank, Package, and Height	1 rank, Height=30mm			60			
6	Data Width of this Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at Maximum Support CAS Latency CL=5	5ns	3.7ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time (t <sub>ac</sub> ) from Clock at CL=5	0.6ns	0.5ns	0.45ns	60	50	45	
11	DIMM Configuration Type	Non – ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDRII SDRAM Width	X8			08			
14	Error Checking DDRII SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3/4/5			38			
19	Reserved	Undefined			00			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01	01	13	
23	Minimum Clock Cycle at CL=4	5ns	3.75ns	3.75ns	50	3D	3D	
24	Maximum Data Access Time (t <sub>ac</sub> ) from Clock at CL=4	0.6ns	0.5ns	0.5ns	60	50	50	
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time (t <sub>ac</sub> ) from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t <sub>RP</sub> )	15ns			3C			
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	7.5ns			1E			
29	Minimum RAS to CAS delay (t <sub>RCD</sub> )	15ns			3C			
30	Minimum Active to Precharge Time (t <sub>RAS</sub> )	45ns			2D			
31	Module Bank Density	512MB			80			
32	Address and Command Input Setup Time Before Clock (t <sub>IS</sub> )	0.35ns	0.25ns	0.2ns	35	25	20	
33	Address and Command Input Hold Time After Clock (t <sub>IH</sub> )	0.475ns	0.375ns	0.2ns	47	37	32	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	0.15ns	0.1ns	0.05ns	15	10	05	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t <sub>WR</sub> )	15ns			3C			
37	Internal Write to Read Command delay (t <sub>WTR</sub> )	10ns	7.5ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge Command delay (t <sub> RTP</sub> )	7.5ns			1E			
39	Memory Analysis Probe Characteristics	Undefined			00			

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)  
M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Serial Presence Detect – Part 2 of 2 (512MB)**

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
40	Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$	The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns			00			
41	Minimum Core Cycle Time ( $t_{RC}$ )	60ns			3C			
42	Min. Auto Refresh Command Cycle Time ( $t_{RFC}$ )	105ns			69			
43	Maximum Clock Cycle Time ( $t_{CK max}$ )	8ns			80			
44	Max. DQS-DQ Skew Factor ( $t_{QHS}$ )	0.35ns	0.3ns	0.25ns	23	1E	19	
45	Read Data Hold Skew Factor ( $t_{QHS}$ )	0.45ns	0.4ns	0.35ns	2D	28	23	
46	PLL Relock Time	N/A			00			
47 – xx	IDD in SPD	Undefined			00			
xx -61	Reserved	Undefined			00			
62	SPD Revision	1.0			10			
63	Checksum Data	Checksum Data			34	B0	80	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-92	Module Part Number	Module Part Number in ASCII			--			
93-255	Reserved	Undefined			--			



## Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank, Package, and Height	2 rank, Height=30mm			61			
6	Data Width of this Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at Maximum Support CAS Latency CL=5	5ns	3.75ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time (t <sub>ac</sub> ) from Clock at CL=5	0.6ns	0.5ns	0.45ns	60	50	45	
11	DIMM Configuration Type	Non - ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDRII SDRAM Width	X8			08			
14	Error Checking DDRII SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3/4/5			38			
19	Reserved	Undefined			00			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01	01	13	
23	Minimum Clock Cycle at CL=4	5ns	3.7ns	3.75ns	50	3D	3D	
24	Maximum Data Access Time (t <sub>ac</sub> ) from Clock at CL=4	0.6ns	0.5ns	0.5ns	60	50	50	
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time (t <sub>ac</sub> ) from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t <sub>RP</sub> )	15ns			3C			
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	7.5ns			1E			
29	Minimum RAS to CAS delay (t <sub>RCD</sub> )	15ns			3C			
30	Minimum Active to Precharge Time (t <sub>RAS</sub> )	45ns			2D			
31	Module Bank Density	512MB			80			
32	Address and Command Input Setup Time Before Clock (t <sub>IS</sub> )	0.35ns	0.25ns	0.2ns	35	25	20	
33	Address and Command Input Hold Time After Clock (t <sub>IH</sub> )	0.475ns	0.375ns	0.325ns	47	37	32	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	0.15ns	0.1ns	0.05ns	15	10	05	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t <sub>WR</sub> )	15ns			3C			
37	Internal Write to Read Command delay (t <sub>WTR</sub> )	10ns	7.5ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge Command delay (t <sub>TRP</sub> )	7.5ns			1E			

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Serial Presence Detect -- Part 2 of 2 (1GB)**

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	DDR2 -400 (-5A)	DDR2 -533 (-37B)	DDR2 -667 (-3C)	
39	Memory Analysis Probe Characteristics	Undefined			00			
40	Extension of Byte 41 t <sub>RC</sub> and Byte 42 t <sub>RFC</sub>	The number below a decimal point of t <sub>RC</sub> and t <sub>RFC</sub> are 0, t <sub>RFC</sub> is less than 256ns			00			
41	Minimum Core Cycle Time (t <sub>RC</sub> )	60ns			3C			
42	Min. Auto Refresh Command Cycle Time (t <sub>RFC</sub> )	105ns			69			
43	Maximum Clock Cycle Time (t <sub>CK max</sub> )	8ns			80			
44	Max. DQS-DQ Skew Factor (t <sub>DQs</sub> )	0.35ns	0.3ns	0.25ns	23	1E	19	
45	Read Data Hold Skew Factor (t <sub>QHS</sub> )	0.45ns	0.4ns	0.35ns	2D	28	23	
46	PLL Relock Time	N/A			00			
47 - xx	IDD in SPD	Undefined			00			
xx -61	Reserved	Undefined			00			
62	SPD Revision	1.0			10			
63	Checksum Data	Checksum data			35	B1	81	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-92	Module Part Number	Module Part Number in ASCII			--			
93-255	Reserved	Undefined			--			

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{IN}, V_{OUT}$	Voltage on I/O pins relative to Vss	-0.5 to VDDQ+0.5	V
$V_{IN}$	Voltage on Input relative to Vss	-0.5 to +2.3	V
$V_{DD}$	Voltage on VDD supply relative to Vss	-0.5 to +2.3	V
$V_{DDQ}$	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V
$T_A$	Operating Temperature (Ambient)	0 to +70	°C
$T_{STG}$	Storage Temperature (Plastic)	-55 to +100	°C

**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics and Operating Conditions

(TA = 0 °C ~ 70 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V <sub>DD</sub>	Supply Voltage	1.7	1.9	V	1
V <sub>DDQ</sub>	I/O Supply Voltage	1.7	1.9	V	1
V <sub>SS</sub> , V <sub>SSQ</sub>	Supply Voltage, I/O Supply Voltage	0	0	V	
V <sub>REF</sub>	I/O Reference Voltage	0.49 x V <sub>DDQ</sub>	0.51 x V <sub>DDQ</sub>	V	1, 2
V <sub>IH</sub> (DC)	Input High (Logic1) Voltage	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V	1
V <sub>IL</sub> (DC)	Input Low (Logic0) Voltage	-0.3	V <sub>REF</sub> - 0.125	V	1

**Note:**

- Inputs are not recognized as valid until V<sub>REF</sub> stabilizes.
- V<sub>REF</sub> is expected to be equal to 0.5 V<sub>DDQ</sub> of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed 2% of the DC value

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**Operating, Standby, and Refresh Currents**

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$  (512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (-5A)	PC2-4200 (-37B)	PC2-5300 (-3C)	Unit	Notes
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	450	520	TBD	mA	1, 2
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $CL=2.5$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$ ; address and control inputs changing once per clock cycle	480	600	TBD	mA	1, 2
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$	30	30	TBD	mA	1, 2
I <sub>DD2N</sub>	Idle Standby Current: $CS \geq V_{IH}(\text{MIN})$ ; all banks idle; $CKE \geq V_{IH}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; address and control inputs changing once per clock cycle	260	320	TBD	mA	1, 2
I <sub>DD3P</sub>	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$	100	130	TBD	mA	1, 2
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH}(\text{MIN})$ ; $CKE \geq V_{IH}(\text{MIN})$ ; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	280	320	TBD	mA	1, 2
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 2.5$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$	565	720	TBD	mA	1, 2
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL=2.5$ ; $t_{CK} = t_{CK}(\text{MIN})$	600	760	TBD	mA	1, 2
I <sub>DD5</sub>	Auto-Refresh Current: $t_{RC} = t_{RFC}(\text{MIN})$	965	1050	TBD	mA	1, 2
I <sub>DD6</sub>	Self-Refresh Current: $CKE \leq 0.2\text{V}$	32	32	TBD	mA	1, 2
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with $BL = 4$ , address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC}(\text{min})$ ; $I_{OUT} = 0\text{mA}$ .	1050	1110	TBD	mA	1, 2

**Note:**

- $V_{DDQ}=1.8\text{V} \pm 0.1\text{V}$ ,  $V_{DD}=1.8\text{V} \pm 0.1\text{V}$
- I<sub>DD</sub> specifications are tested after the device is properly initialized and ODT disabled.

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**  
**512MB: 64M x 64 / 1GB: 128M x 64**



**Unbuffered DDR2 SDRAM DIMM**

**Operating, Standby, and Refresh Currents**

$T_A = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$  (1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (-5A)	PC2-4200 (-37B)	PC2-5300 (-3C)	Unit	Notes
I <sub>DD0</sub>	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	475	550	TBD	mA	1, 2
I <sub>DD1</sub>	Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; CL=2.5; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$ ; address and control inputs changing once per clock cycle	520	630	TBD	mA	1, 2
I <sub>DD2P</sub>	Precharge Power-Down Standby Current: all banks idle; power-down mode; $\text{CKE} \leq V_{IL}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$	60	60	TBD	mA	1, 2
I <sub>DD2N</sub>	Idle Standby Current: $\text{CS} \geq V_{IH}(\text{MIN})$ ; all banks idle; $\text{CKE} \geq V_{IH}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; address and control inputs changing once per clock cycle	520	640	TBD	mA	1, 2
I <sub>DD3P</sub>	Active Power-Down Standby Current: one bank active; power-down mode; $\text{CKE} \leq V_{IL}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$	200	260	TBD	mA	1, 2
I <sub>DD3N</sub>	Active Standby Current: one bank; active/precharge; $\text{CS} \geq V_{IH}(\text{MIN})$ ; $\text{CKE} \geq V_{IH}(\text{MIN})$ ; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	560	650	TBD	mA	1, 2
I <sub>DD4R</sub>	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$	600	750	TBD	mA	1, 2
I <sub>DD4W</sub>	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; $t_{CK} = t_{CK}(\text{MIN})$	680	800	TBD	mA	1, 2
I <sub>DD5</sub>	Auto-Refresh Current: $t_{RC} = t_{RFC}(\text{MIN})$	1000	1060	TBD	mA	1, 2
I <sub>DD6</sub>	Self-Refresh Current: $\text{CKE} \leq 0.2\text{V}$	65	65	TBD	mA	1, 2
I <sub>DD7</sub>	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC}(\text{min})$ ; $I_{OUT} = 0\text{mA}$ .	1060	1160	TBD	mA	1, 2

**Note:**

- $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$ ,  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$
- I<sub>DD</sub> specifications are tested after the device is properly initialized and ODT disabled

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)  
M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



**AC Timing Specifications for DDR2 SDRAM Devices Used on Module**

(TA = 0 °C ~ 70 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-5A		-37B		-3C		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>AC</sub>	DQ output access time from CK/ $\overline{\text{CK}}$	-0.6	+0.6	-0.5	+0.5	-0.45	+0.45	ns	
t <sub>DQSCK</sub>	DQS output access time from CK/ $\overline{\text{CK}}$	-0.5	+0.5	-0.45	+0.45	-0.4	+0.4	ns	
t <sub>CH</sub>	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
t <sub>CL</sub>	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	
t <sub>HP</sub>	Minimum half clk period for any given cycle; defined by clk high (t <sub>CH</sub> ) or clk low (t <sub>CL</sub> ) time	t <sub>CH</sub> or t <sub>CL</sub>		t <sub>CH</sub> or t <sub>CL</sub>		t <sub>CH</sub> or t <sub>CL</sub>		t <sub>CK</sub>	
t <sub>CK</sub>	Clock cycle time	CL=3	5	8	3.75	8	3	8	ns
t <sub>CK</sub>		CL=4, 5	5	8	3.75	8	3	8	ns
t <sub>DH</sub>	DQ and DM input hold time	0.275		0.225		0.175		ns	
t <sub>DS</sub>	DQ and DM input setup time	0.15		0.1		0.1		ns	
t <sub>IPW</sub>	Input pulse width	0.6		0.6		0.6		ns	
t <sub>DIPW</sub>	DQ and DM input pulse width (each input)	0.35		0.35		0.35		ns	
t <sub>HZ</sub>	Data-out high-impedance time from CK/ $\overline{\text{CK}}$		t <sub>AC</sub> (max)		t <sub>AC</sub> (max)	t <sub>AC</sub>		ns	
t <sub>LZ</sub>	Data-out low-impedance time from CK/ $\overline{\text{CK}}$	2t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	2t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	t <sub>AC</sub>		ns	
t <sub>DQSQ</sub>	DQS-DQ skew (DQS & associated DQ signals)		0.35		0.3		0.24	ns	
t <sub>QHS</sub>	Data hold Skew Factor		0.45		0.4		0.34	ns	
t <sub>QH</sub>	Data output hold time from DQS	t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>CK</sub>	
t <sub>DQSS</sub>	Write command to 1st DQS latching transition	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	t <sub>CK</sub>	
t <sub>DQSL(H)</sub>	DQS input low (high) pulse width (write cycle)	0.35		0.35		0.35		t <sub>CK</sub>	
t <sub>DSS</sub>	DQS falling edge to CK setup time (write cycle)	0.2		0.2		0.2		t <sub>CK</sub>	
t <sub>DSH</sub>	DQS falling edge hold time from CK (write cycle)	0.2		0.2		0.2		t <sub>CK</sub>	
t <sub>MRD</sub>	Mode register set command cycle time	2		2		2		t <sub>CK</sub>	
t <sub>WPST</sub>	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
t <sub>WPRE</sub>	Write preamble	0.35		0.35		0.35		t <sub>CK</sub>	
t <sub>IH</sub>	Address and control input hold time	0.475		0.375		0.275		ns	
t <sub>IS</sub>	Address and control input setup time	0.35		0.25		0.2		ns	
t <sub>RPRE</sub>	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>	
t <sub>RPST</sub>	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
t <sub>RAS</sub>	Active to Precharge command	45	120,000	40	120,000	45	120,000	ns	
t <sub>R RD</sub>	Active bank A to Active bank B command	7.5		7.5		7.5		ns	
t <sub>CCD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$	2		2		2		t <sub>CK</sub>	

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**



512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

**AC Timing Specifications for DDR2 SDRAM Devices Used on Module**

(TA = 0 °C ~ 70 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-5A		-37B		-3C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WR</sub>	Write recovery time	15		15		15		ns
t <sub>DAL</sub>	Auto precharge write recovery + precharge time	t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		t <sub>CK</sub>
t <sub>WTR</sub>	Internal write to read command delay	10		7.5		7.5		t <sub>CK</sub>
t <sub>RTP</sub>	Internal read to precharge command delay	7.5		7.5		7.5		ns
t <sub>XSNR</sub>	Exit self refresh to a Non-read command	t <sub>RFC</sub> +10		t <sub>RFC</sub> +10		t <sub>RFC</sub> +10		ns
t <sub>XSRD</sub>	Exit self refresh to a Read command	200		200		200		t <sub>CK</sub>
t <sub>XP</sub>	Exit precharge power down to any Non- read command	2		2		2		t <sub>CK</sub>
t <sub>XARD</sub>	Exit active power down to read command	2		2		2		t <sub>CK</sub>
t <sub>XARDS</sub>	Exit active power down to read command	6-AL		6-AL		7-AL		t <sub>CK</sub>
t <sub>CKE</sub>	CKE minimum pulse width	3		3		3		t <sub>CK</sub>
t <sub>AOND</sub>	ODT turn-on delay	2		2		2		t <sub>CK</sub>
t <sub>AON</sub>	ODT turn-on	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +0.7	t <sub>CK</sub>
t <sub>AONPD</sub>	ODT turn-on (Power down mode)	t <sub>AC</sub> (min) +2	2t <sub>CK</sub> + t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min) +2	2t <sub>CK</sub> + t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min) +2	2t <sub>CK</sub> + t <sub>AC</sub> (max) +1	t <sub>CK</sub>
t <sub>AOFD</sub>	ODT turn-off delay	2.5		2.5		2.5		t <sub>CK</sub>
t <sub>AOFF</sub>	ODT turn-off	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +0.6	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +0.6	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) +0.6	ns
t <sub>AOFFPD</sub>	ODT turn-off (Power down mode)	t <sub>AC</sub> (min)+2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min)+2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) +1	t <sub>AC</sub> (min)+2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) +1	ns
t <sub>ANPD</sub>	ODT to power down entry latency	3		3		3		t <sub>CK</sub>
t <sub>AXPD</sub>	ODT power down exit latency	8		8		8		t <sub>CK</sub>
t <sub>OIT</sub>	OCD drive mode output delay	0	12	0	12	0	12	ns
t <sub>Delay</sub>	Minimum time clocks remains ON after CKE asynchronously drops Low	t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		ns
t <sub>RCD</sub>	Active to Read or Write delay	15		15		12		ns
t <sub>RP</sub>	Precharge command period	15		15		12		ns
t <sub>REFI</sub>	Average Periodic Refresh Interval		7.8		7.8		7.8	us

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

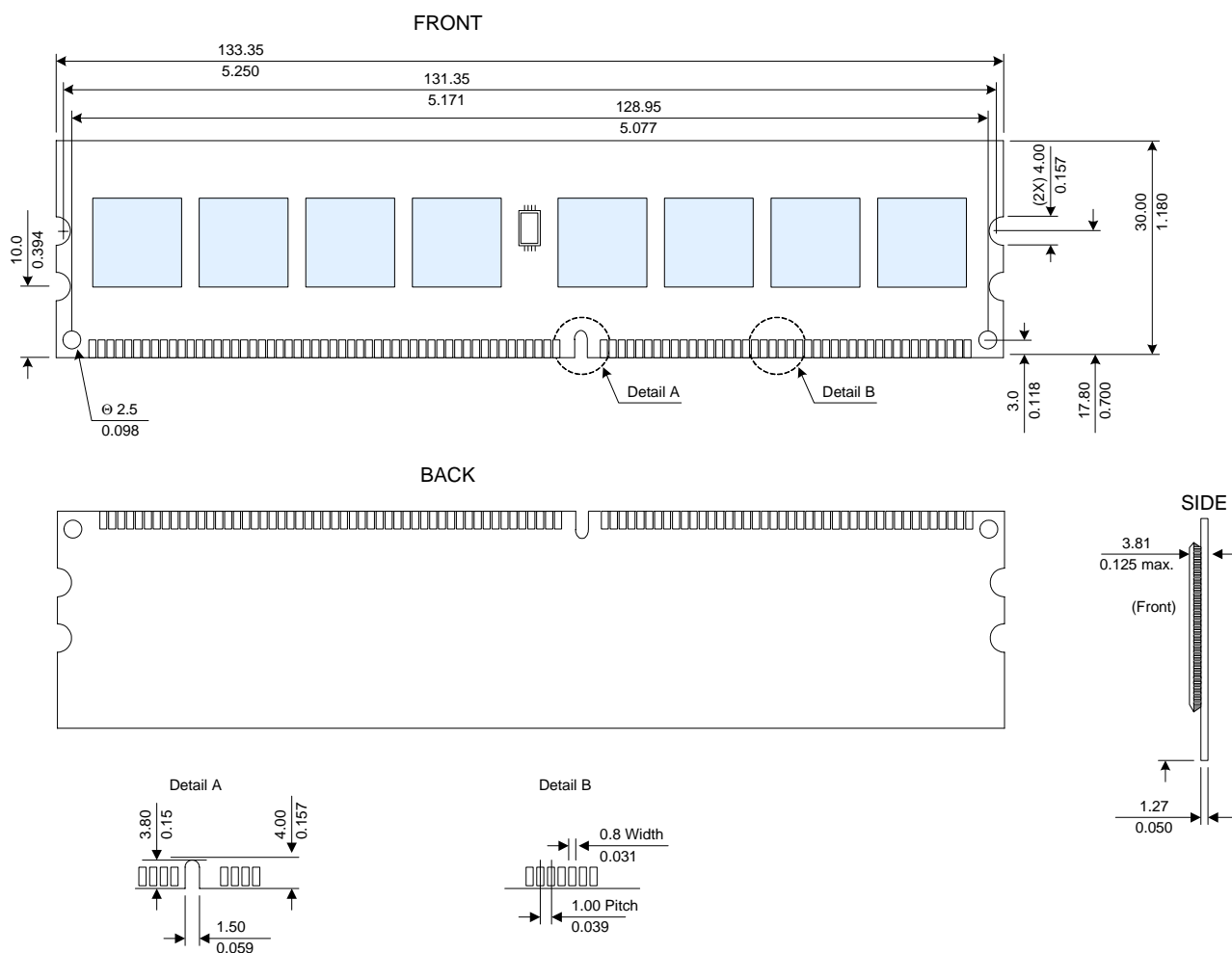


512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

**Package Dimensions**

(512MB, 1 Rank, 64Mx8 DDR SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

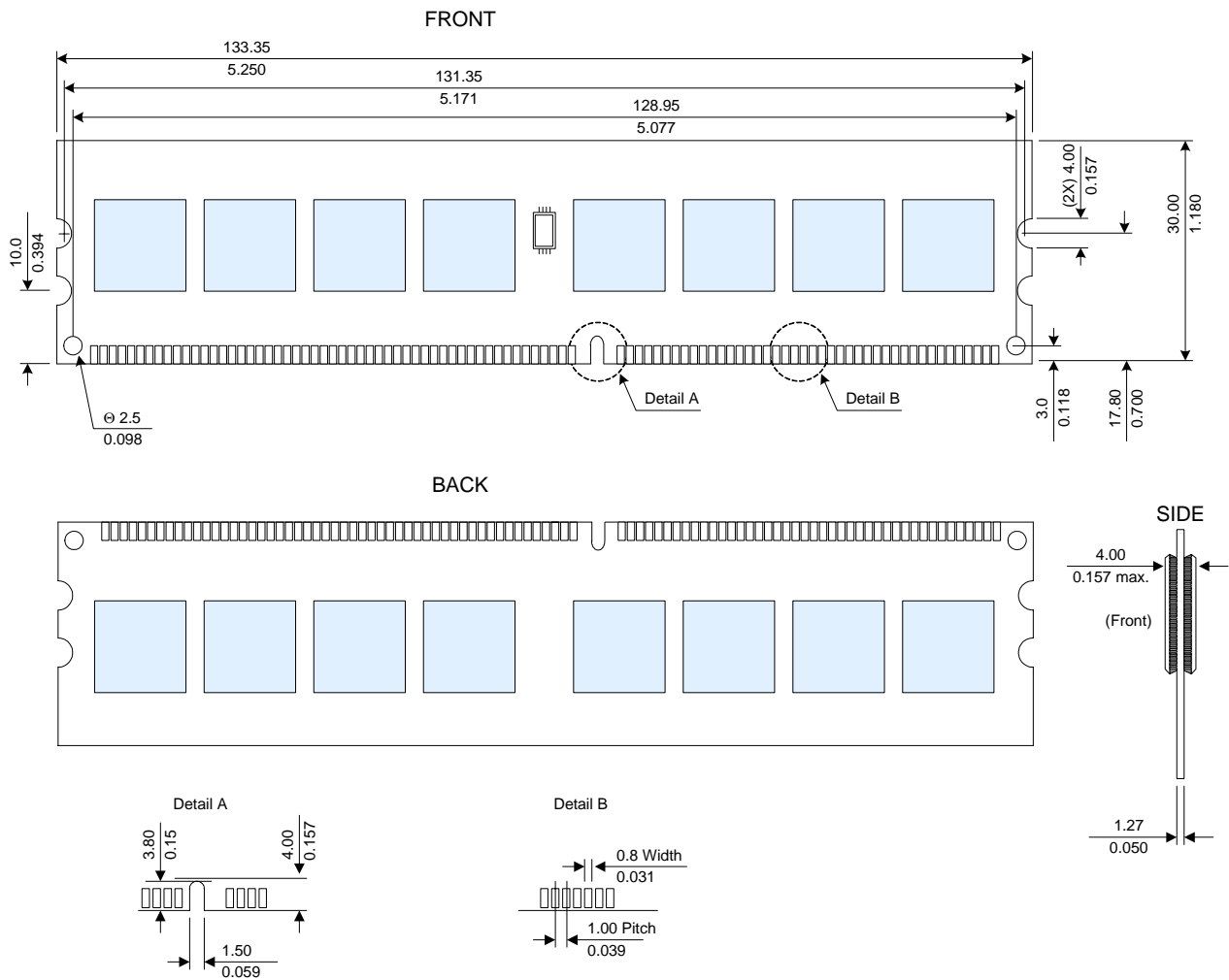


512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM

**Package Dimensions**

(1GB, 2 Rank, 64Mx8 DDR SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

**M1U51264TU88A0F / M1U51264TU88A0B / M1Y51264TU88A0B (Green)**  
**M1U1G64TU8HA0F / M1U1G64TU8HA0B / M1Y1G64TU8HA0B (Green)**

512MB: 64M x 64 / 1GB: 128M x 64

Unbuffered DDR2 SDRAM DIMM



## Revision Log

Rev	Date	Modification
0.1	01/2004	Preliminary Release
1.0	01/2005	Added I <sub>dd</sub> values
1.1	03/2005	Added DDR2-667 spec.