MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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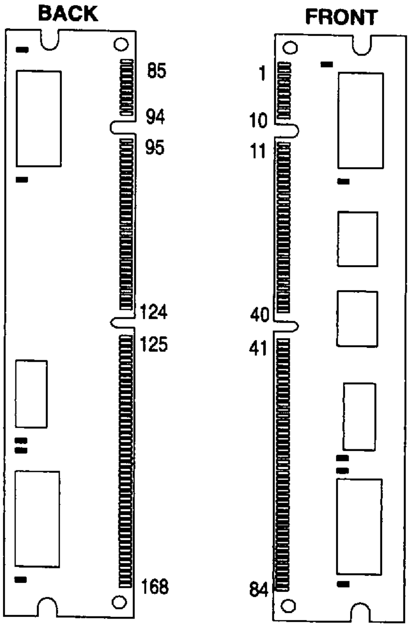
1M x 72
3.3 V, EDO, Buffered

DRAM Dual-In-Line Memory Module (DIMM)

For Error Correction Code Applications
8 Megabyte

- JEDEC–Standard 168–Lead Dual–In–Line Memory Module (DIMM)
- Single 3.3 V Power Supply, LVTTL–Compatible Inputs and Outputs
- Extended Data Out (EDO)
- $\overline{RAS}$–Only Refresh, $\overline{CAS}$ Before $\overline{RAS}$ Refresh, Hidden Refresh
- 8MB: 1024 Cycle Refresh: 16 ms (Max)
- Keys Prevent Accidental Insertion into 5 V Systems

1M x 72 (8MB)
168–LEAD DIMM
CASE 1115F–01



BACK NOT POPULATED ON 1M x 72 (8MB)

PART NUMBERS (See Last Page for Definitions)

Organization	60	70
1M x 72	MB721BJ58TADG60	MB721BJ58TADG70

KEY TIMING PARAMETERS

Speed	t_{RC} (ns)	t_{RAC} (ns)	t_{CAC} (ns)	t_{AA} (ns)	t_{EPC} (ns)
60	104	60	24	37	25
70	124	70	27	42	30

ADDITIONAL PARAMETERS

Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation	
			TTL	CMOS
8MB	60	3,240	58	47
	70	2,772		

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PIN ASSIGNMENTS

Front Side								Back Side							
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
1	V_{SS}	22	NC	43	V_{SS}	64	NC	85	V_{SS}	106	NC	127	V_{SS}	148	NC
2	DQ0	23	V_{SS}	44	$\overline{\text{G2}}$	65	DQ25	86	DQ36	107	V_{SS}	128	NC	149	DQ61
3	DQ1	24	NC	45	$\overline{\text{RAS2}}$	66	NC	87	DQ37	108	NC	129	NC	150	NC
4	DQ2	25	NC	46	$\overline{\text{CAS4}}$	67	DQ27	88	DQ38	109	NC	130	NC	151	DQ63
5	DQ3	26	V_{CC}	47	NC	68	V_{SS}	89	DQ39	110	V_{CC}	131	NC	152	V_{SS}
6	V_{CC}	27	$\overline{\text{WE0}}$	48	$\overline{\text{WE2}}$	69	DQ28	90	V_{CC}	111	NC	132	$\overline{\text{PDE}}$	153	DQ64
7	DQ4	28	$\overline{\text{CAS0}}$	49	V_{CC}	70	DQ29	91	DQ40	112	NC	133	V_{CC}	154	DQ65
8	DQ5	29	NC	50	NC	71	DQ30	92	DQ41	113	NC	134	NC	155	DQ66
9	DQ6	30	$\overline{\text{RAS0}}$	51	NC	72	DQ31	93	DQ42	114	NC	135	NC	156	DQ67
10	DQ7	31	$\overline{\text{G0}}$	52	DQ18	73	V_{CC}	94	DQ43	115	NC	136	DQ54	157	V_{CC}
11	NC	32	V_{SS}	53	DQ19	74	DQ32	95	NC	116	V_{SS}	137	DQ55	158	DQ68
12	V_{SS}	33	A0	54	V_{SS}	75	DQ33	96	V_{SS}	117	A1	138	V_{SS}	159	DQ69
13	DQ9	34	A2	55	DQ20	76	DQ34	97	DQ45	118	A3	139	DQ56	160	DQ70
14	DQ10	35	A4	56	DQ21	77	NC	98	DQ46	119	A5	140	DQ57	161	DQ71
15	DQ11	36	A6	57	DQ22	78	V_{SS}	99	DQ47	120	A7	141	DQ58	162	V_{SS}
16	DQ12	37	A8	58	DQ23	79	PD1	100	DQ48	121	A9	142	DQ59	163	PD2
17	DQ13	38	NC	59	V_{CC}	80	PD3	101	DQ49	122	NC	143	V_{CC}	164	PD4
18	V_{CC}	39	NC	60	DQ24	81	PD5	102	V_{CC}	123	NC	144	DQ60	165	PD6
19	DQ14	40	V_{CC}	61	NC	82	PD7	103	DQ50	124	V_{CC}	145	NC	166	PD8
20	DQ15	41	NC	62	NC	83	ID0	104	DQ51	125	NC	146	NC	167	ID1
21	DQ16	42	NC	63	NC	84	V_{CC}	105	DQ52	126	B0	147	NC	168	V_{CC}

PRESENCE DETECT/ID BIT POPULATIONS

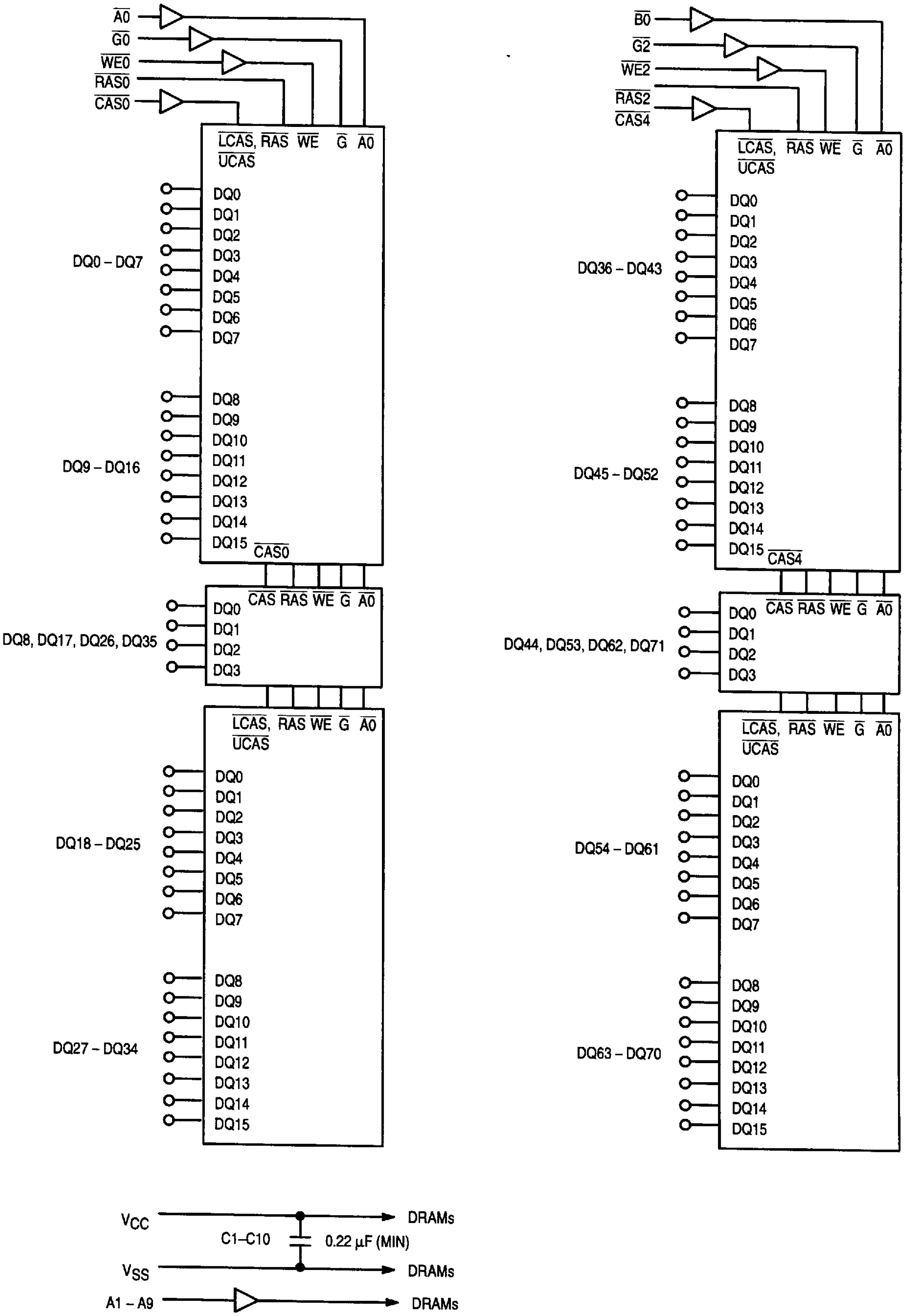
Pin Name		8MB
PD1		V_{OL}
PD2		V_{OL}
PD3		V_{OH}
PD4		V_{OL}
PD5		V_{OH}
PD6	60 70	V_{OH} V_{OL}
PD7	60 70	V_{OH} V_{OH}
PD8		V_{OL}
ID1		V_{SS}
ID0		V_{SS}

NOTE: IDs must be pulled up through a resistor to V_{CC} at the next higher level of assembly. PDs are buffered and gated to the edge connector by the $\overline{\text{PDE}}$ (presence detect enable) signal.

PIN NAMES

A0, B0, A1 – A9	Address Inputs
$\overline{\text{CAS0}}$, $\overline{\text{CAS4}}$	Column Address Strobe
$\overline{\text{WE0}}$, $\overline{\text{WE2}}$	Write Enable
PD1 – PD8	Buffered Presence Detect
$\overline{\text{PDE}}$	Presence Detect Output Enable
V_{SS}	Ground
DQ0 – DQ71	Data Input/Output
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{G0}}$, $\overline{\text{G2}}$	Output Enable
ID0, ID1	Unbuffered ID Bit
V_{CC}	Power
NC	No Connection

8MB BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.3 to + 4.6	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 0.3 to V_{CC} + 0.3	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.4	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.3**	—	0.8	V
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 30	—	30	µA
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	—	10	µA
Output High Voltage (I_{OH} = – 2 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	—	—	0.4	V

* V_{CC} + 1.2 V at pulse widths ≤ 20 ns.
** – 1.2 V at pulse widths ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All Voltages Referenced to V_{SS})

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	60 70	I_{CC1}	— —	900 770	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{IH})		I_{CC2}	—	16	mA	
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min)	60 70	I_{CC3}	— —	900 770	mA	1, 2
V_{CC} Power Supply Current (t_{EPC} = t_{EPC} Min) During EDO Cycle	60 70	I_{CC4}	— —	640 590	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V_{CC} – 0.2 V)		I_{CC5}	—	13	mA	
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min) During $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle	60 70	I_{CC6}	— —	900 770	mA	1

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL} and $\overline{\text{CAS}}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 3.3 V, Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	8MB Max	Unit
Addresses, $\overline{\text{W}}$, $\overline{\text{G}}$, $\overline{\text{CAS}}$, PDE	C_{in}	16	pF
$\overline{\text{RAS}}$	C_{in}	31	pF
DQ	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		70		Unit	Notes
	Std	**Alt**	**Min**	**Max**	**Min**	**Max**		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	104	—	124	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	140	—	165	—	ns	5
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7, 8, 9
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	24	—	27	ns	6, 8, 10
Access Time from Column Address	t_{AVQV}	t_{AA}	—	37	—	42	ns	6, 9, 11
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	42	—	47	ns	6
$\overline{\text{CAS}}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	2	—	2	—	ns	
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	2	22	2	22	ns	12, 13
Transition Time (Rise and Fall)	t_T	t_T	2	50	2	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	22	—	27	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	50	—	60	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	10	10 k	15	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	18	36	18	43	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	13	23	13	28	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	12	—	12	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	12	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	7	—	7	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	8	—	8	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	2	—	2	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	17	—	22	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	37	—	42	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	2	—	2	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power–up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, instead of 8 $\overline{\text{RAS}}$ only refresh cyces are required.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min), t_{RWC} (min), and t_{EPC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C $\le T_A \le$ 70°C) is ensured.
6. Measured with a current load equivalent to 1 LVTTL (– 2 mA, + 2 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
10. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
11. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
12. t_{OFF} (max), t_{REZ} (max), t_{WEZ} (max), and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ goes high, the open circuit condition is controlled by $\overline{\text{CAS}}$ going high (t_{OFF}). If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ goes high, the open circuit condition is controlled by $\overline{\text{RAS}}$ going high (t_{REZ}).

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (continued)

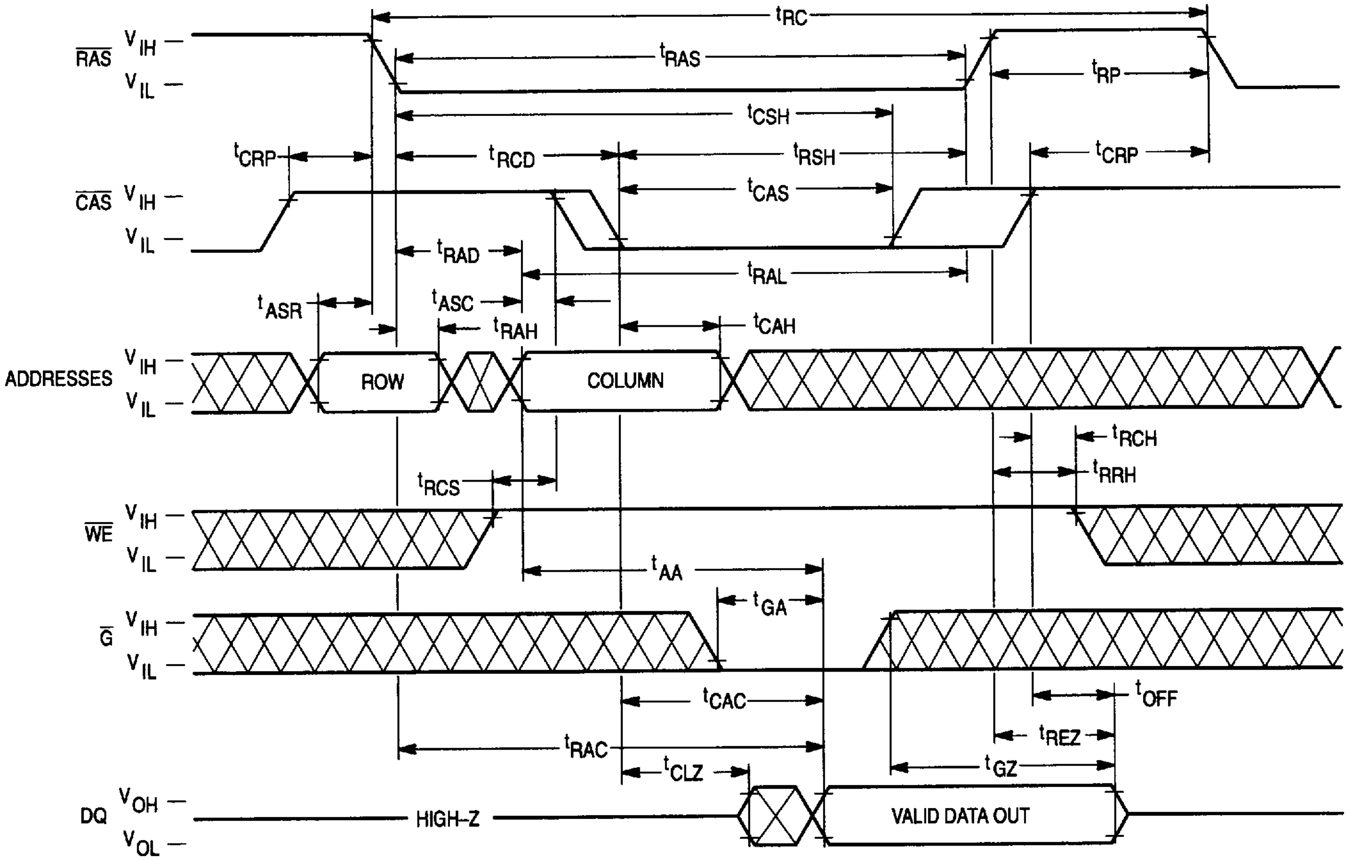
	Symbol		60		70			
Parameter	**Std**	**Alt**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CEHWX}	t_{RCH}	2	—	2	—	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{REHWX}	t_{RRH}	0	—	0	—	ns	14
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{CELWH}	t_{WCH}	17	—	22	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{WLREH}	t_{RWL}	22	—	27	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{WLCEH}	t_{CWL}	10	—	15	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	–2	—	–2	—	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	17	—	22	—	ns	15
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	2	—	2	—	ns	16
$\overline{\text{CAS}}$ to Write Delay	t_{CELWL}	t_{CWD}	36	—	44	—	ns	16
$\overline{\text{RAS}}$ to Write Delay	t_{RELWL}	t_{RWD}	79	—	89	—	ns	16
Column Address to Write Delay	t_{AVWL}	t_{AWD}	49	—	59	—	ns	16
$\overline{\text{CAS}}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	56	—	66	—	ns	16
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{CELCEL}	t_{CSR}	7	—	7	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	t_{RELCEH}	t_{CHR}	8	—	13	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	—	25	—	ns	
$\overline{\text{G}}$ Access Time	t_{GLQV}	t_{GA}	—	22	—	27	ns	6
$\overline{\text{G}}$ to Data Delay	t_{GLHDX}	t_{GD}	17	—	22	—	ns	
Output Buffer Turn–Off Delay from $\overline{\text{G}}$	t_{GHQZ}	t_{GZ}	0	15	0	20	ns	12
$\overline{\text{G}}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (EDO)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO)	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	ns	
$\overline{\text{RAS}}$ to Next $\overline{\text{CAS}}$ Delay (EDO)	t_{RELCEL}	t_{RNCD}	60	—	70	—	ns	
EDO Cycle Time	t_{CELCEL}	t_{EPC}	25	—	30	—	ns	
EDO Read–Write Cycle Time	t_{CELCEL}	t_{ERWC}	68	—	75	—	ns	
Output Data Hold Time	t_{CELQZ}	t_{COH}	5	—	5	—	ns	
Output Buffer Turn–Off Delay from $\overline{\text{RAS}}$	t_{REHQZ}	t_{REZ}	0	15	0	20	ns	12, 13
Output Buffer Turn–Off Delay from $\overline{\text{WE}}$	t_{WLQZ}	t_{WEZ}	0	15	0	20	ns	12
$\overline{\text{WE}}$ to Data Delay	t_{WLDV}	t_{WED}	15	—	20	—	ns	
$\overline{\text{G}}$ Precharge Time	t_{GHGL}	t_{GP}	10	—	12	—	ns	

NOTES:

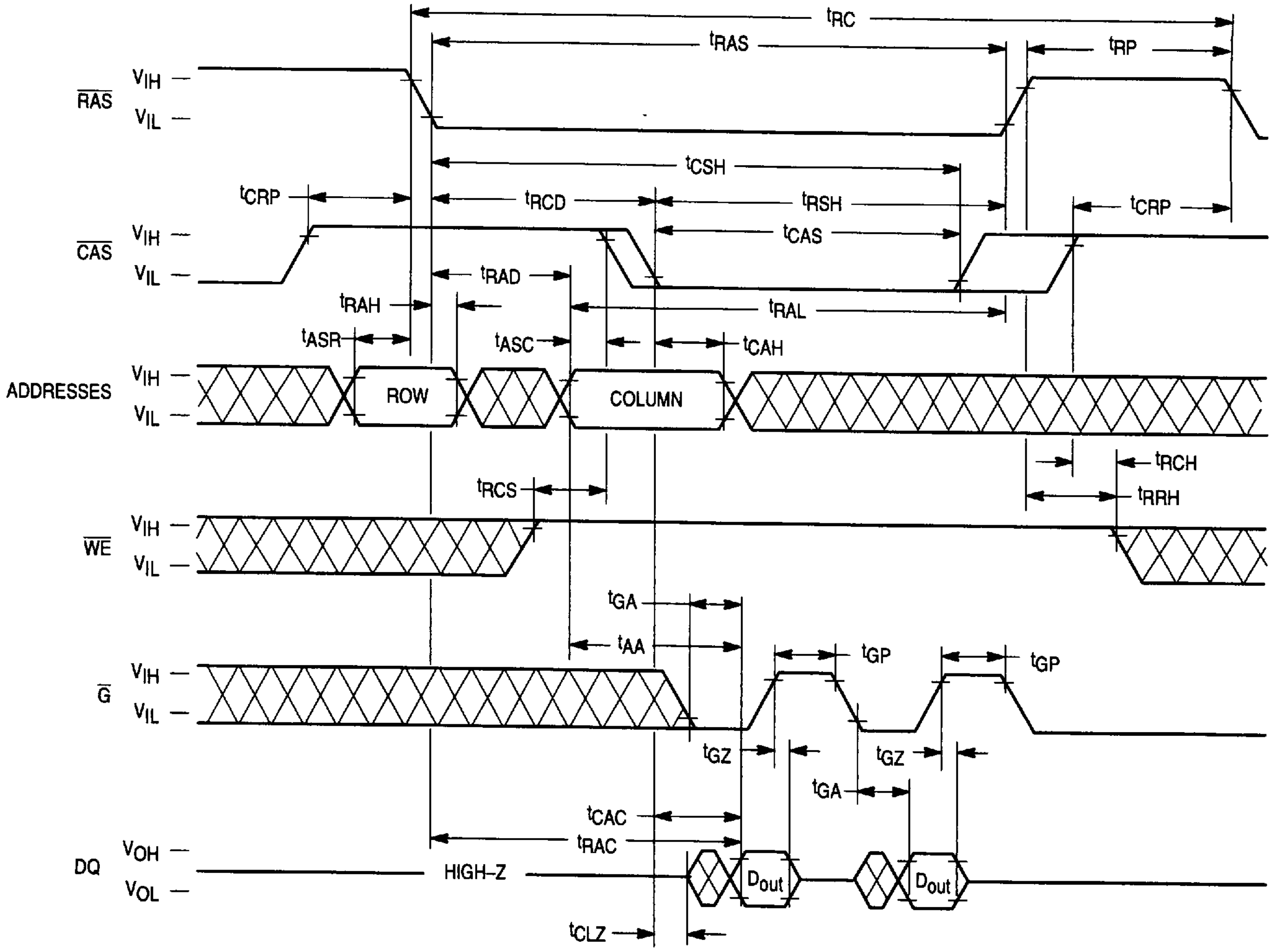
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read–write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), (extended data out), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

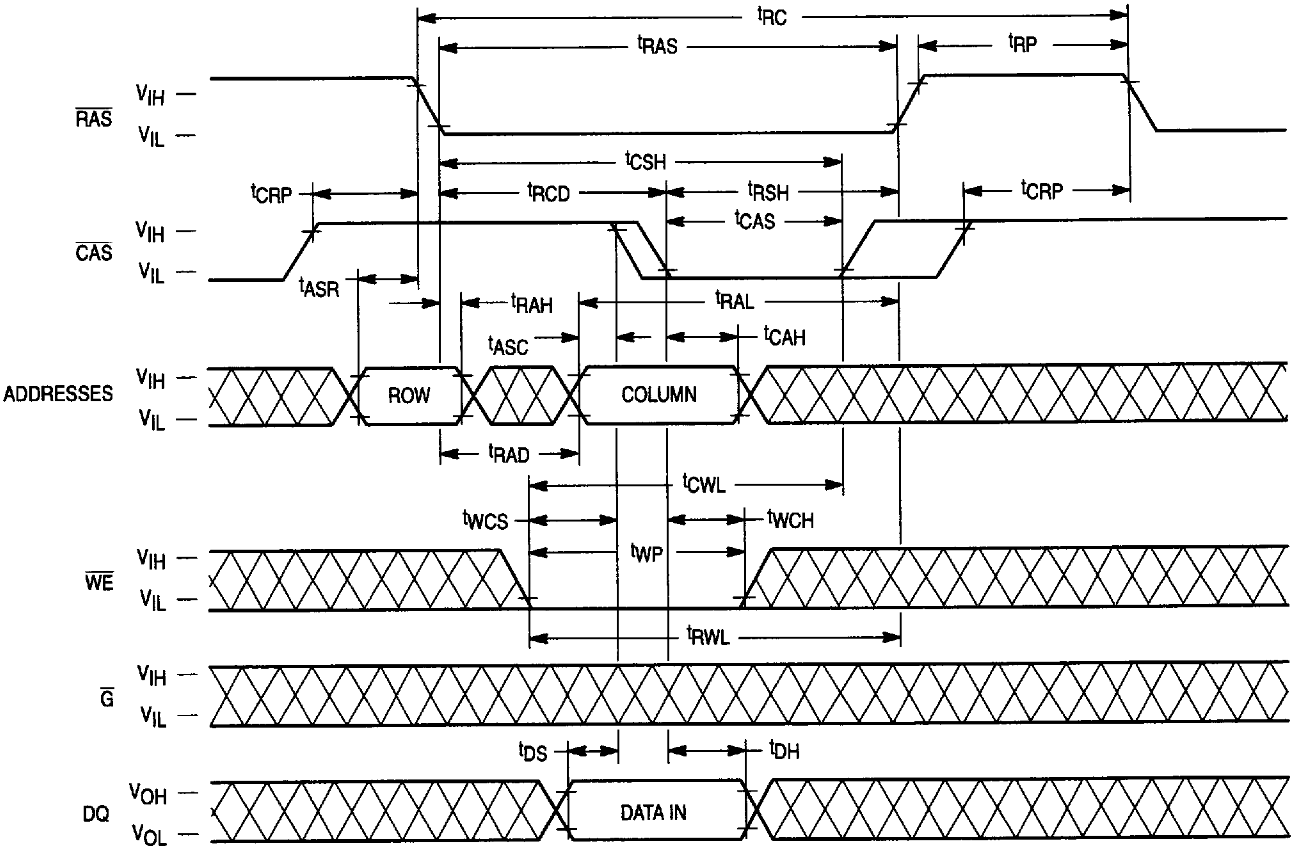
READ CYCLE



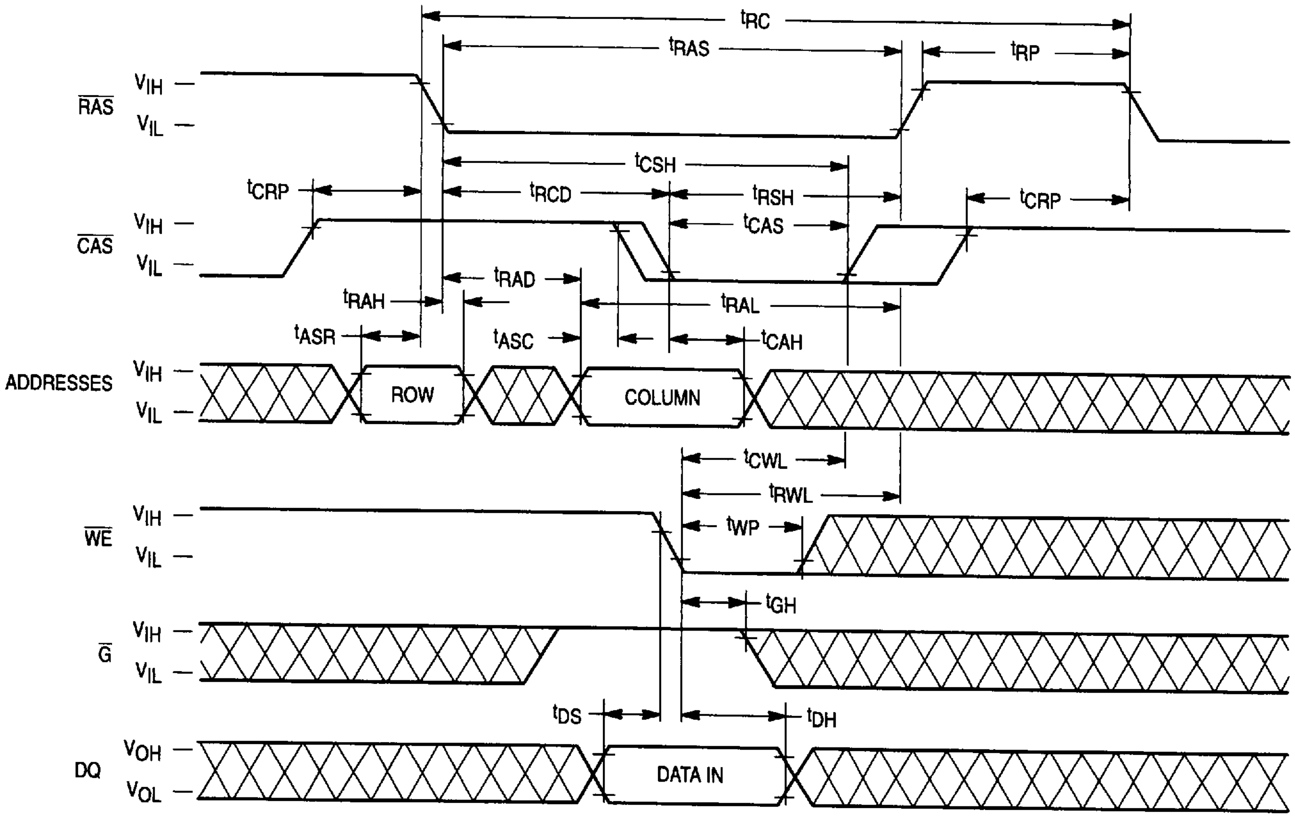
READ CYCLE ($\overline{G}$ CONTROLLED READ)



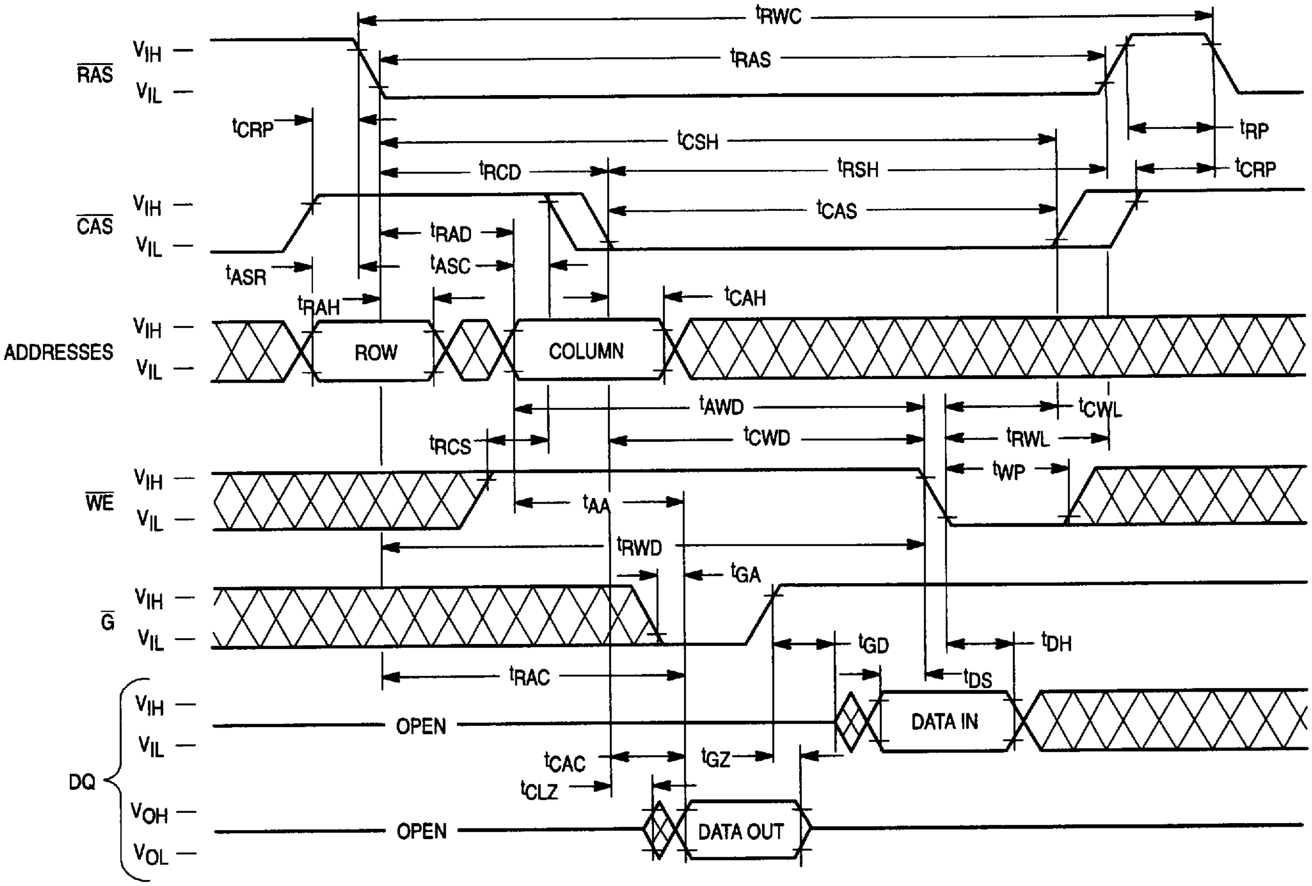
WRITE CYCLE (EARLY WRITE)



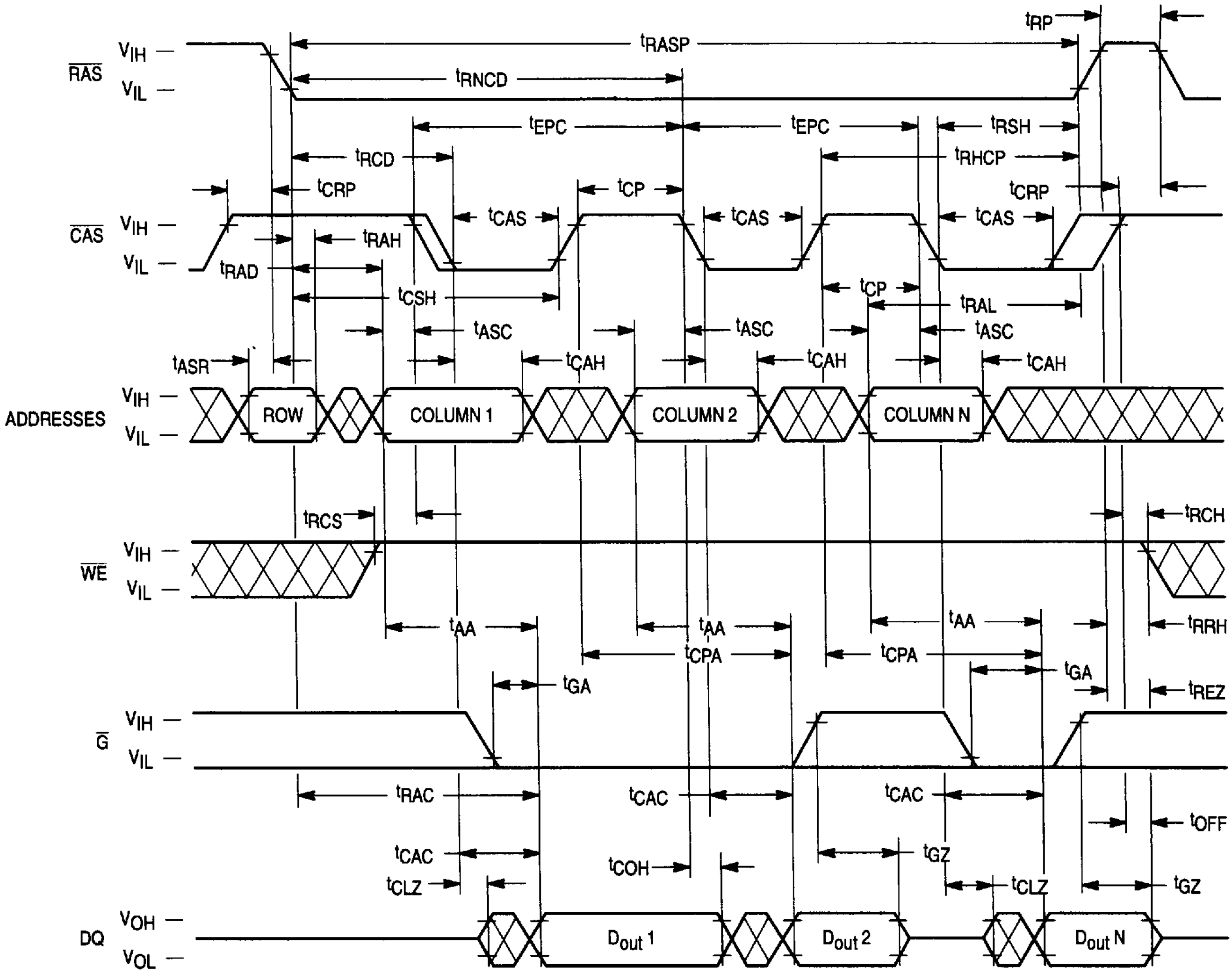
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



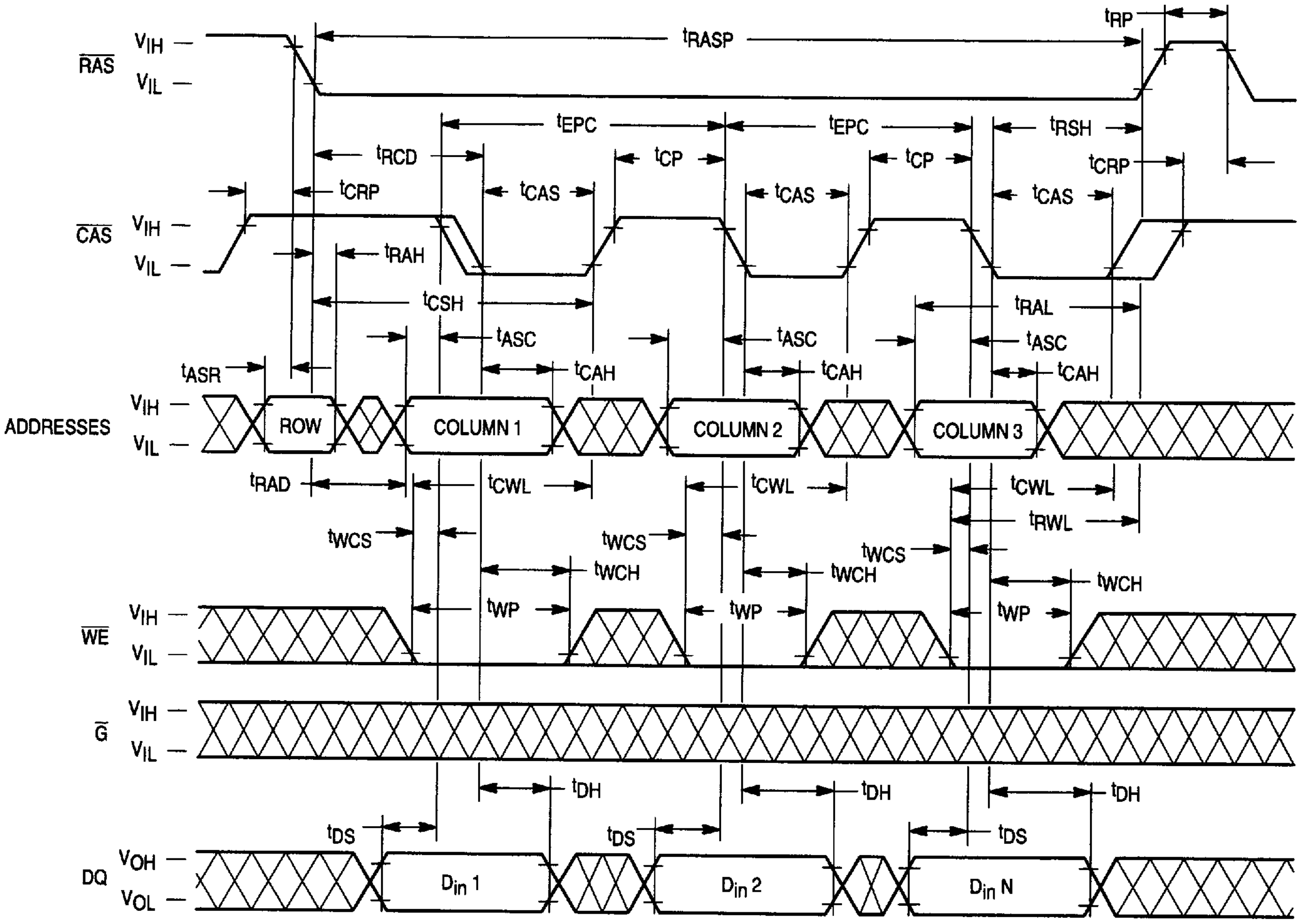
READ–WRITE CYCLE



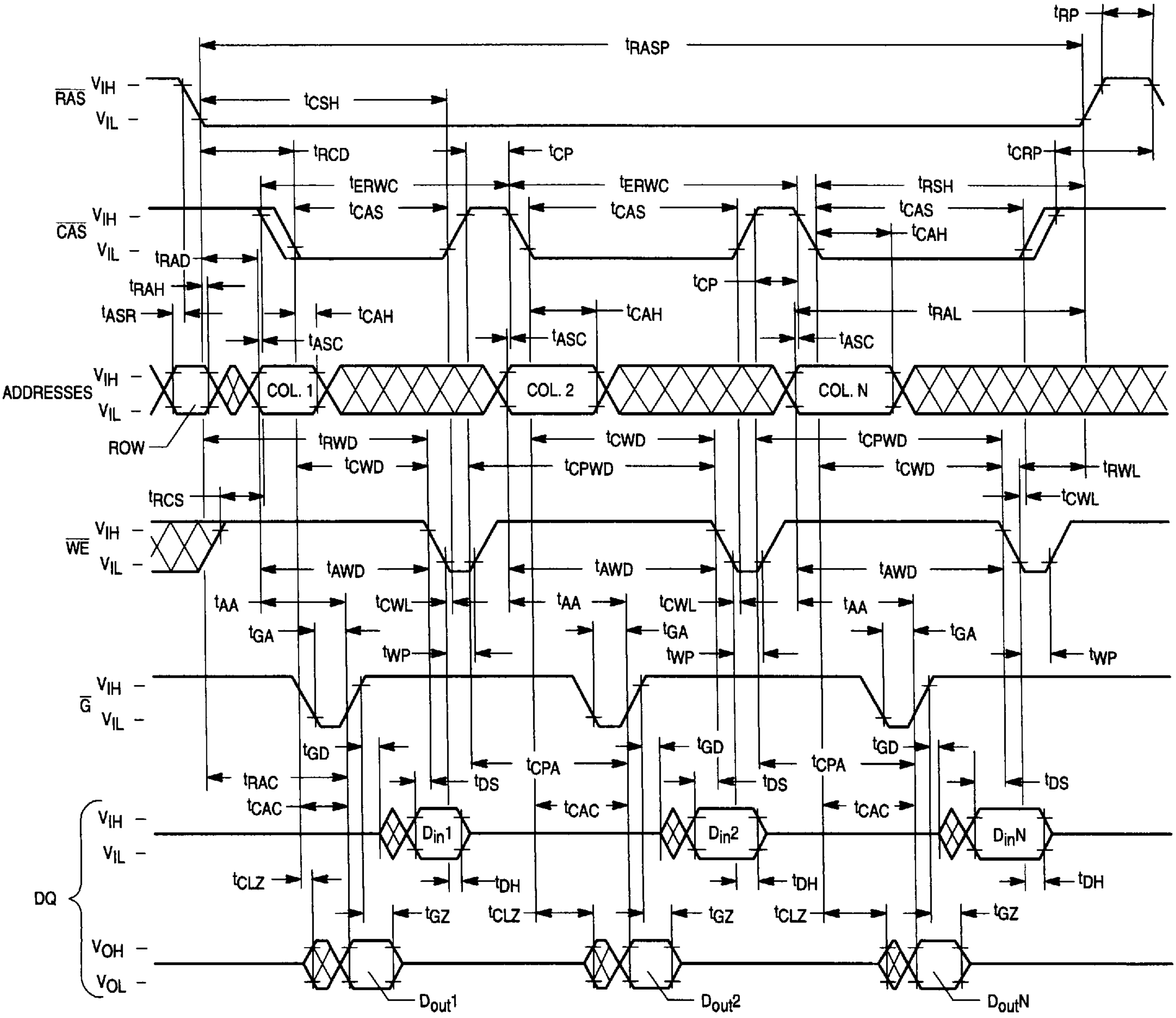
EXTENDED DATA OUT READ CYCLE



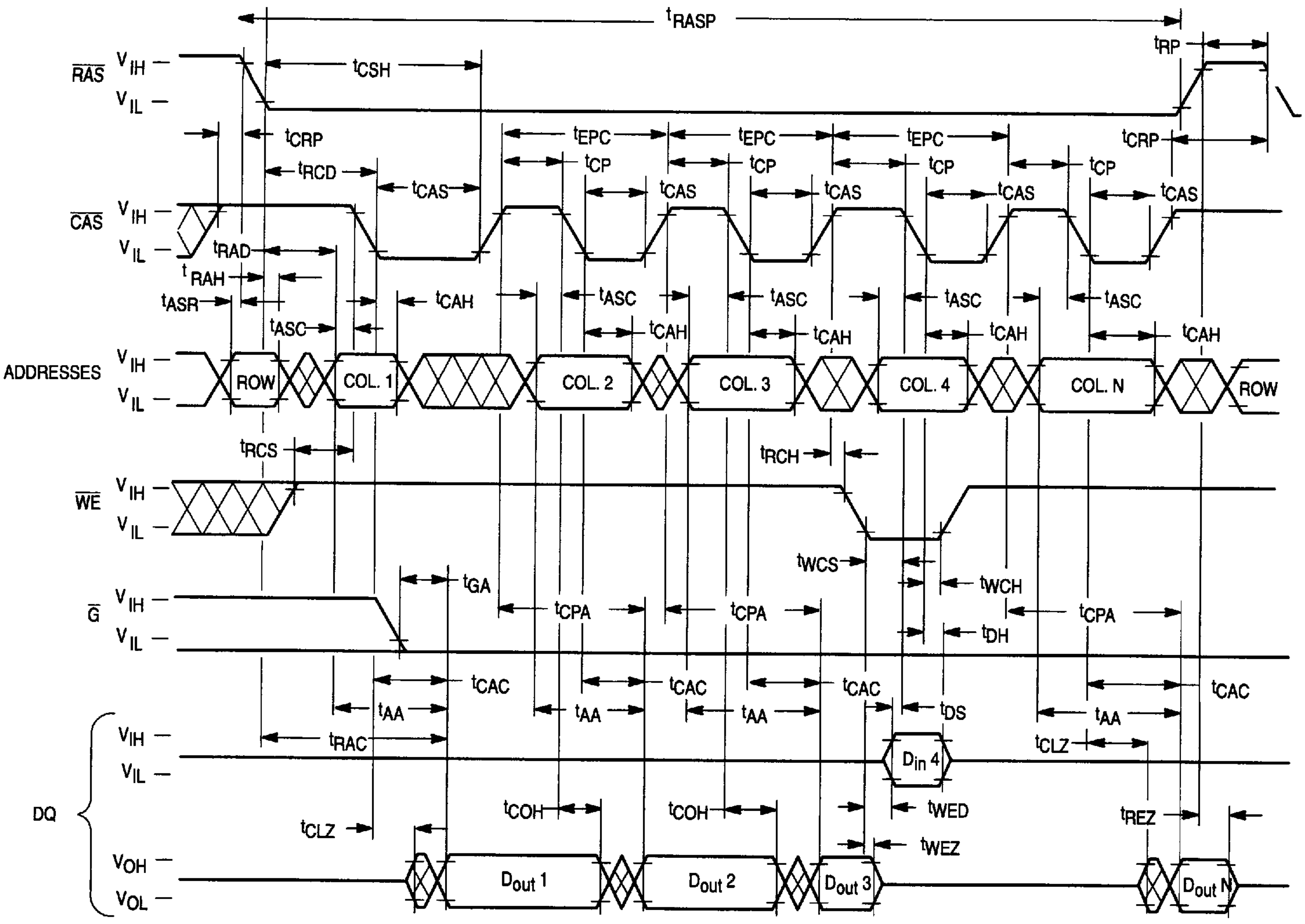
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



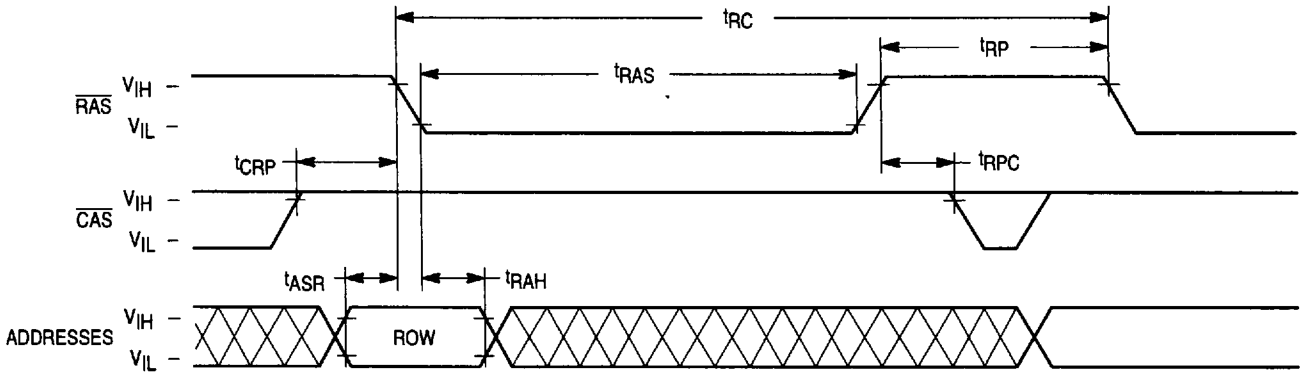
EXTENDED DATA OUT READ–WRITE CYCLE



EXTENDED DATA OUT READ–WRITE MIXED CYCLE

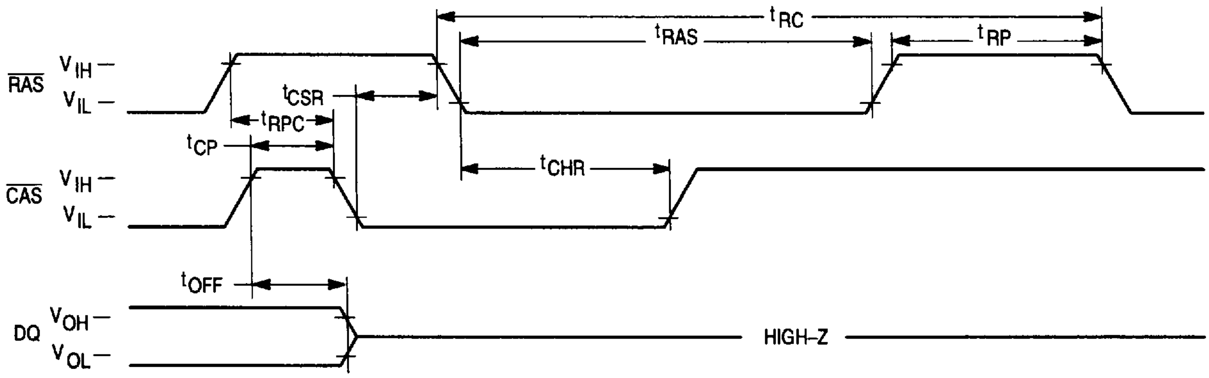


RAS–ONLY REFRESH CYCLE



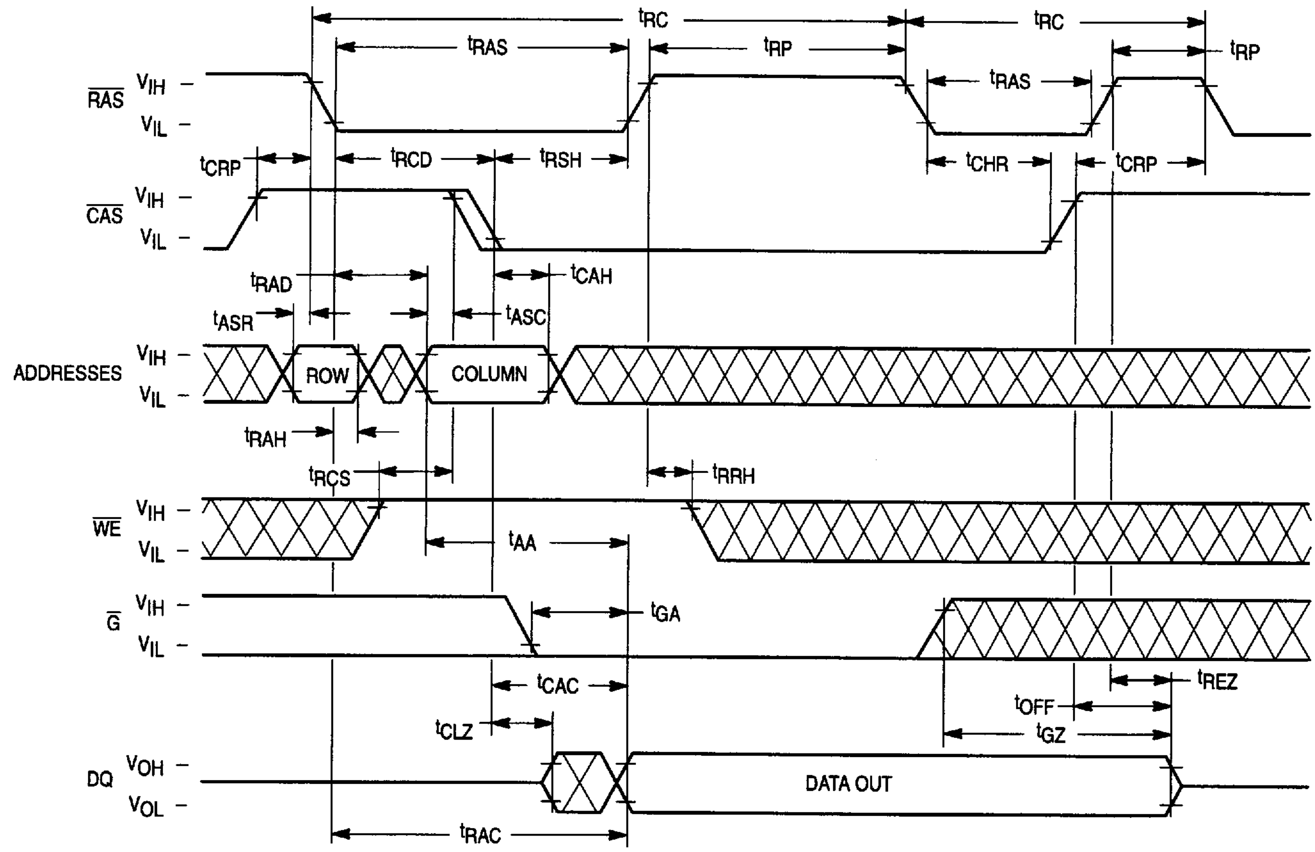
NOTE: WE, G = H or L.
DQ = Open.

CAS BEFORE RAS REFRESH CYCLE

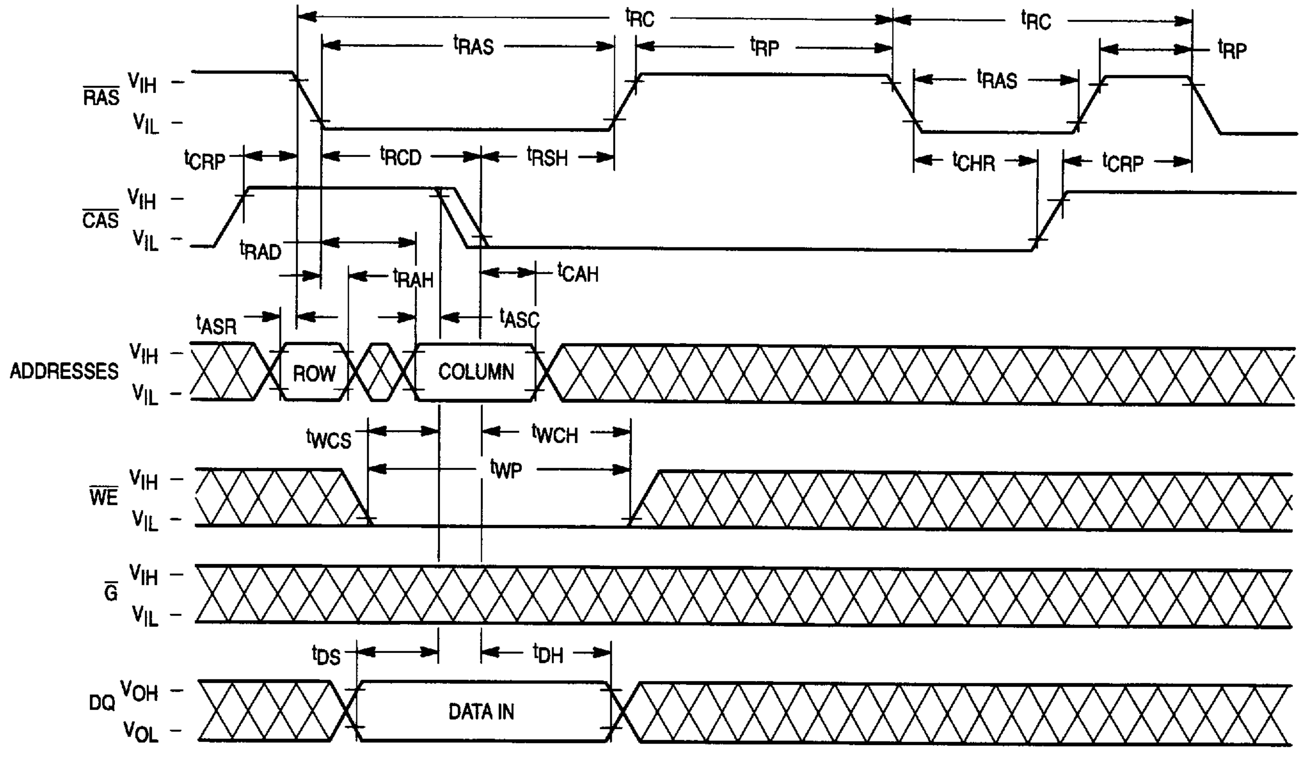


NOTE: Addresses = H or L.
8MB: W = H or L.

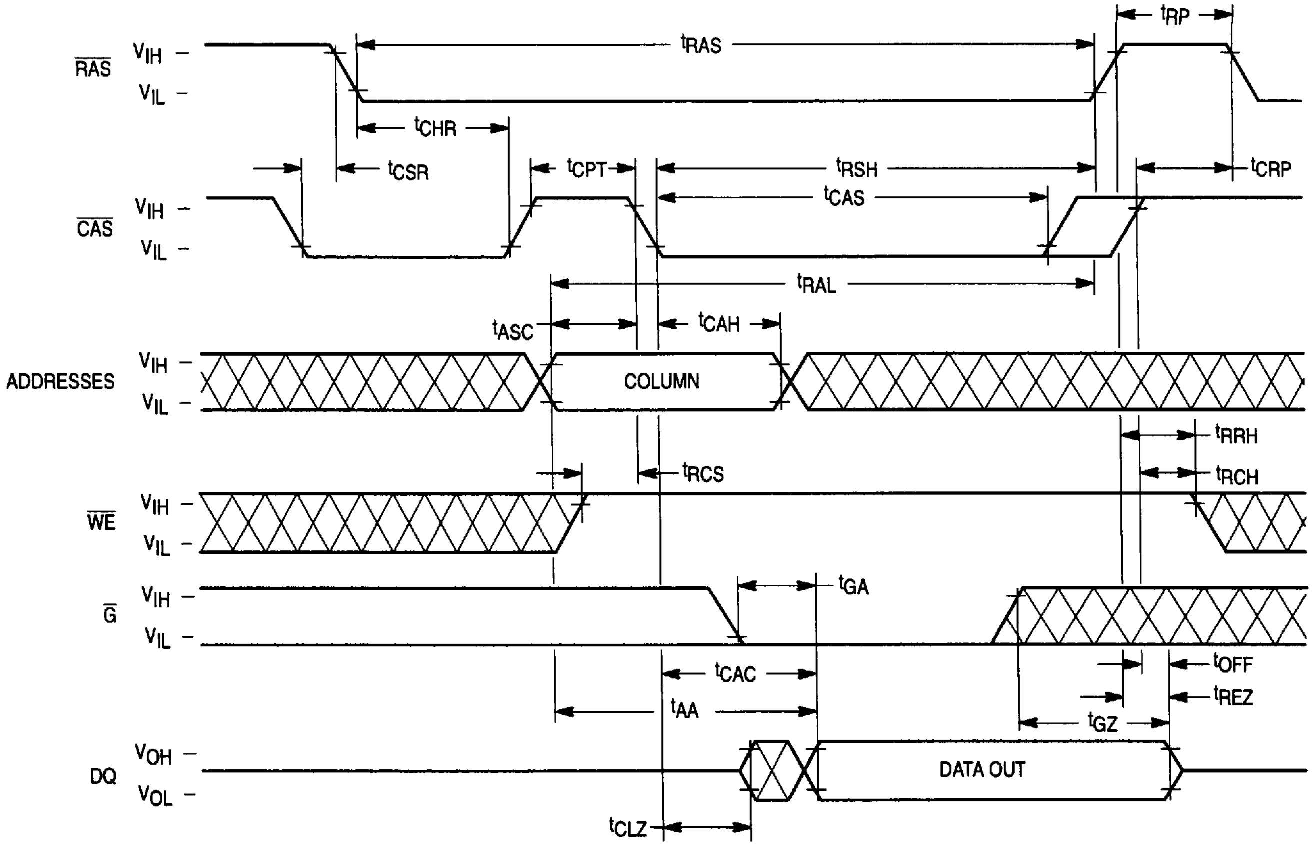
HIDDEN REFRESH CYCLE (READ)



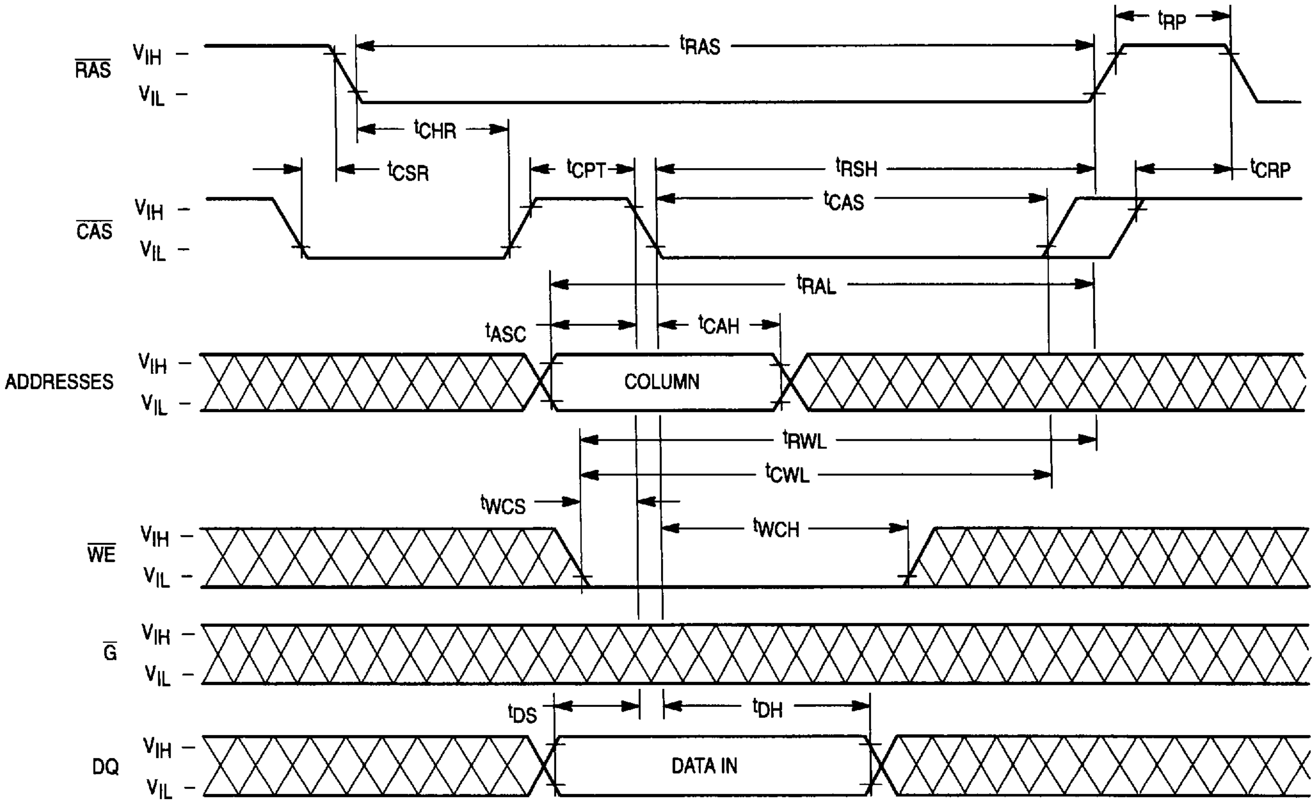
HIDDEN REFRESH CYCLE (WRITE)



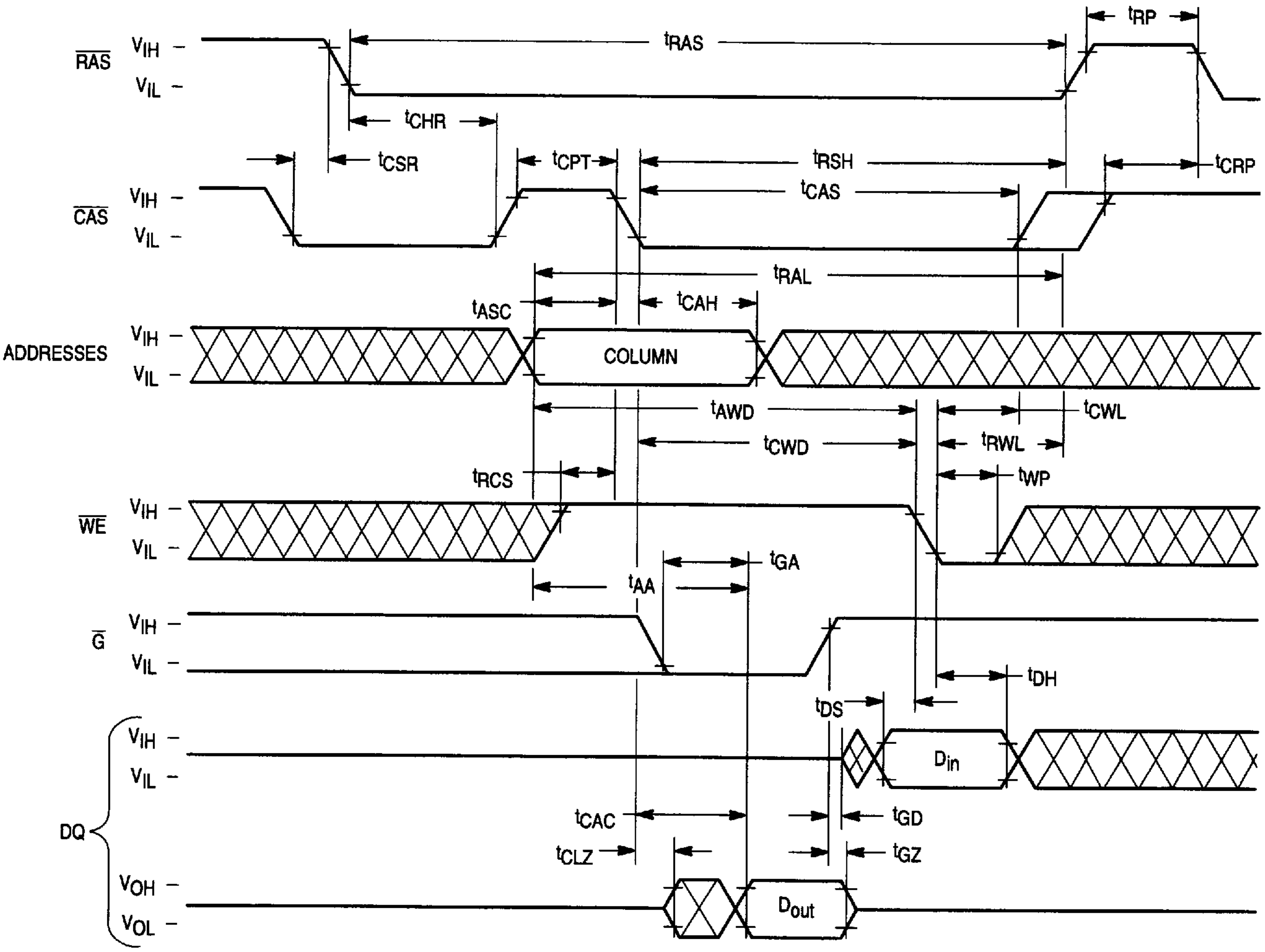
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ CYCLE



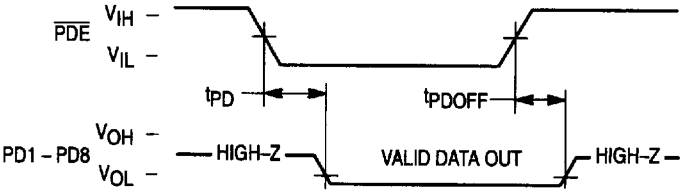
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST WRITE CYCLE



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST READ–WRITE CYCLE



PRESENCE DETECT ENABLE CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 µs is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 ms with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate address fields. For the 8MB modules a total of 20 address bits, 10 rows and 10 columns, will decode one of the word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, extended data out read cycle, read–write cycle, and extended data out read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}–t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, extended data out early write, and extended data out read–write. Early and late write modes are discussed here, while extended data out write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

A late–write cycle (referred to as $\overline{G}$–controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 µs after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition. Outputs are switched off by $\overline{G}$ inactive transition, which is required to write to the device. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle. $\overline{G}$ devices must remain inactive for t_{GH} after $\overline{W}$ active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

EDO MODE CYCLES

EDO mode allows fast successive data operations at all column locations on a selected row. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. EDO mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

An EDO mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first EDO mode cycle (t_{EPC} or t_{ERWC}). Either a read, write, or read–write operation can be performed in an EDO mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive EDO mode cycles and performed in any order. The maximum number of consecutive EDO mode cycles is limited by t_{RASP}. EDO mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every t_{RFSH}.

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 µs. Burst refresh, a refresh of all rows consecutively, must be performed every t_{RFSH}.

A normal read, write, or read–write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test.** This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after completing one cycle for each column as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle.** Repeat this operation for every column.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle.** Repeat this operation for every column.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

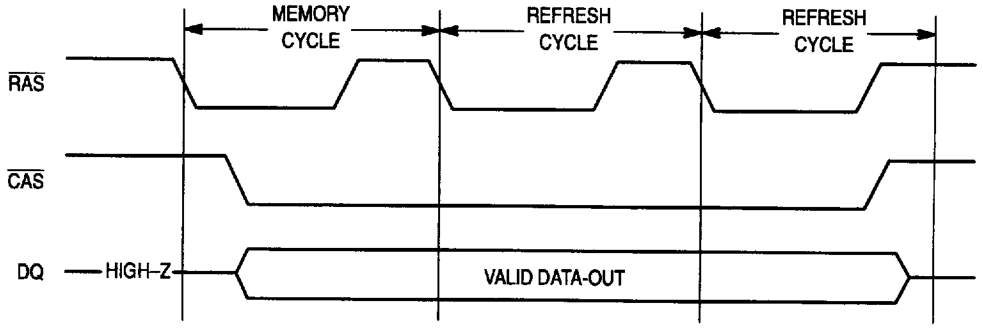
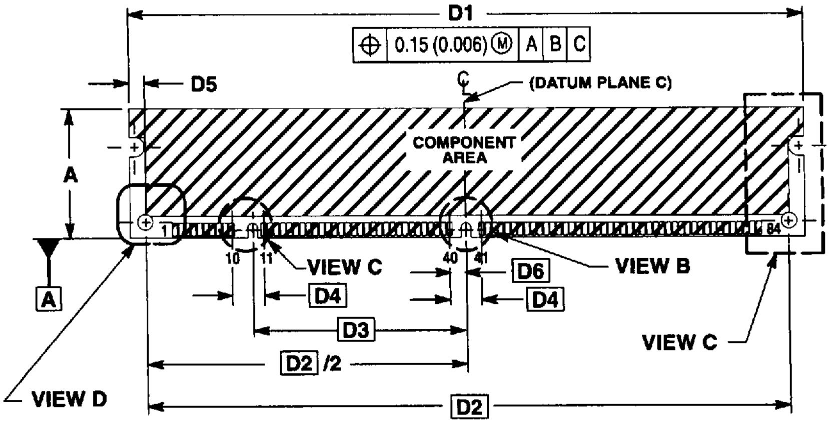


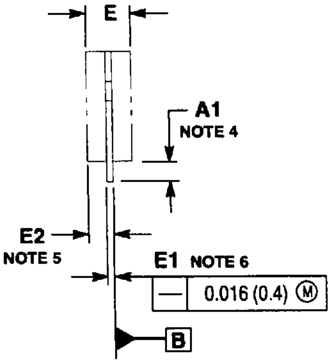
Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSIONS

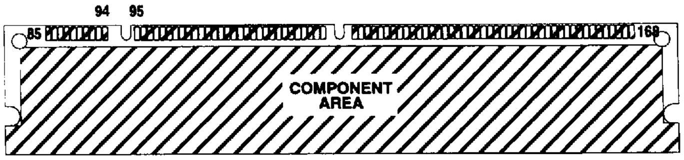
1M x 72 (8MB)
168–LEAD DIMM
CASE 1115F–01



FRONT VIEW



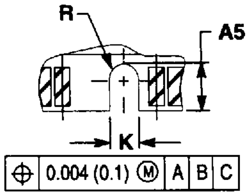
SIDE VIEW



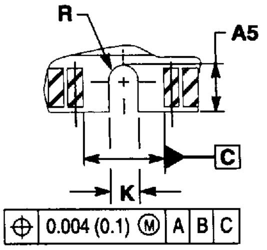
BACK VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS E AND A1 DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION E2 DEFINES OPTIONAL SINGLE–SIDED MODULE
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.
7. D5 DIMENSION DEFINES SLOT END AND EDGE OF COMPONENT AREA.

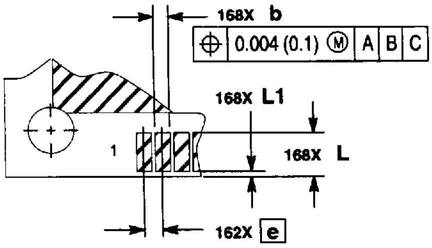


VIEW A

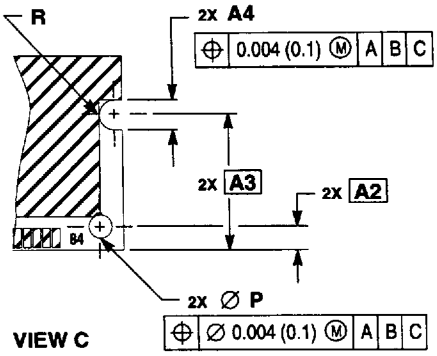


VIEW B

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.995	1.005	25.27	25.53
A1	0.158	—	4.00	—
A2	0.118 BSC		3.00 BSC	
A3	0.700 BSC		17.78 BSC	
A4	0.154	0.161	3.90	4.10
A5	0.118	0.128	3.00	3.25
b	0.037	0.041	0.95	1.05
D1	5.245	5.255	133.22	133.48
D2	5.014 BSC		127.35 BSC	
D3	1.700 BSC		43.18 BSC	
D4	0.250 BSC		6.35 BSC	
D5	0.118	—	3.00	—
D6	0.125 BSC		3.175 BSC	
e	0.050 BSC		1.27 BSC	
E	—	0.354	—	9.00
E1	0.046	0.054	1.17	1.37
E2	—	0.205	—	5.20
K	0.075	0.083	1.90	2.10
L	0.100	—	2.54	—
L1	—	0.010	—	0.25
P	0.114	0.122	2.90	3.10



VIEW D



VIEW C

ORDERING INFORMATION
(Order by Full Part Number)

M B 72 X B X XX X X X X XX

- M — Motorola Memory Prefix
- B — EDO
- 72 — Width
- X — Depth (1 = 1M)
- B — Component Die Revision: B–Revision — 1M x 16
- X — Component Package (J = SOJ)
- XX — Data Characters: 58 = Commercial, Buffered, 3.3 V, x16 DRAM–Based, Square Refresh
- X — Fab (T = TSB/TSC)
- X — A = Board Type/Revision
- X — D = DIMM
- X — Pad Metal (G = Gold)
- XX — Speed (60 = 60 ns, 70 = 70 ns)

Full Part Numbers — MB721BJ58TADG60
MB721BJ58TADG70

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