

## CMOS Programmable Electrically Erasable Logic Device

February 1993

### Features

#### Advanced CMOS EEPROM Technology

#### Low Power Consumption

- 65mA + 1mA/MHz Max

#### High Performance

- tPD = 30ns Max, tOE = 30ns Max

#### Architectural Flexibility

- 12 Inputs and 10 I/Os
- Programmable-AND/OR arrays with 42 product terms/10 sum terms

#### EE Reprogrammability

- Superior programming and functional yield
- Low-cost, "windowless" package
- Erases and programs in seconds

#### FPLA Architecture

- Superset Replacement for PLS173
- 10 additional product terms
- Output-enable terms in OR array
- Signature word
- Foolproof design security

#### Application Versatility

- Replaces random SSI/MSI logic
- Creates customized comparators, multiplexers, encoders, converters, etc.

#### Development Support

- Third-party software and programmers
- AMI PEEL Development System with APEEL Logic Assembler

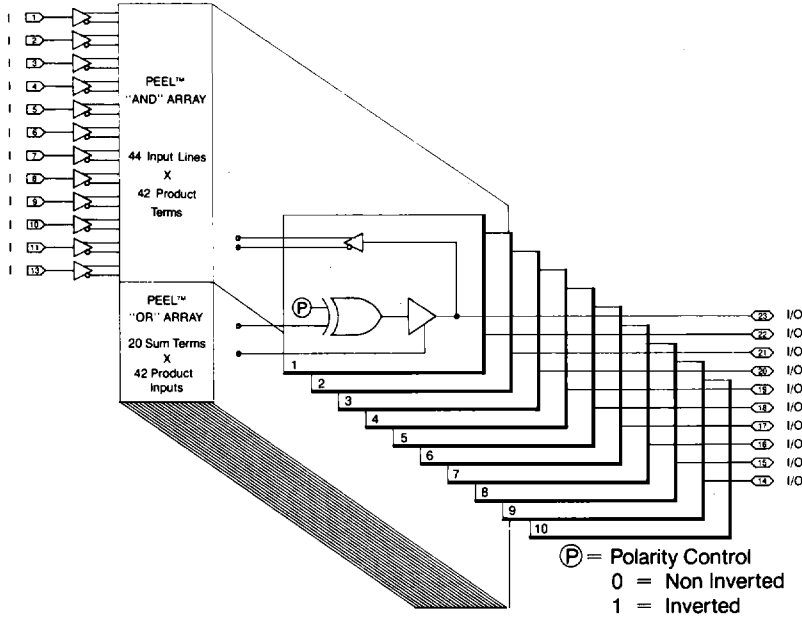
### General Description

The AMI PEEL273 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL273 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL273 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low-cost, "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

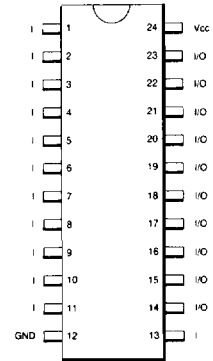
The PEEL273 provides both a programmable-AND array and a programmable-OR array. It offers superset compatibility with the bipolar PLS173 with several architectural enhancements, including output enable terms in the OR array, 10 additional product terms, and signature word. Applications for the PEEL273 cover a wide range of combinatorial functions: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL273 is supported by popular development tools and programmers from third-party manufacturers, and by AMI's APEEL Logic Assembler.

**Figure 40: PEEL273 Pin and Block Diagram**

**Block Diagram**



**Pin Diagram**



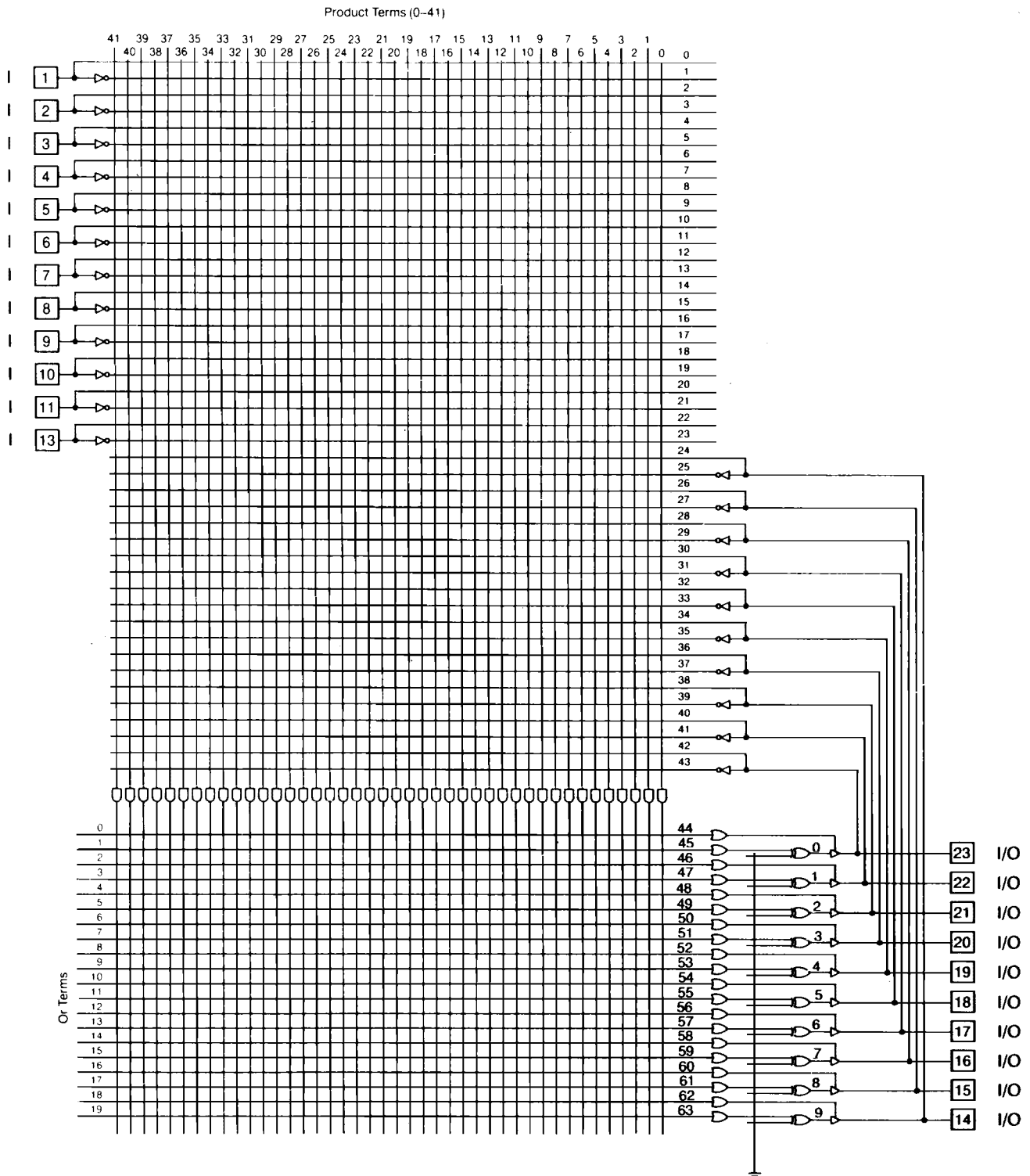
**Pin Names**

- I = Input Only
- I/O = Bi-Directional Input/Output
- GND = Ground
- Vcc = Power Supply (+5V)

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### Figure 41: PEEL273 Logic Array Diagram



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**CMOS Programmable Electrically Erasable Logic Device**
**Absolute Values**
**Absolute Maximum Ratings<sup>8</sup>**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>cc</sub>	Supply Voltage	Relative to GND	-0.5	7.0	V
V <sub>i</sub>	Voltage applied to Input <sup>4</sup>	Relative to GND <sup>1,10</sup>	-0.5	V <sub>cc</sub> +0.6	V
V <sub>o</sub>	Voltage applied to Output	Relative to GND <sup>1</sup>	-0.5	V <sub>cc</sub> +0.6	V
I <sub>o</sub>	Output Current	Per pin (I <sub>ol</sub> , I <sub>oh</sub> )		+25	mA
T <sub>st</sub>	Storage Temperature		-65	+150	C
T <sub>lt</sub>	Lead Temperature	(soldering 10 seconds)		+300	C

**Operating Ranges**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>cc</sub>	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T <sub>a</sub>	Operating Temperature	Commercial	0	+70	C
		Industrial	-40	+85	C
T <sub>r</sub>	Clock Rise Time <sup>5</sup>	Test points at 10% and 90% levels		250	ns
T <sub>f</sub>	Clock Fall Time <sup>5</sup>	Test points at 10% and 90% levels		250	ns
T <sub>rvcc</sub>	V <sub>cc</sub> Rise Time <sup>5</sup>	Test points at 10% and 90% levels		250	ms

**DC Characteristics (Over Operating Range Specifications)**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>il</sub>	Input Leakage	V <sub>in</sub> = GND to V <sub>cc</sub>			±10	μA
I <sub>oz</sub>	Output Leakage	I/O = High Impedance V <sub>o</sub> = GND to V <sub>cc</sub>			±10	μA
V <sub>il</sub>	Input Low Voltage		-0.3		0.8	V
V <sub>ih</sub>	Input High Voltage		2.0		V <sub>cc</sub> +0.3	V
V <sub>ol</sub>	Output Low Voltage TTL	I <sub>ol</sub> = +8.0mA <sup>12</sup>			0.45	V
V <sub>olc</sub>	Output Low Voltage CMOS	I <sub>ol</sub> = 10μA <sup>12</sup>			0.1	V
V <sub>oh</sub>	Output High Voltage TTL	I <sub>oh</sub> = -4.0mA <sup>12</sup>	2.4			V
V <sub>ohc</sub>	Output High Voltage CMOS	I <sub>oh</sub> = -10μA <sup>12</sup>	V <sub>cc</sub> -0.1			v

**Capacitance**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>in</sub> <sup>3,7</sup>	Input Capacitance	Frequency = 1MHz		4	6	pF
C <sub>out</sub> <sup>3,7</sup>	Output Capacitance	Frequency = 1MHz		8	12	pF
C <sub>clk</sub> <sup>3,7</sup>	Clk Pin Capacitance	Frequency = 1MHz		8	13	pF

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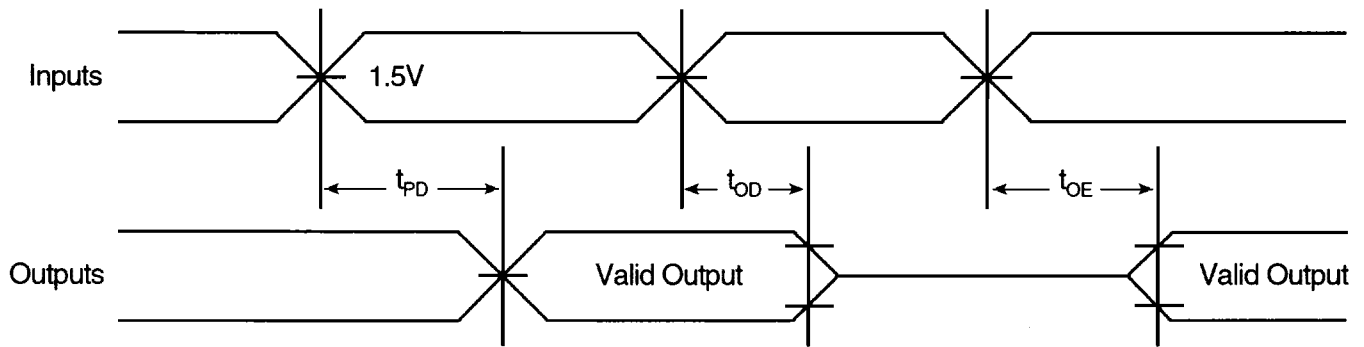
**Electrical Characteristics (Over Operating Range Specifications)**

SYMBOL	PARAMETER	UNITS	MIN	MAX
I <sub>CCS</sub>	V <sub>CC</sub> Current Standby <sup>9</sup>	mA		65
I <sub>CCA</sub>	V <sub>CC</sub> Current Active <sup>9</sup>	mA		I <sub>CCS</sub> + 0.5 mA/MHz
t <sub>PD</sub>	Input <sup>4</sup> to combinatorial output	ns		30
t <sub>OD</sub>	Input <sup>4</sup> to output disable <sup>11</sup>	ns		30
t <sub>OE</sub>	Input <sup>4</sup> to output enable <sup>11</sup>	ns		30

**NOTES:**

1. Minimum DC input is -0.5V; however, inputs may undershoot to -2.0V for periods less than 30ns.
2. Voltage applied to input or output must not exceed V<sub>CC</sub>+1.0V.
3. These measurements are periodically sample tested.
4. "Input" refers to an Input signal.
5. Test points assume signal transitions of 5ns or less from the 10% and 90% points, and timing reference levels of 1.5V (unless otherwise specified).
6. See AC test point/load circuit table for t<sub>OE</sub> and t<sub>OD</sub> testing.
7. Typical values and capacitance are measured at V<sub>CC</sub>=5.0V and T<sub>a</sub> = 25°C.
8. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
9. I/O pins are open (no load).
10. V<sub>in</sub> specified is not for program/verify operation. Contact AMI for information regarding PEEL program/verify specifications.
11. t<sub>OD</sub> and t<sub>OE</sub> are measured at V<sub>oh</sub>=-0.1V and V<sub>ol</sub>=+0.1V.
12. Contact factory for increased Iol requirements.

**Figure 42: PEEL273 AC Switching Waveforms**



**Figure 43: PEEL273 AC Test Loads**

