

## SERIAL I/O REAL TIME CLOCK

**■ GENERAL DESCRIPTION**

The NJU6355 series is a serial I/O Real Time Clock suitable for 4 bits microprocessor.

It contains quartz crystal oscillator, counter, shift register, voltage regulator, voltage detector and interface controller.

The NJU6355 required only 4-port of microprocessor for data transfer, and the microprocessor can receive the data at any time when the microprocessor requires.

The operating voltage is as wide as 2.0V to 5.5V, consequently, the NJU6355 can count accurate time data even if the back up period.

Furthermore, the long time back up is available as the current consumption during the back up period is less than  $3\mu A$ .

**■ PACKAGE OUTLINE**

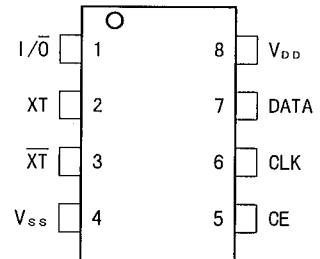

NJU6355XD



NJU6355xE

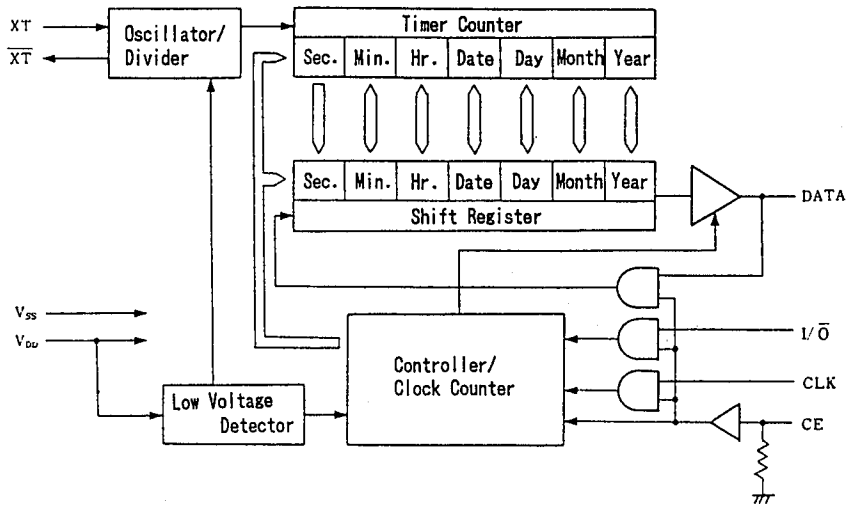
**■ FEATURES**

- Operating Voltage : 2.0 ~ 5.5V
- Low operating current : 3  $\mu A$  (Typ.) at 3.0V  
4  $\mu A$  (Typ.) at 5.0V
- BCD Counts of Seconds, Minutes, Hours, Date,  
Days of Week, Month and Year
- Required only 4-port (DATA, CLK, CE and I/O)
- Low Battery Detector (Low voltage alarm signal output)
- Automatic Leap Year Compensation
- Package Outline --- DIP 8/DMP 8
- C-MOS Technology

**■ PIN CONFIGURATION**

**■ LINE UP**

VERSION	O U T P U T D A T A	OSC. CAPACITOR
6355 E	Seconds, Minutes, Hours, Days of Week, Date, Month, Year	$C_s/C_d$ on chip
F	Seconds, Minutes, Hours, Days of Week	$C_s/C_d$ on chip
G	Seconds, Minutes, Hours, Days of Week, Date, Month, Year	$C_d$ on chip
H	Seconds, Minutes, Hours, Days of Week	$C_d$ on chip

## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N															
1	$I/\bar{O}$	Input/Output Select Terminal for DATA Terminal "H": Input, "L": Output During the CE terminal is "L", the Data terminal is high impedance.															
2	XT	Quartz Crystal Connecting Terminal (f=32.768kHz)															
3	$\bar{X}T$	Refer to the Line-Up Table for internal Gg, Cd value.															
5	CE	Chip Enable Input Terminal (with pull-down resistance) "H": Data Input/Output is available "L": Data terminal is high impedance When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L".															
6	CLK	Clock Input Terminal The Data Input/Output is synchronized by this clock. When the CE terminal is "L" the data terminal is high impedance.															
7	DATA	Serial Timer Data Input/Output <table border="1" style="margin-left: 20px;"> <thead> <tr> <th><math>I/\bar{O}</math></th> <th>CE</th> <th>DATA Terminal</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>Input</td> </tr> <tr> <td>L</td> <td>H</td> <td>Output</td> </tr> <tr> <td>H</td> <td>L</td> <td>High-Impedance</td> </tr> <tr> <td>L</td> <td>L</td> <td>High-Impedance</td> </tr> </tbody> </table>	$I/\bar{O}$	CE	DATA Terminal	H	H	Input	L	H	Output	H	L	High-Impedance	L	L	High-Impedance
$I/\bar{O}$	CE	DATA Terminal															
H	H	Input															
L	H	Output															
H	L	High-Impedance															
L	L	High-Impedance															
8	$V_{DD}$	Power Supply (+5V)															
4	$V_{SS}$	GND															

**FUNCTIONAL DESCRIPTION**
**1. Timer Data structure**

The NJU6355 using BCD code which consisting of 4 bits per 1 digit.

The calendar function including the last date of each month and the leap year calculation is executed automatically.

The unused bit for the timer data is "0".

< Timer Data Bit Map >

	MSB				LSB				Range
Second	0	S6	S5	S4	S3	S2	S1	S0	0 - 59
Minute	0	m6	m5	m4	m3	m2	m1	m0	0 - 59
Hour	0	0	H5	H4	H3	H2	H1	H0	0 - 23
Days of Week					0	W2	W1	W0	1 - 7
Date	0	0	D5	D4	D3	D2	D1	D0	1 - 31
Month	0	0	0	M4	M3	M2	M1	M0	1 - 12
Year	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0 - 99

**2. Timer Data Reading**

When the  $I/\bar{O}$  terminal is "L" and the CE terminal is "H", timer data can read out. The output is LSB first and the output data strings (depending on the version) is shown below.

The timer data is transferred from timer counter to shift register at rising edge of the chip enable on the CE terminal, and output the LSB of the timer data from the Data terminal.

Afterward the timer data in the shift register shift by synchronized at the falling edge of clock signal on CLK terminal and output from the DATA terminal.

If the timer data is updated in the data output, there are one second difference between timer data and output data.

< E & G Version >

Year	Month	Date	Day	Hour	Minute	Second
------	-------	------	-----	------	--------	--------

The data is read out from LSB of Year, and first 52-bit is effective.

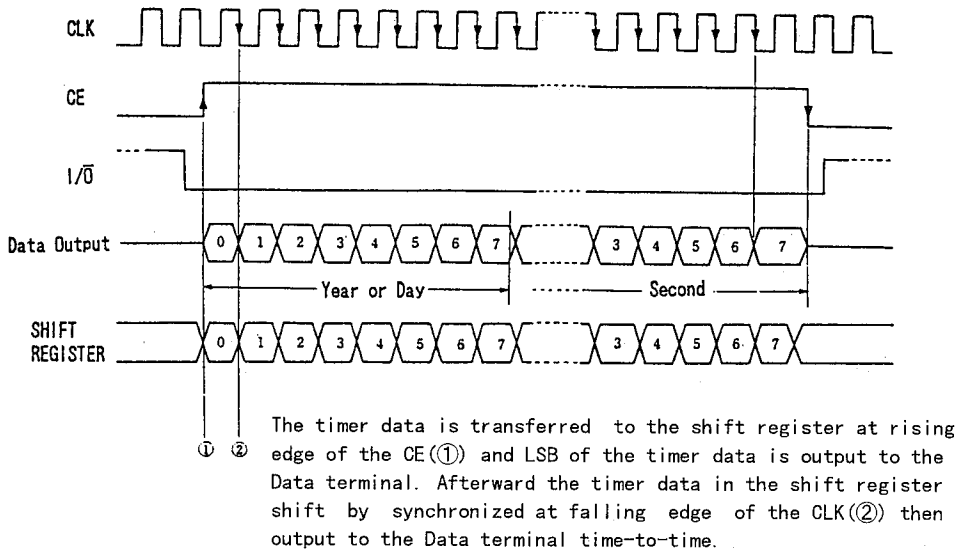
< F & H Version >

Day	Hour	Minute	Second
-----	------	--------	--------

The data is read out from LSB of Days of Week, and first 28-bit is effective.

If the low voltage detector detect the low battery,  $(EE)_H$  is written into each digit of timer data and read out. The code of  $(EE)_H$  is a warning for the data broken.

## &lt; Read-Out Timing &gt;



note ) When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L". And so, before the CE signal is raised, the I/O signal should be fixed to "L".

## 3. Timer Data Writing

When both of I/O terminal and CE terminal are "H", update is stopped. Oscillator divider is cleared, and the timer data can be written to the NJU6355. The timer data is written into the shift register from the Data terminal by synchronized with rising edge of the clock signal input from the CLK terminal, and the data is transferred from the shift register to the timer counter by synchronized with falling edge of the CE signal. In this time the second-counter is cleared to "0", and the oscillator divider start the operation. The input data strings are LSB first of each digit as shown below (the data format is depend on the version):

## &lt; E &amp; G Version &gt;

Year	Month	Date	Day	Hour	Minute
------	-------	------	-----	------	--------

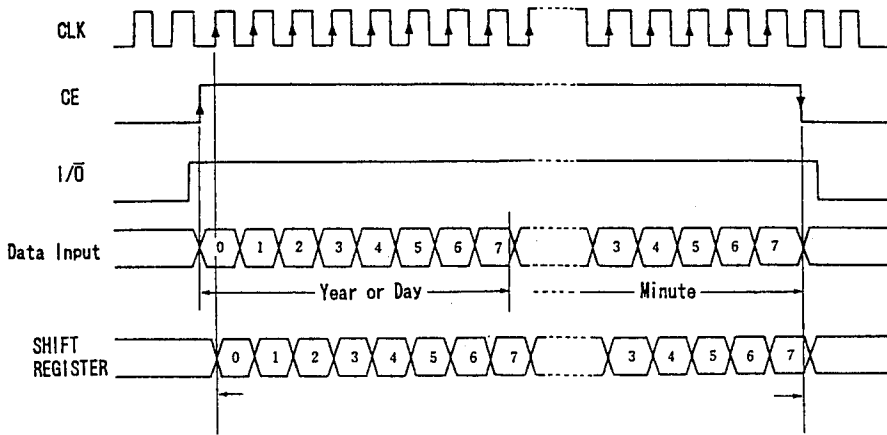
The data is written from LSB of Year and last 44-bit is effective.

## &lt; F &amp; H Version &gt;

Day	Hour	Minute
-----	------	--------

The data is written from LSB of Days of Week and last 20-bit is effective.

## &lt; Write-Down Timing &gt;



The data is input into the shift register at rising edge of the CLK.

The data in the shift register is transferred to the timer counter at this falling edge of the CE, then the oscillator divider start the operation.

note ) When the CE signal is which raising edge or falling edge, the CLK signal should be fixed to "L". And so, before the CE signal is raised, the I/O signal should be fixed to "H".

**4. Low Voltage Detector**

The NJU6355 series incorporate the low battery detector. If the supply voltage reduce to the detection level, (EE)<sub>H</sub> is written into each digit of the shift register as warning code for the CPU.

**5. Data Access**

The NJU6355 series can operate from 2.0V to 5.5V. However, it is not allow the data access out of the range of  $5V \pm 10\%$ . It may be broken the data unless  $5V \pm 10\%$ .

Thus, when the data access, CE terminal should be "H" after the power supply rise to  $5V \pm 10\%$ , then start the operation.

**■ ABSOLUTE MAXIMUM RATINGS**

( Ta=25°C )

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sub>DD</sub>	- 0.3 ~ + 6.0	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	250 (DIP) 200 (DMP)	mW
Operating Temperature	T <sub>OPR</sub>	- 30 ~ + 80	°C
Storage Temperature	T <sub>STG</sub>	- 55 ~ +150	°C

**■ ELECTRICAL CHARACTERISTICS**

## DC Characteristics

 (  $V_{DD}=2.0V$ ,  $T_a=25^\circ C$  )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	$I_{DD}$	XT=32.768kHz, CE=0V		3.0	4.0	$\mu A$
LowBattery Detect Voltage	$V_{DET}$		1.1		1.7	V

## DC Characteristics

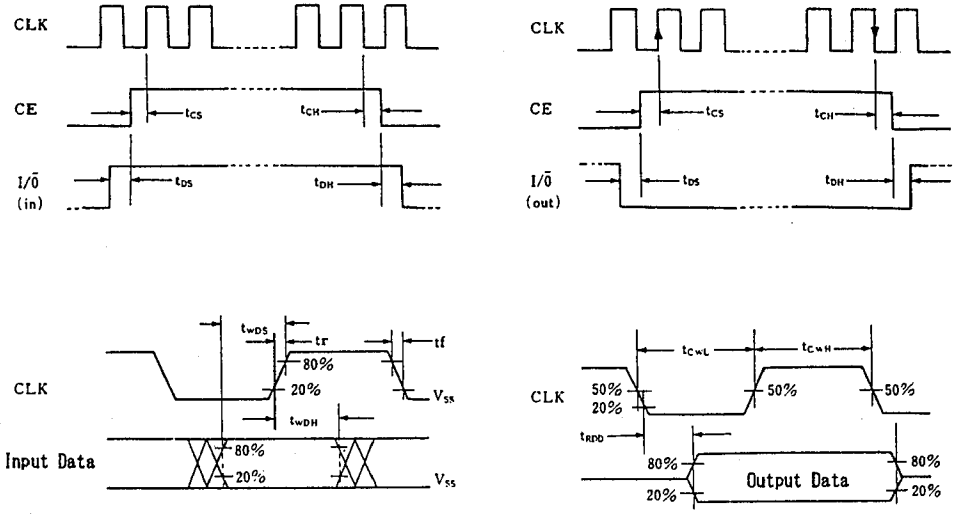
 (  $V_{DD}=5.0V \pm 10\%$ ,  $T_a=25^\circ C$  )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	$V_{DD}$		4.5		5.5	V
Operating Current	$I_{DD}$	XT=32.768kHz, CE=0V		4.0	15	$\mu A$
3-st Leakage Current	$I_{TSL}$	DATA Terminal (CE=0V)	-2.0		2.0	$\mu A$
Input Leakage Current	$I_{IL}$	$I/\bar{O}$ , CLK Terminals	-1.0		1.0	$\mu A$
Input Current	$I_{CE}$	CE Terminal (CE= $V_{DD}$ )			20	$\mu A$
Input Voltage	$V_{IH}$	$I/\bar{O}$ , CE, CLK, DATA Terminals	$V_{DD} \times 0.8$		$V_{DD}$	V
	$V_{IL}$	$I/\bar{O}$ , CE, CLK, DATA Terminals	$V_{SS}$		$V_{DD} \times 0.2$	
Output Voltage	$V_{OH}$	DATA Terminal ( $I_{OH}=-0.4mA$ )	4.1			V
	$V_{OL}$	DATA Terminal ( $I_{OL}=1.0mA$ )			0.4	

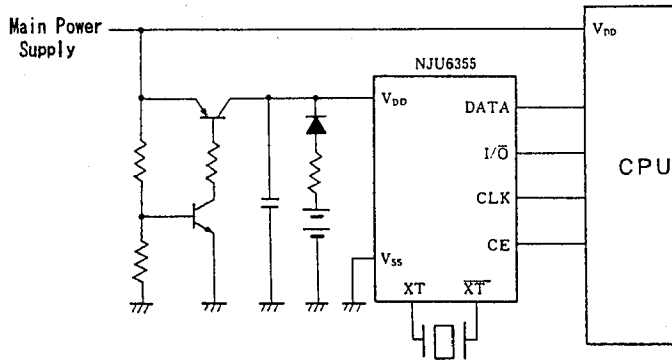
## AC CHARACTERISTICS

 (  $V_{DD}=5.0V \pm 10\%$ ,  $T_a=25^\circ C$ ,  $C_L=50pF$  )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CLK Pulse "H" Period	$t_{CWH}$		0.47		5000	$\mu s$
CLK Pulse "L" Period	$t_{CWL}$		0.47		5000	$\mu s$
CE Set-up Time Before CLK Rising	$t_{CS}$		470			ns
CE Hold Time After CLK Falling	$t_{CH}$		20			ns
$I/\bar{O}$ Set-up Time Before CLK Rising	$t_{DS}$		60			ns
$I/\bar{O}$ Hold Time After CLK Falling	$t_{DH}$		20			ns
Write-Down Data Set-Up Time	$t_{WDS}$		100			ns
Write-Down Data Hold Time	$t_{WDH}$		20			ns
Data Delay Time After CLK Falling	$t_{RDD}$				200	ns
Rise/Fall Time	$t_{RF}$				50	ns



■ APPLICATION CIRCUIT



11

# NJU6355 Series

---

MEMO

**[CAUTION]**

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.