D2421, REVISED APRIL 1985

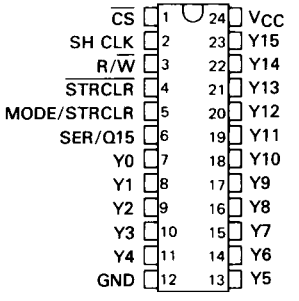
'LS673

- **16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register**
- **Performs Serial-to-Parallel Conversion**

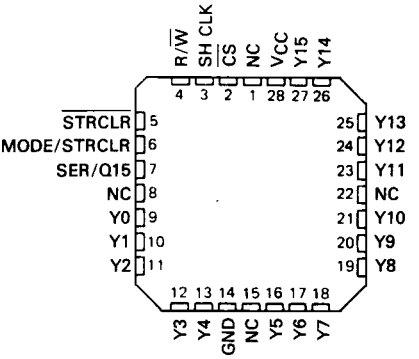
'LS674

- **16-Bit Parallel-In, Serial-Out Shift Register**
- **Performs Parallel-to-Serial Conversion**

SN54LS673 . . . J OR W PACKAGE
SN74LS673 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS673 . . . FK PACKAGE
SN74LS673 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level ($\overline{CS}$) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

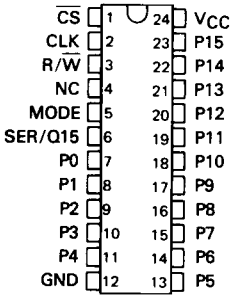
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

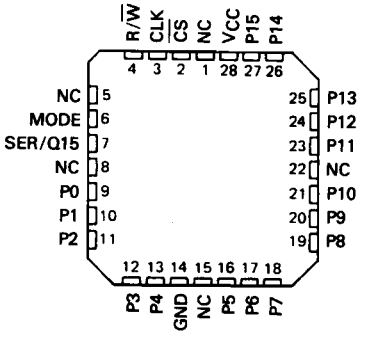
1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . FK PACKAGE
SN74LS674 . . . FN PACKAGE
(TOP VIEW)



'LS673

FUNCTION TABLE

INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/$\overline{W}$	SH CLK	$\overline{STRCLR}$	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

'LS674 FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

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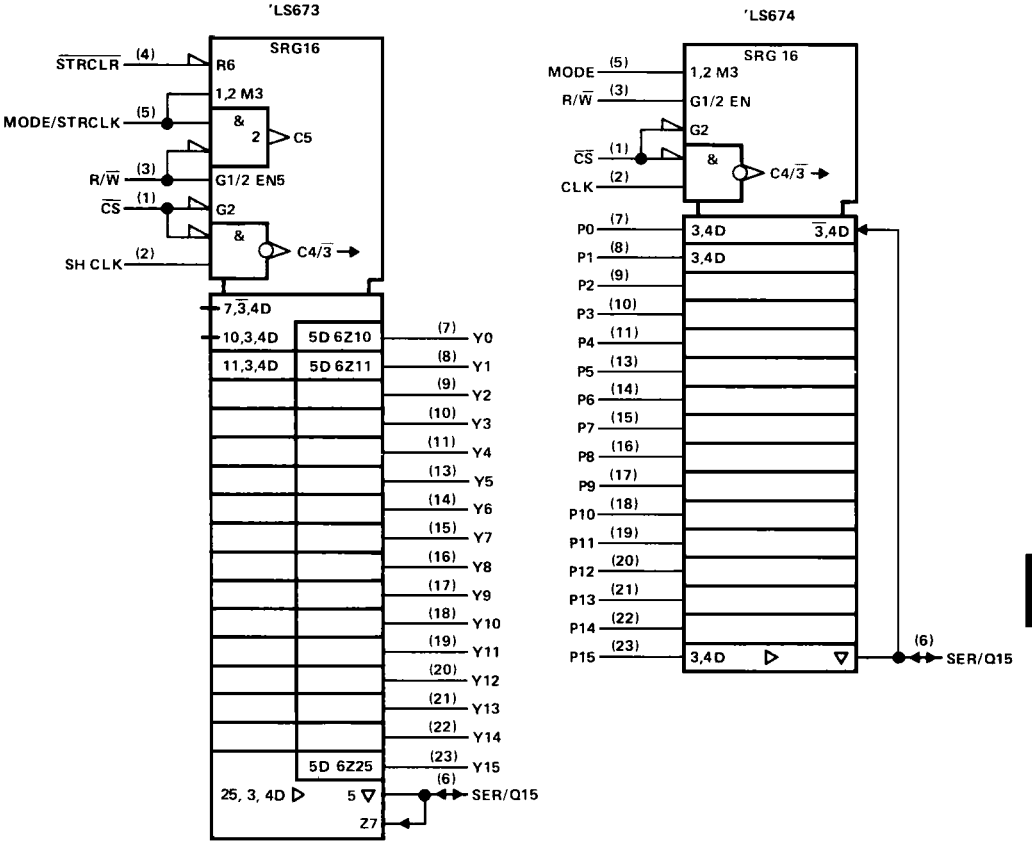
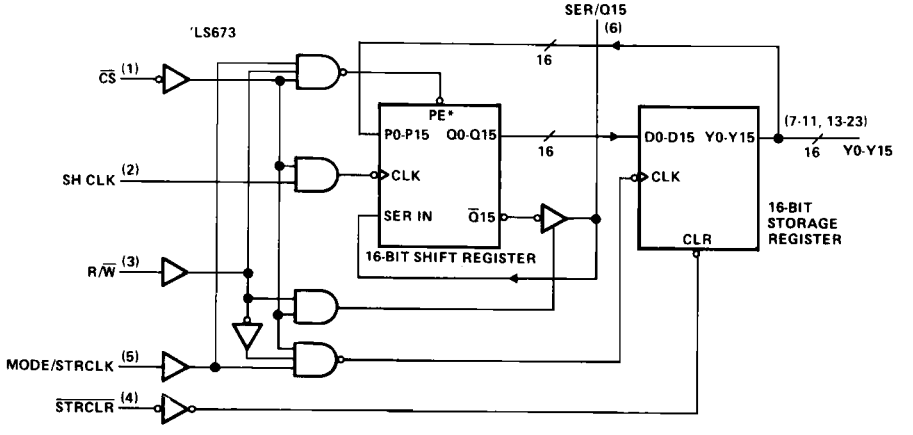
logic symbols



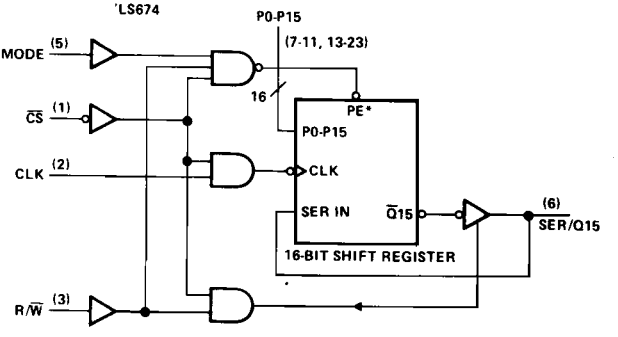
Pin numbers shown on logic notation are for DW, J or N packages.

functional block diagrams

SN54LS673, SN74LS673



SN54LS674, SN74LS674



*When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.
Pin numbers shown on logic notation are for DW, J or N packages.

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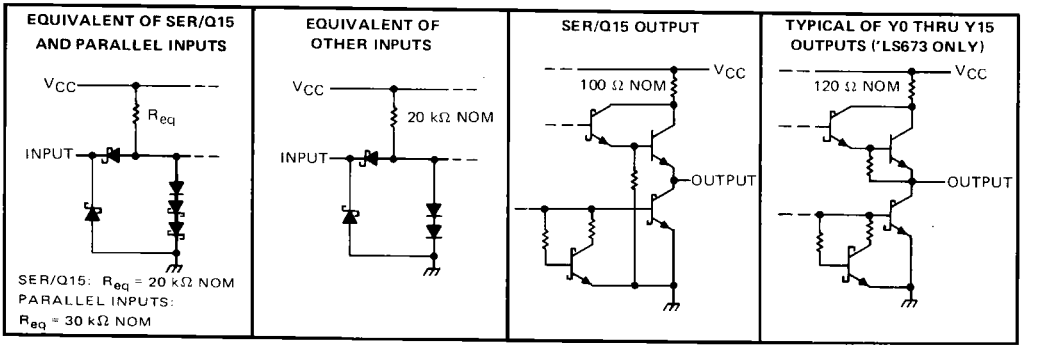
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: SER/Q15 . . . . . 5.5 V
All others . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674 . . . . . −55°C to 125°C
SN74LS673, SN74LS674 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	SER/Q15				−1			−2.6	mA
		Y0 thru Y15				−0.4			−0.4	
I_{OL}	Low-level output current	SER/Q15				12			24	mA
		Y0 thru Y15				4			8	
f_{clock}	Clock frequency			0		20	0		20	MHz
$t_{w(clock)}$	Width of clock input pulse			20			20			ns
$t_{w(clear)}$	Width of clear input pulse			20			20			ns
t_{su}	Setup time	SER/Q15		20			20			ns
		P0 thru P15		20			20			
		Mode		35			35			
		R/$\overline{W}$, $\overline{CS}$		35			35			
		SH CLK ↓ to Mode/STR CLK ↑ See Note 2		25			25			
t_h	Hold time	SER/Q15		0			0			ns
		P0 thru P15	'LS673	0			0			
			'LS674	5.0			5.0			
		Mode		0			0			
T_A	Operating free-air temperature			−55		125	0		70	°C

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.

3 TTL DEVICES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	SER/Q15	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Y0 thru Y15¶	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	SER/Q15	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Y0 thru Y15¶		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 0.4 V			−0.4			−0.4	mA
I_I	Input current at maximum input voltage	SER/Q15	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	SER/Q15	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Others					20			20	
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	SER/Q15	V_{CC} = MAX		−30		−130	−30		−130	mA
		Y0 thru Y15¶			−20		−100	−20		−100	
I_{CC}	Supply current	'LS673	V_{CC} = MAX			50	80		52	80	mA
		'LS674				25	40		25	40	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
¶'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673 FROM	'LS673 TO	'LS674 FROM	'LS674 TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF	20	28		MHz
t_{PHL}	$\overline{STRCLR}$	Y0 thru Y15			R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PLH}	MODE/ STRCLK	Y0 thru Y15					28	45	
t_{PHL}							30	45	
t_{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF		21	33	ns
t_{PHL}							26	40	
t_{PZH}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 45 pF		30	45	ns
t_{PZL}							30	45	
t_{PHZ}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 5 pF		25	40	ns
t_{PLZ}							25	40	

NOTE 2: See General Information Section for load circuits and voltage waveforms.
f_{max} = maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from low level
t_{PLZ} = Output disable time from high level

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