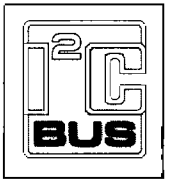
Data sheet	
status	Product specification
date of issue	July 1990

SAA7192

Digital colour space converter



INTRODUCTION

The Digital Color Space Converter (DCSC) is a matrix which is used to transform 8-bit digital input signals, i.e. Y (luminance), Cr (colour, R-Y) and Cb (colour, B-Y), into an RGB 8-bit format in accordance with the CCIR-601 recommendations.
The system accepts the formats of the DMSD2 family of decoders at the input. The maximum data rate is 16 MHz. The propagation delay of the device is constant. A matched pipeline delay line is available to enable the HREF signal to be synchronized with the video data at the output.

SYSTEM FUNCTIONS

The DCSC consists of the following functional blocks, as illustrated in Fig.1:

- Input Formatter with;
  multiplexer
  Y-delay line
  Cr and Cb Interpolating filters
- Conversion matrix
- Video look up tables
- Pipeline delay line
- I²C-bus interface

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7192	68	PLCC	plastic	SOT188AA,AGA

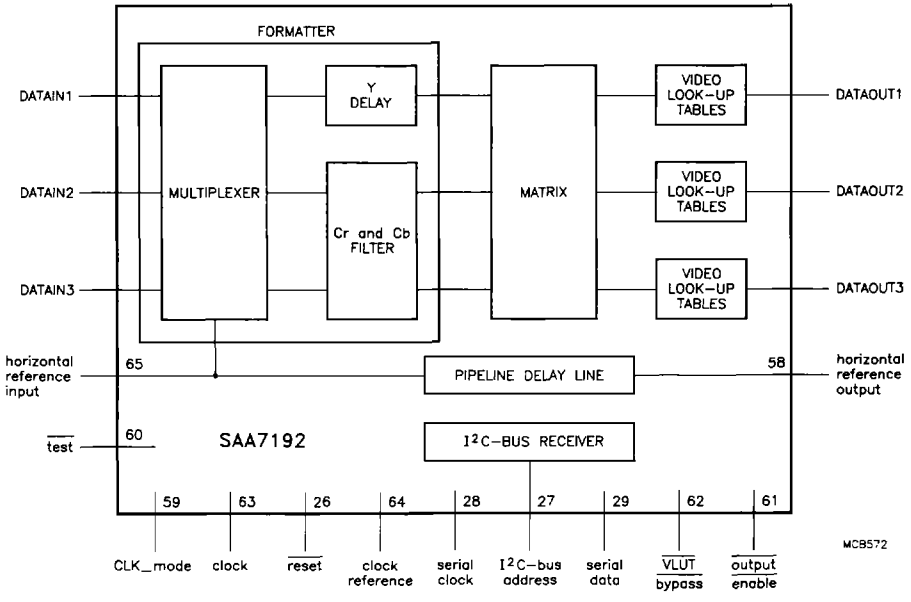


Fig.1 Block diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

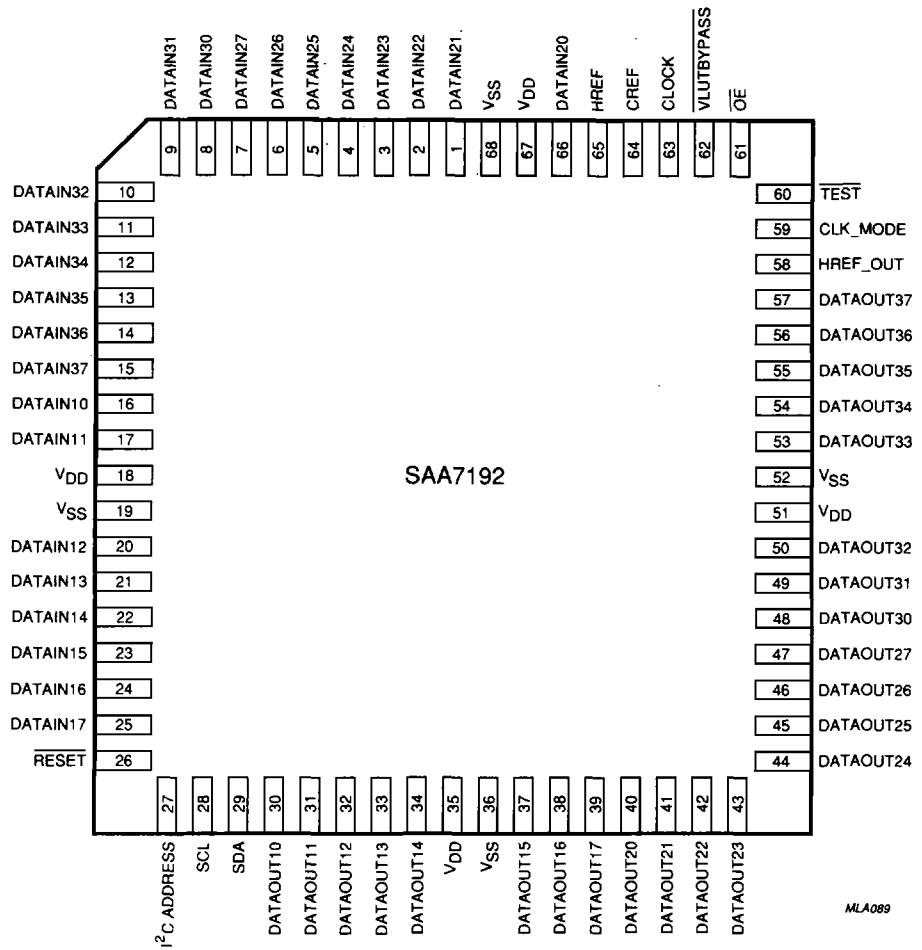


Fig.2 Pinning diagram.

Functional modes

Table 1 Functional Modes.

MODE	FUNCTION
1	4:1:1 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
2	4:1:1 filter, matrix, no VLUT; DATAOUT = RGB
3	4:1:1 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
4	4:1:1 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
5	4:2:2 filter, no matrix, no VLUT; DATAOUT = upsampled DATAIN
6	4:2:2 filter, matrix, no VLUT; DATAOUT = RGB
7	4:2:2 filter, no matrix, VLUT; DATAOUT = upsampled DATAIN multiplied by the factor loaded into the VLUT
8	4:2:2 filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT
9	no filter, no matrix, no VLUT; DATAOUT = DATAIN "Process Bypass"
10	no filter, matrix, no VLUT; DATAOUT = RGB
11	no filter, no matrix, VLUT; DATAOUT = DATAIN multiplied by the factor loaded into the VLUT.
12	no filter, matrix, VLUT; DATAOUT = RGB multiplied by the factor loaded into the VLUT

Figures 3 to 9b illustrate the various functional modes.

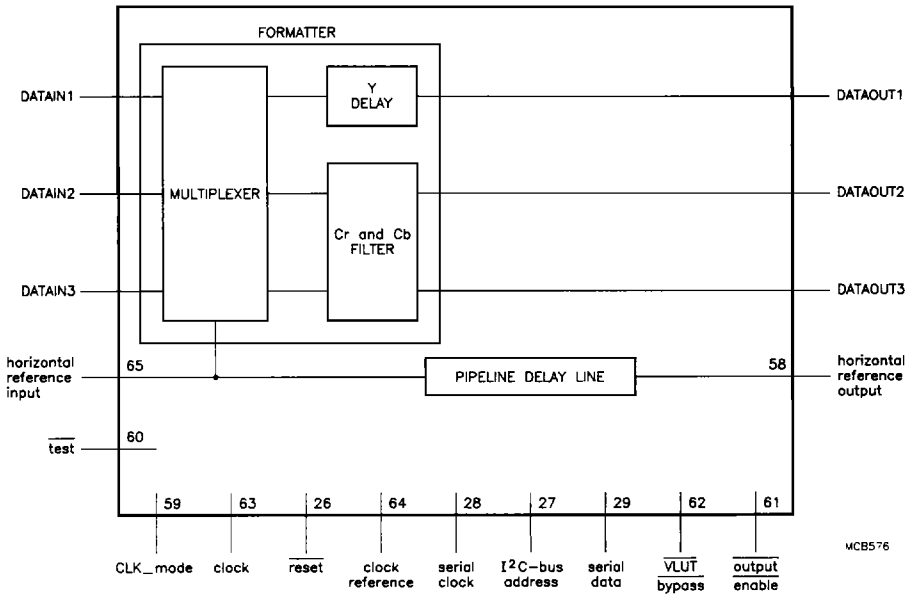


Fig.3 Functional mode 1 and 5.

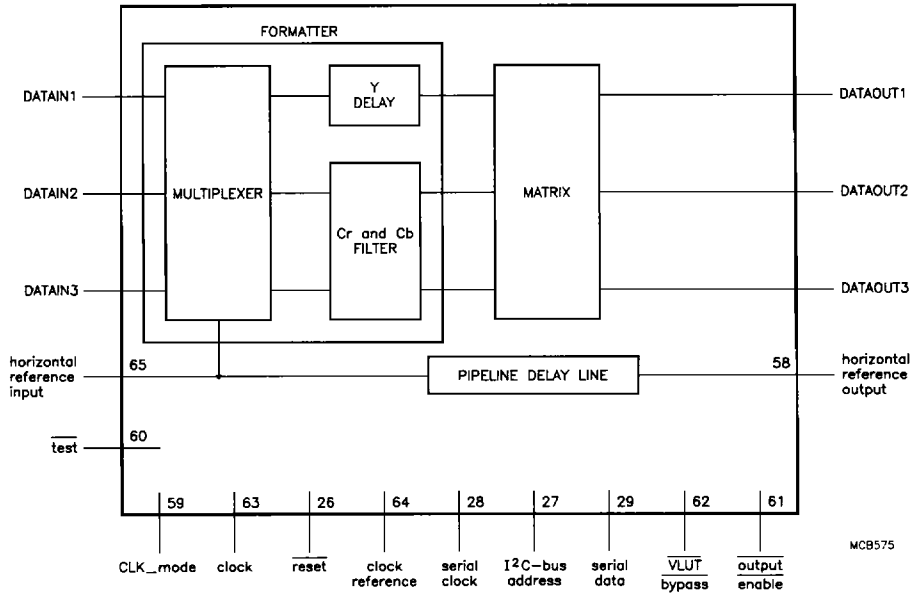


Fig.4 Functional mode 2 and 6.

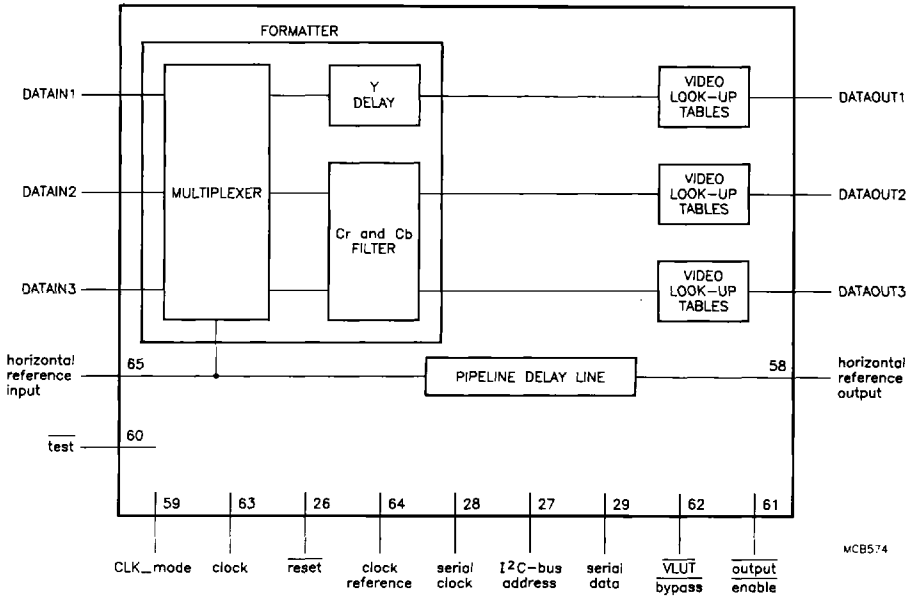


Fig.5 Functional mode 3 and 7.

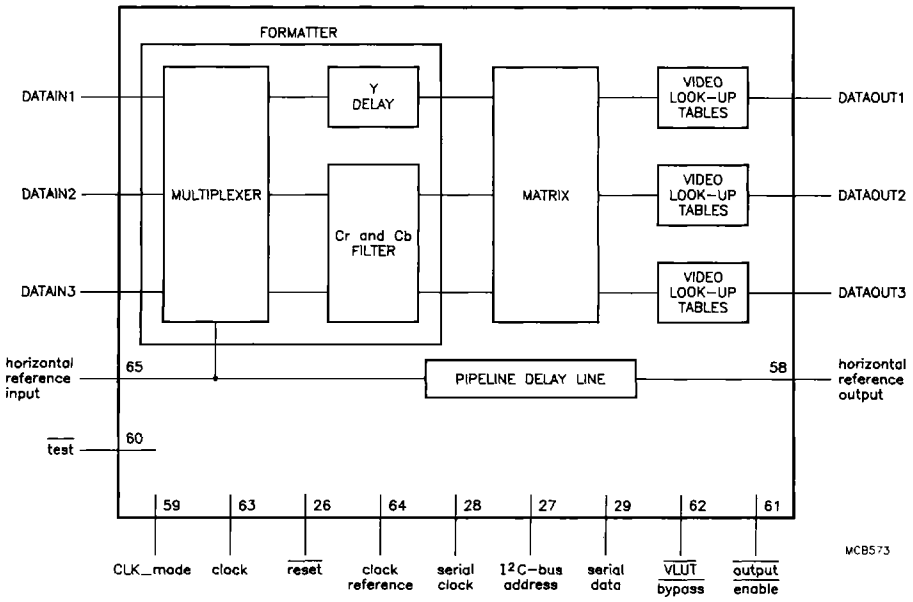


Fig.6 Functional mode 4 and 8.

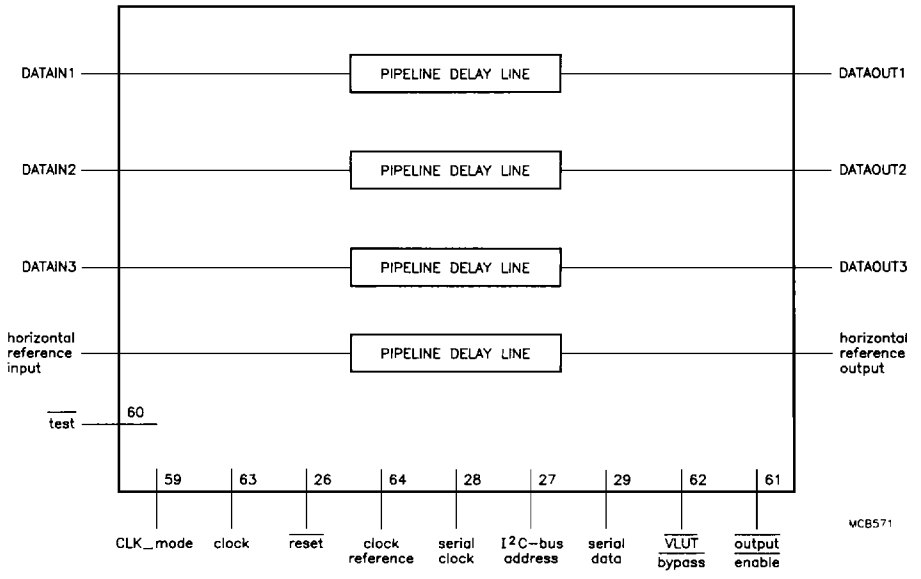


Fig.7 Functional mode 9.

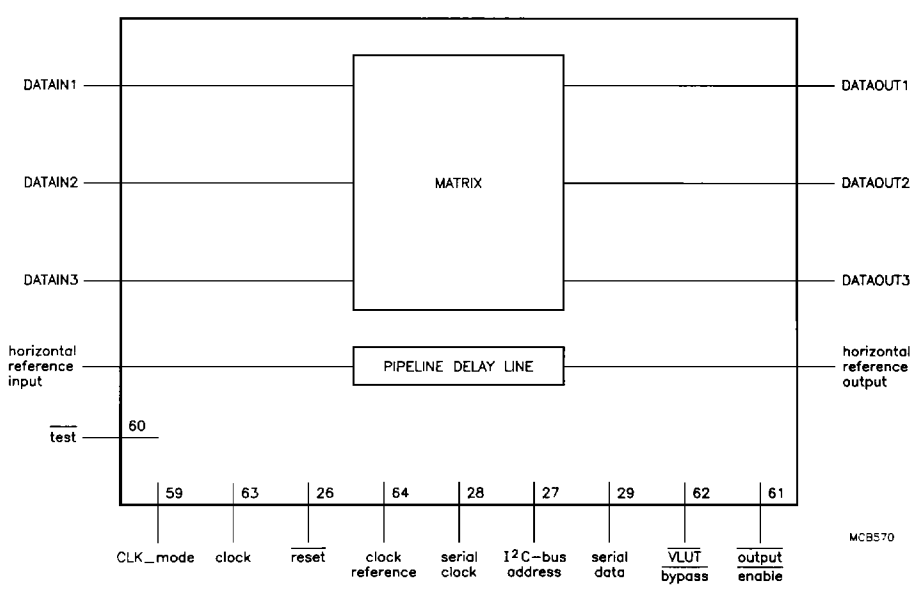


Fig.8 Functional mode 10.

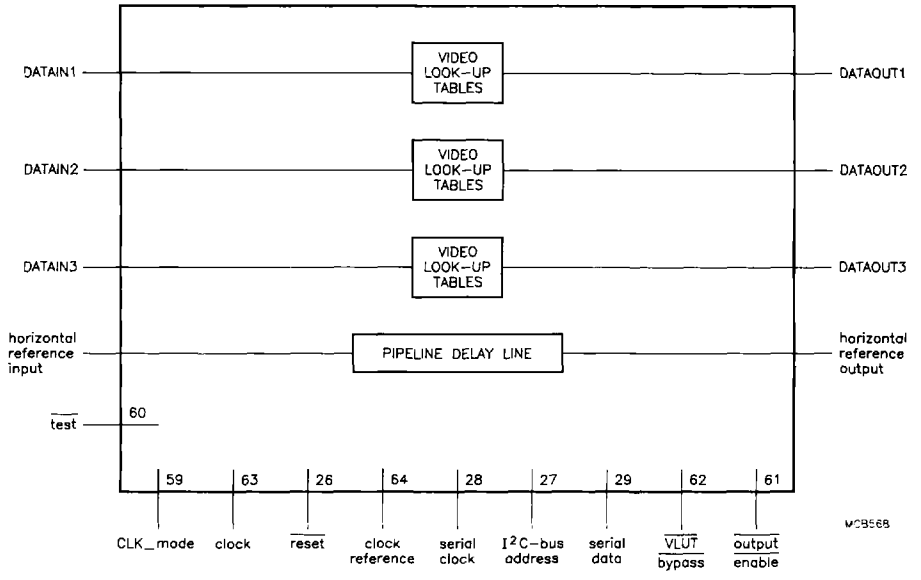


Fig.9a Functional mode 11.

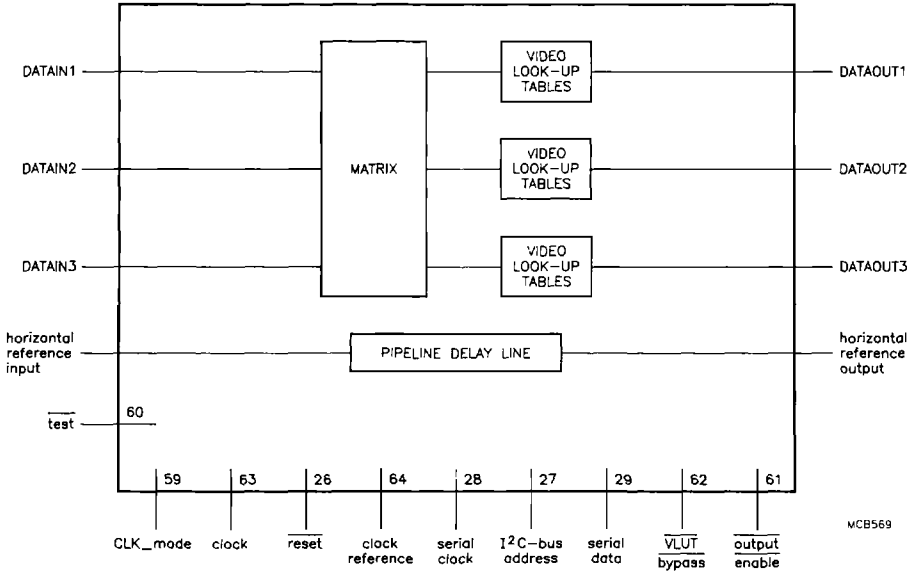


Fig.9b Functional mode 12.

Control facilities

After power-up all internal control signals of the device are at undefined values. The I²C-bus receiver must, therefore, be reset by using the external RESET signal. The control signals are then set to:

IICOE = 1
output in 3-state

FMTCNTRL = 4
format 4:4:4

$\overline{\text{MATBYPASS}}$ = 0
matrix bypassed

$\overline{\text{VLUTLOAD}}$ = 1
VLUT at READ operation

$\overline{\text{INRESET}}$ = 0
input data set to fixed values

Table 2 Input formats and functional modes

FMTCNTRL	$\overline{\text{MATBYPASS}}$	$\overline{\text{VLUTBYPASS}}$	FUNCTIONS
0	0	0	mode 1, input format 1 (DMSD2 format)
0	1	0	mode 2, input format 1 (DMSD2 format)
1	0	0	mode 1, input format 2
1	1	0	mode 2, input format 2
2	0	0	mode 5, input format 3 (DMSD2 format)
2	1	0	mode 6, input format 3 (DMSD2 format)
3	0	0	mode 5, input format 4 (parallel IN)
3	1	0	mode 6, input format 4 (parallel IN)
4	0	0	mode 9, input format 5 (parallel IN)
4	1	0	mode 10, input format 5 (parallel IN)
x	x	1	each of the above described modes will be multiplied by the factor loaded into the VLUT.

Note

The modes are given in Table 1.

The other control signals are:

$\overline{\text{VLUTLOAD}}$ = logic 1: VLOAD inactive
= logic 0: VLOAD datalines active to load VLUT

$\overline{\text{INRESET}}$ = logic 1: input latches at the formatter are always transparent
= logic 0: at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr and Cb to 128; if HREF = 0)

CLK_MODE = logic 1: DMSD mode (LL27 clock of DMSD feeds the DCSC)
= logic 0: DCSC is fed by a maximum 16 MHz clock without CREF signal.

Table 3 Output enable control

IICOE	$\overline{OE}$	CONTROL LINE TO DRIVER STAGES
0	X	1 = DATAOUT in high impedance mode
1	1	1 = DATAOUT in high impedance mode
1	0	0 = DATAOUT working

Note

IICOE: output enable control of I^2C-bus (enables $\overline{OE}$)
$\overline{OE}$: output enable (fast switch)

SYSTEM I/O INTERFACES

Input signals

VIDEO DATA (DATAIN)

Table 4 Format 1 (4:1:1, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal, 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black, quantization level 16 100 IRE; white, quantization level 235
DATAIN3 - U, V	multiplexed colour difference signals 4-bit; corresponds to UV7 to UV4 of DMSD2
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 5 Timing of Format 1; pin (DATAIN) and bit (U,V) numbers are indicated except clock

Y; 7 to 0	Y	Y	Y	Y	Y	Y	Y
DATAIN2, 7	U7	U5	U3	U1	U7	U5	U3
DATAIN2, 6	U6	U4	U2	U0	U6	U4	U2
DATAIN2, 5	V7	V5	V3	V1	V7	V5	V3
DATAIN2, 4	V6	V4	V2	V0	V6	V4	V2
Clock A	1	2	3	4	5	6	7

Table 6 Format 2 (4:1:1, semi-parallel, customized format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals,8-bit
Sampling frequency	1/4 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 7 Timing of Format 2; the indexes show the clock (sample) number

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0		Cr0		Cb4		Cr4
Clock A	0	1	2	3	4	5	6

Table 8 Format 3 (4:2:2, semi-parallel, DMSD2 format)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cr, Cb	multiplexed colour difference signals corresponds to UV7 to UV0 of DMSD2
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128
DATAIN2	not used

Table 9 Timing of Format 3

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cr, Cb	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4	Cb6
Clock A	0	1	2	3	4	5	6

Table 10 Format 4 (4:2:2, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	12 to 16 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128b
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	1/2 of the Y signal
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 11 Timing of Format 4

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0		Cb2		Cb4		Cb6
Cr	Cr0		Cr2		Cr4		Cr6
Clock A	0	1	2	3	4	5	6

Table 12 Format 5 (4:4:4, Y-Cr-Cb, parallel)

DATAIN1 - Y	luminance signal; 8-bit
Sampling frequency	maximum 16.0 MHz
Level	0 IRE; black; quantization level 16 100 IRE; white; quantization level 235
DATAIN2 - Cr	colour difference signal R-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless, binary 128
DATAIN3 - Cb	colour difference signal B-Y, 8-bit
Sampling frequency	maximum 16.0 MHz
Level	bottom peak; quantization level 16 top peak; quantization level 240 colourless; quantization level 128

Table 13 Timing of Format 5

Y	Y0	Y1	Y2	Y3	Y4	Y5	Y6
Cb	Cb0	Cb1	Cb2	Cb3	Cb4	Cb5	Cb6
Cr	Cr0	Cr1	Cr2	Cr3	Cr4	Cr5	Cr6
Clock A	0	1	2	3	4	5	6

CONTROL DATA

Clock

The line locked clock LL27 (denoted as CLOCK at the DCSC input) is twice the data rate of that specified for the DMSD2 family of decoders. The data rate is denoted as CLOCK_A in Tables 5, 7, 9, 11 and 13.

The data rate on the input (DATAIN) is as follows;

12.2727 MHz; 60 Hz signals (from SAA7191)
13.5 MHz; CCIR signals (from SAA7151)
14.75 MHz; 50 Hz signals (from SAA7191)
16.0 MHz; maximum frequency

Timing reference (Fig. 10)

The timing reference signal from the SAA7151/7191 is used to synchronize the multiplexer and refers to the LL27 clock. Each alternative positive slope, marked by a CREF signal, is used to obtain data. The horizontal reference signal, HREF, indicates the active part of a line and also synchronizes the multiplexer.

CREF The clock reference signal is a clock qualifier signal distributed by the clock generator of the DMSD system. The frequency is identical to the sample rates denoted in the input and the output formats (see Video data and Operating conditions).

HREF Horizontal reference signal is the line reference signal of the YUV-bus. A positive slope marks the beginning of the active part of a line. The length of the active part corresponds to the number of samples (see Operating conditions).

Table 14 Real-time control signals

$\overline{OE}$	= 1 : = 0 :	switches the output to high-z mode output enable, output stage in use
$\overline{VLUTBYPASS}$	= 1 : = 0 :	VLUT's in use VLUT's bypassed
$\overline{RESET}$	= 1 : = 0 :	device in use general reset
CLK_MODE	= 1 : = 0 :	DMSD mode (LL27 clock of DMSD feeds the DCSC) DCSC is feed by a clock signal with a maximum data rate of 16 MHz (without CREF signal).

Table 15 I^2C-bus controls

FMTCNTRL	= 0 : = 1 : = 2 : = 3 : = 4 : = 5 : = 6 : = 7 :	4:1:1 format, DMSD2 format 4:1:1 format, customized format 4:2:2 format, from DMSD2 4:2:2 format, parallel 4:4:4 format, parallel not used not used not used
$\overline{MATBYPASS}$	= 1 : = 0 :	matrix in use matrix bypassed
$\overline{VLUTLOAD}$	= 1 : = 0 :	VLOAD inactive VLOAD data lines active to load VLUT
VLUTDATA	:	load VLUT's via I^2C-bus (256 x 8-bit)
$\overline{INRESET}$	= 1 : = 0 :	input latches at the formatter are always transparent at the end of each active video line the input latches have to be set to fixed values (Y to 16; Cr, Cb to 128; if HREF = 0)
IICOE	= 1 : = 0 :	$\overline{OE}$ enabled switches the output to high impedance mode

Output signals

VIDEO DATA

$\overline{OE}$ (output enable, fast switch, active LOW) and IICOE (I^2C output enable, active HIGH) switchs the DATAOUT lines when in the high-impedance mode (see Control facilities).

Table 16 Format of DATAOUT (RGB if matrix in use)

DATAOUT1 (0 to 7)	Red
DATAOUT2 (0 to 7)	Green
DATAOUT3 (0 to 7)	Blue
To all three DATAOUT lines:	
Sampling frequency	12 to 16 MHz
Level	0 IRE; quantization level 16 100 IRE; quantization level 235

AUXILIARY DATA

Pipelined external reference signal HREF_OUT (delayed HREF).

The delay line (wordlength 1-bit) has the same duration as the signal processing of the video data lines.

OPERATING CONDITIONS

Electrical Conditions

Start-up condition

No particular function except the external power-on-reset e.g. for I^2C-bus interface (RESET) is intended.

Operating time

As this device will be used in computers, it has been designed to operate continuously.

Temperature range

Refer to the characteristics.

Backup

No backup capability (standby) is provided internally.

Power down mode

No power-down capability is provided internally.

CHARACTERISTICS

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DD}	supply voltage range		4.5	5.5	V
Inputs					
V_{IL}	input voltage LOW (SDA, SCL)		−0.5	1.5	V
V_{IH}	input voltage HIGH (SDA, SCL)		3.0	V_{DD} +0.5	V
V_{IL}	input voltage LOW (any other)		−0.5	0.8	V
V_{IH}	input voltage HIGH (any other)		2.0	V_{DD} +0.5	V
I_{LI}	input leakage current		-	10	µA
C_I	input capacitance (clocks)		-	10	pF
C_I	input capacitance (data)		-	8	pF
Outputs					
V_{OH}	output voltage HIGH	note 1	2.4	V_{DD}	V
V_{OL}	output voltage LOW	note 1	0	0.6	V
C_L	output load capacitance (data and HREF)		15	40	pF
Timing					
t_{LL27}	cycle time	note 2	31	45	ns
k_{LL27}	duty factor		40	60	%
t_r	rise time		-	5	ns
t_f	fall time		-	6	ns
t_{CDL}	duty time LOW	note 3	26	-	ns
t_{CDH}	duty time HIGH		18	-	ns
t_{CS}	CREF set-up time		*	11	ns
t_{CH}	CREF hold time		*	3	ns
t_{HS}	HREF set-up time		*	11	ns
t_{HH}	HREF hold time		*	3	ns
$t_{SU;DAT}$	input data set-up time		11	-	ns
$t_{HD;DAT}$	input data hold time		3	-	ns
t_{OH}	ouput hold time		13	-	ns
$t_{OS;DAT}$	output data set-up time		14	-	ns
t_{SZ}	output disable time to 3-state		*	-	ns
t_{ZS}	output enable time from 3-state		*	-	ns

Note to the characteristics

1. The levels must be measured with the following load circuits; 0.6 kΩ to 3.0 V (2 TTL load); C_L = 40 pF.

2. DMSD-mode means that the DCSC will work in a DMSD environment. The CLOCK and the clock reference signal CREF is fed by the SCGC (SAA7157).

3. 16 MHz-mode means that the DCSC will work in any other environment. The CREF signal will be set to HIGH, the CLOCK signal can be any clock up to 16 MHZ.

* Value to be fixed

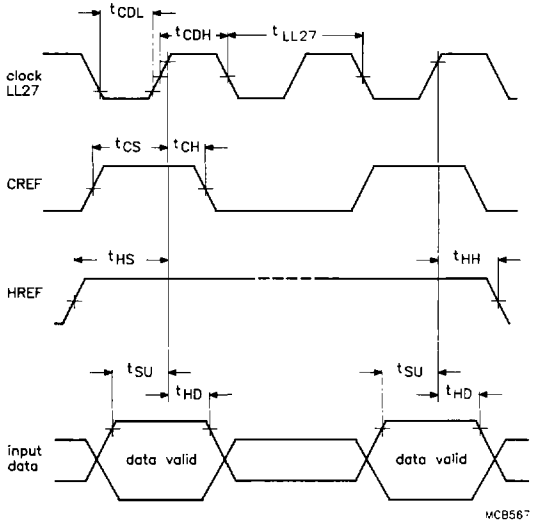


Fig.10 Input timing diagram.

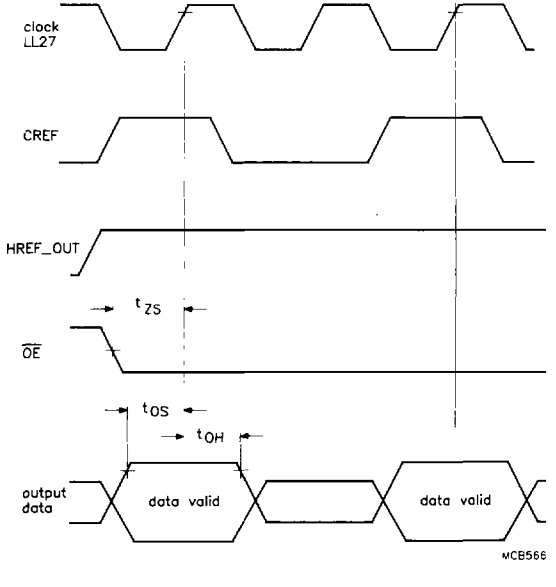


Fig.11 Output timing diagram.

Error condition

So as to inhibit unwanted operations, no information signal is available to the peripheral circuits. In the advent of an error the system has to be started again by applying the $\overline{\text{RESET}}$ signal.

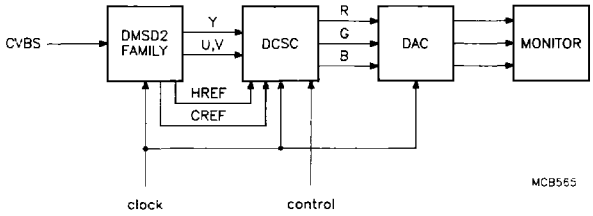


Fig.12 Application example.

SYSTEM BLOCK DESCRIPTION

INPUT FORMATTER

The formatter consist of five functional blocks;

- the multiplexer, which decodes the luminance and chrominance input signals
- the filter, which interpolates the samples of the incoming signal to get an upsampled data rate as at DATAIN1
- the luminance delay line;
- the timing control which creates the internal reference signals from the various inputs
- the bypass output multiplexer

Multiplexer

The data applied at DATAIN1 to DATAIN3 is converted as follows;

FIL1 : Y Luminance
FIL2 : Cb colour-difference signal B-Y
FIL3 : Cr colour-difference signal R-Y

The formats and data rates of DATAIN are described in 'Video data' (see tables 4 to 13).

The sampling frequency of the FIL data lines is 16 MHz maximum. The levels of the FIL data lines are the same as characterized for the DATAIN signals.

The timing reference signals CLOCK, HREF and CREF, for distinguishing the incoming data signals, are described in 'Control data'.

The signal FMTCNTRL is used to control the multiplexer and the filter.

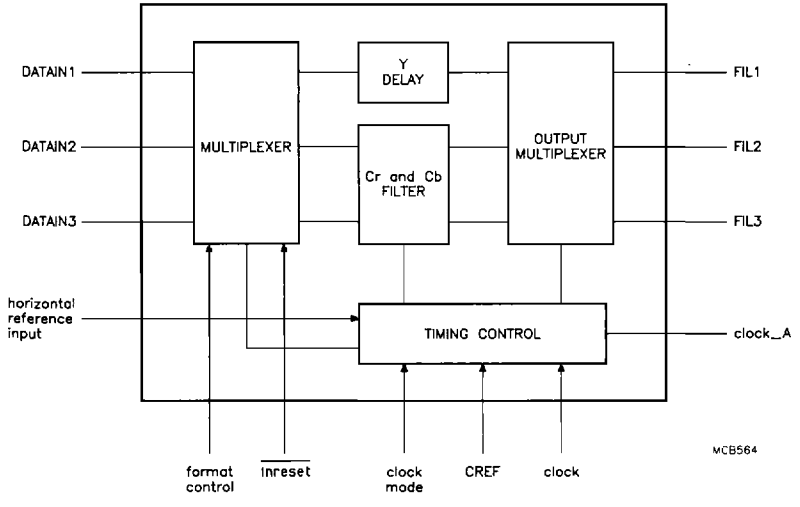


Fig.13 Input formatter.

FMTCNTRL = 0 : 4:1:1 format; DMSD2 format
= 1 : 4:1:1 format; customized format
= 2 : 4:2:2 format; from DMSD2
= 3 : 4:2:2 format; parallel
= 4 : 4:4:4 format; parallel
= 5 : not used
= 6 : not used
= 7 : not used

$\overline{\text{INRESET}}$ = 1 : input latches transparent
= 0 : input latches has to be set to fixed values (Y to 16, Cr, Cb to 128) if HREF = 0

CLK_MODE = 1 : DMSD mode (LL27 clock of DMSD feeds the DCSC)
= 0 : DCSC is feed by a clock of maximum 16 MHz without CREF signal.

Timing control

The timing control unit generates the required control signals from the incoming reference signals and the internally used CLOCK_A.

Filter and delay line

In the various functional modes the signal FMTCNTRL switches in the required filters (FMTCNTRL is described in 'Control data'). In all modes the same propagation delay will be realized, (the reference is Cb0).

DELAY LINE (LUMINANCE-DELAY)

At all frequencies and in all formats, there is a delay line to compensate for the delay of the signal processing time needed in the chrominance section.

CHROMINANCE FILTER

The filter for the Cr and Cb signal is realized in one filter design.

Format 1, 2 4:1:1

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. four times the colour signal. Figure 14 illustrates the frequency response of the chrominance section.

Format 3, 4 4:2:2

An interpolating filter is inserted to convert the original sampling frequency to the sampling frequency of the luminance signal i.e. twice the colour signal. Figure 15 illustrates the frequency response of the chrominance section.

Format 5 4:4:4

A bypass with a specified delay is inserted.

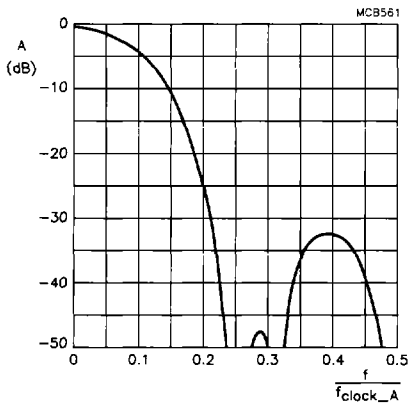


Fig.14 Frequency response of 4:1:1 filter.

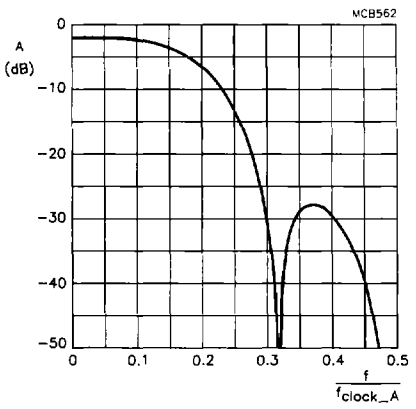


Fig.15 Frequency response of 4:2:2 filter

CONVERSIONAL MATRIX

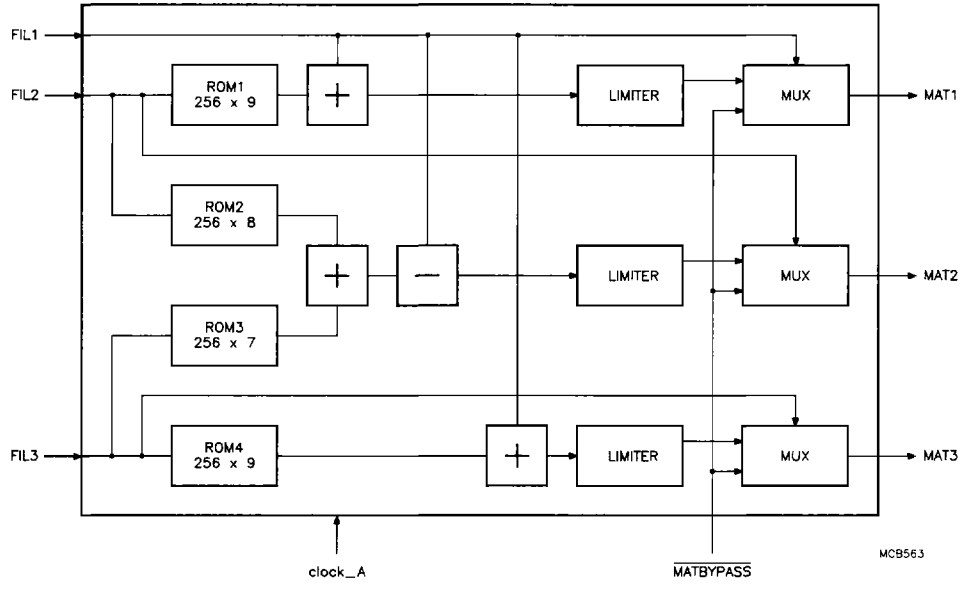


Fig.16 Block diagram MATRIX.

The properties of the conversion matrix are as follows:

- the conversion equations are (according to CCIR 601, with respect to the different quantisation on Y, Cb and Cr);

  Red = Y + 1.371 (Cr - 0.5)
  Green = Y - 0.698 (Cr - 0.5)
  - 0.336 (Cb - 0.5)
  Blue = Y + 1.732 (Cb - 0.5)

- the accuracy of the signal processing is within ± 0.5% of the accuracy of a theoretical conversion.

- the input and output data lines are 8-bit.

- $\overline{\text{MATBYPASS}}$ switches the matrix in bypass. The bypass has the same propagation delay as the matrix itself.

Input/Output Data

The levels are as follows:

FIL1 : luminance signal Y
: 0 IRE; black, quantization level 16
100 IRE; white, quantization level 235

FIL2 : multiplexed colour difference signals Cr
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

FIL3 : multiplexed colour difference signals Cb
: bottom peak; quantization level 16
: top peak; quantization level 240
: colourless; quantization level 128

The data rate on the input is maximum 16 MHz

The levels at the input and output, for some specific colour patterns, are given in Table 17.

CONTROL SIGNALS

$\overline{\text{MATBYPASS}}$ = 1 : matrix in use
= 0 : matrix bypassed

Functional description

Four ROMs are used to obtain the coefficients with the required accuracy.

In the advent of non-standard input levels the limiter reduces the possible data values at the output (red, green, blue channel) to values between 0 and 255. Consequently, all negative values are set to 0 and all values higher than 255 are set to 255.

Table 17 Levels at the functional blocks

test number	Y FIL1	CR FIL2	CB FIL3	MAT1 R	MAT2 G	MAT3 B
1 (white)	235	128	128	235	235	235
2 (black)	16	128	128	16	16	16
3 (red)	82	240	90	235	16	16
4 (green)	145	34	54	16	236	16
5 (blue)	41	110	240	16	16	235

VIDEO LOOK-UP TABLE AND OUTPUT STAGE

Functional description

The $\overline{\text{VLUTLOAD}}$ signal enables the memories to obtain data from the VLUTDATA signal via the I²C-bus (auto-increment mode). The three RAMs will also obtain the same data.

$\overline{\text{VLUTBYPASS}}$ will bypass the VLUT's in clock period time (real time switch).

In computer applications the VLUT is also known as Colour Look-Up Table (CLUT).

In the DCSC this table might be used to invert the Gamma-correction of a camera. This correction is applied to compensate for the non-linear relationship between the video voltage applied to the cathode and the light output of the phosphor of a CRT.
The Gamma-correction function (also known as Gradation) is given as;

$Y = X^{\gamma}$

The VLUT's are realized by 256 x 8-bit RAMs.

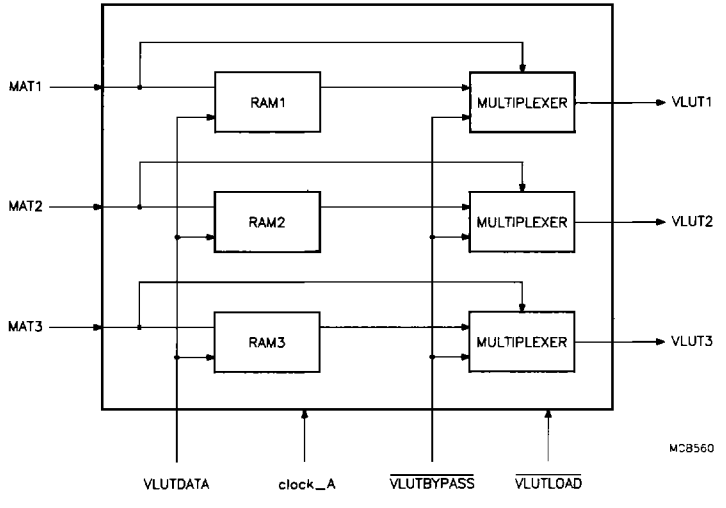


Fig.17 Block diagram video look up table.

I²C-bus receiver

Functional description

At switch-on all internal control signals are at undefined values and the I²C-bus receiver must, therefore, be reset by the external $\overline{\text{RESET}}$ signal. After reset the control signals will be set as follows:

IICOE	= logic 1	$\overline{\text{OE}}$ enabled
FMTCNTRL	= 4	format 4:4:4
$\overline{\text{MATBYPASS}}$	= logic 0	matrix bypassed
$\overline{\text{VLUTLOAD}}$	= logic 1	VLUT at read operation
$\overline{\text{INRESET}}$	= logic 0	input data set to fixed values

Receiver organisation

The address for the DCSC is as follows:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	1	0	0	0	X	0

write only

hardware programmable address bit

S	DCSC ADDRESS	A	SUB-ADDRESS	A	DATA BYTE	A	P

where S = start
A = acknowledge
P = stop

Table 18 Sub-address and data byte formats

HEX SUBADD	BINARY - DATA								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
00	X	X	X	X	X	0	0	0	input formatter to Format 1
00	X	X	X	X	X	0	0	1	input formatter to Format 2
00	X	X	X	X	X	0	1	0	input formatter to Format 3
00	X	X	X	X	X	0	1	1	input formatter to Format 4
00	X	X	X	X	X	1	0	0	input formatter to Format 5
00	X	X	X	X	0	X	X	X	matrix bypassed
00	X	X	X	X	1	X	X	X	matrix in use
00	X	X	X	0	X	X	X	X	input data at fixed values
00	X	X	X	1	X	X	X	X	input data to formatter
00	X	X	1	X	X	X	X	X	$\overline{OE}$ enabled
00	X	X	0	X	X	X	X	X	output stages 3-state
00	X	0	X	X	X	X	X	X	VLUT write enabled
00	X	1	X	X	X	X	X	X	VLUT read enabled
01	X	X	X	X	X	X	X	X	VLUTDATA

where;

D0 to D2 = FMTCONTROL
D3 = $\overline{MATBYPASS}$
D4 = $\overline{INRESET}$
D5 = IICOE
D6 = $\overline{VLUTLOAD}$
D7 = not used