HM514102C/CL Series

Preliminary

4,194,304-word × 1-bit Dynamic Random Access Memory

HITACHI

Rev. 0.0
Oct. 20, 1994

The Hitachi HM514102C/CL is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM514102C/CL has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514102C/CL offers Static Column Mode as a high speed access mode. Multiplexed address input permits the HM514102C/CL to be packaged in standard 300-mil 26-pin plastic SOJ and standard 400-mil 20-pin plastic ZIP.

Ordering Information

Type No.	Access time	Package
HM514102CS/CLS-7	70 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM514102CS/CLS-8	80 ns	
HM514102CZ/CLZ-7	70 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514102CZ/CLZ-8	80 ns	

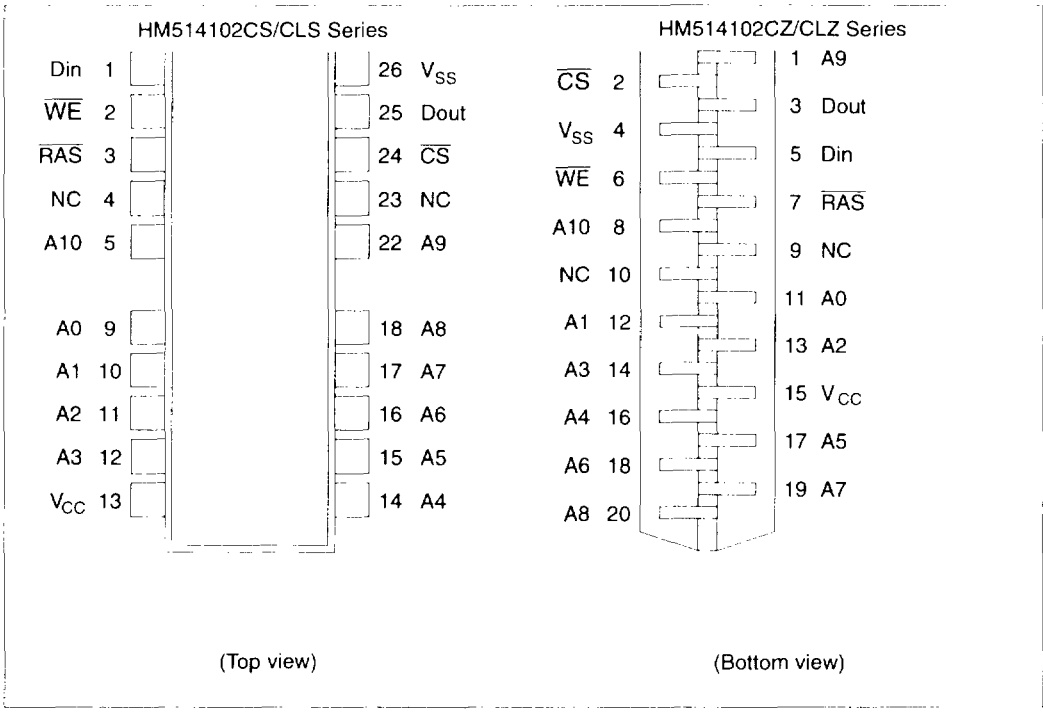
Features

- Single 5 V (±10%)
- High speed
  - Access time
    70 ns/80 ns (max)
- Low power dissipation
  - Active mode
    550 mW/495 mW (max)
  - Standby mode 11 mW (max)
    0.55 mW (max) (L-version)
- Static column mode capability
- 1,024 refresh cycles : 16 ms
  1,024 refresh cycles : 128 ms (L-version)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function
- Battery back up operation
  (L-version)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

ADE-203-296(Z)

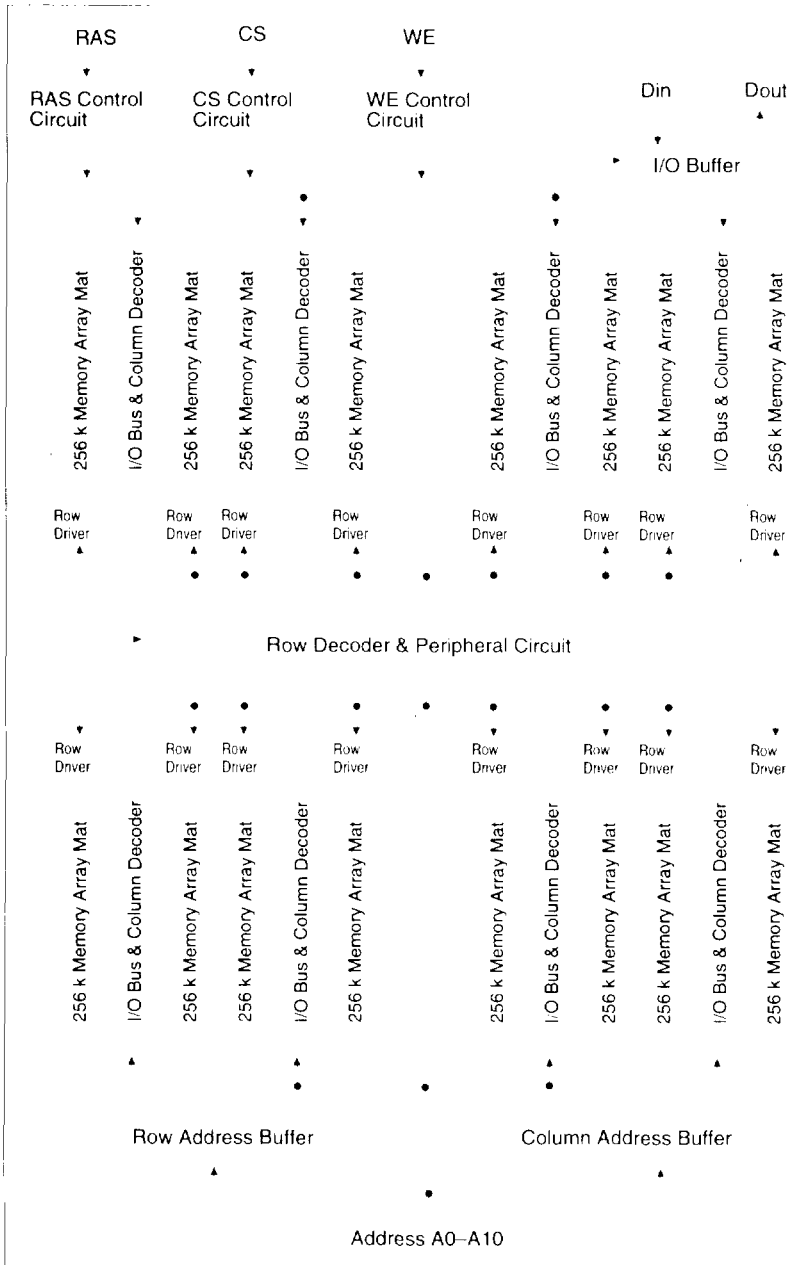
Pin Arrangement



Pin Description

Pin name	Function
A0 to A10	Address input
A0 to A9	Refresh address input
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Read/Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note : 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

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		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test condition	Notes
Operating current	I_{CC1}	—	100	—	90	mA	$\overline{RAS}$, $\overline{CS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)		—	100	—	100	µA	CMOS interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} $\overline{WE}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z	5
$\overline{RAS}$-only refresh current	I_{CC3}	—	100	—	90	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL} Dout = enable	1
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	100	—	90	mA	t_{RC} = min	
Static column mode current	I_{CC9}	—	100	—	90	mA	t_{SC} = min	1, 3, 4
Battery back up current (Standby with CBR refresh) (L-version)	I_{CC10}	—	200	—	200	µA	t_{RC} = 125 µs $t_{\overline{RAS}}$ ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CS}$ = V_{IL}, Address, Din = V_{IH} or V_{IL}, Dout = High-Z	5
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.
4. Invalid address is prohibited during static column cycle.
5. V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V and 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *17, *18

Test Conditions

- Input rise and fall times : 5 ns
- Input timing reference levels : 0.8 V, 2.4 V
- Output load : 2 TTL gate + C_L (100 pF)
  (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514102C/CL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	ns	21
$\overline{CS}$ pulse width	t_{SP}	20	10000	20	10000	ns	22
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	ns	
$\overline{CS}$ hold time	t_{CSH}	70	—	80	—	ns	

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)(cont.)

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	ns	2, 3, 19
Access time from $\overline{CS}$	t_{ACS}	—	20	—	20	ns	3, 4, 19
Access time from address	t_{AA}	—	35	—	40	ns	3, 5, 14, 19
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	t_{RCH}	0	—	0	—	ns	20
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	20
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	20	ns	6
$\overline{RAS}$ to column address hold time	t_{AHR}	15	—	15	—	ns	16
Output hold time from address	t_{AOH}	5	—	5	—	ns	
Column address hold time to $\overline{RAS}$ on read	t_{AR}	70	—	80	—	ns	

Write Cycle

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	65	—	70	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	ns	11
Data-in hold time to $\overline{RAS}$	t_{DHR}	65	—	70	—	ns	
Column address hold time to $\overline{RAS}$ on write	t_{AWR}	65	—	70	—	ns	

Read-Modify-Write Cycle

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	155	—	175	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	70	—	80	—	ns	10
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	20	—	20	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	35	—	40	—	ns	10
Output hold time from $\overline{WE}$	t_{WOH}	0	—	0	—	ns	

Refresh Cycle

Parameter	Symbol	HM514102C/CL -7 Min	-7 Max	-8 Min	-8 Max	Unit	Notes
$\overline{CS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	—	10	—	ns	
$\overline{CS}$ precharge time in normal mode	t_{SIN}	10	—	10	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514102C/CL -7 Min	-7 Max	-8 Min	-8 Max	Unit	Notes
Static column mode cycle time	t_{SC}	40	—	45	—	ns	
Static column mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	70	—	80	—	ns	
Static column mode $\overline{CS}$ precharge time	t_{SI}	10	—	10	—	ns	
Write invalid time	t_{WI}	10	—	10	—	ns	

Static Column Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM514102C/CL -7 Min	-7 Max	-8 Min	-8 Max	Unit	Notes
Static column mode cycle time on read-modify-write	t_{SRW}	75	—	85	—	ns	12
Access time from previous $\overline{WE}$	t_{ALW}	—	70	—	80	ns	3, 13, 19
Previous $\overline{WE}$ to column address delay time	t_{LWAD}	20	35	20	40	ns	15
Column address hold time to previous $\overline{WE}$	t_{AHLW}	70	—	80	—	ns	
Output enable time from $\overline{WE}$	t_{OW}	—	25	—	25	ns	19

Test Mode Cycle

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	10	—	10	—	ns	

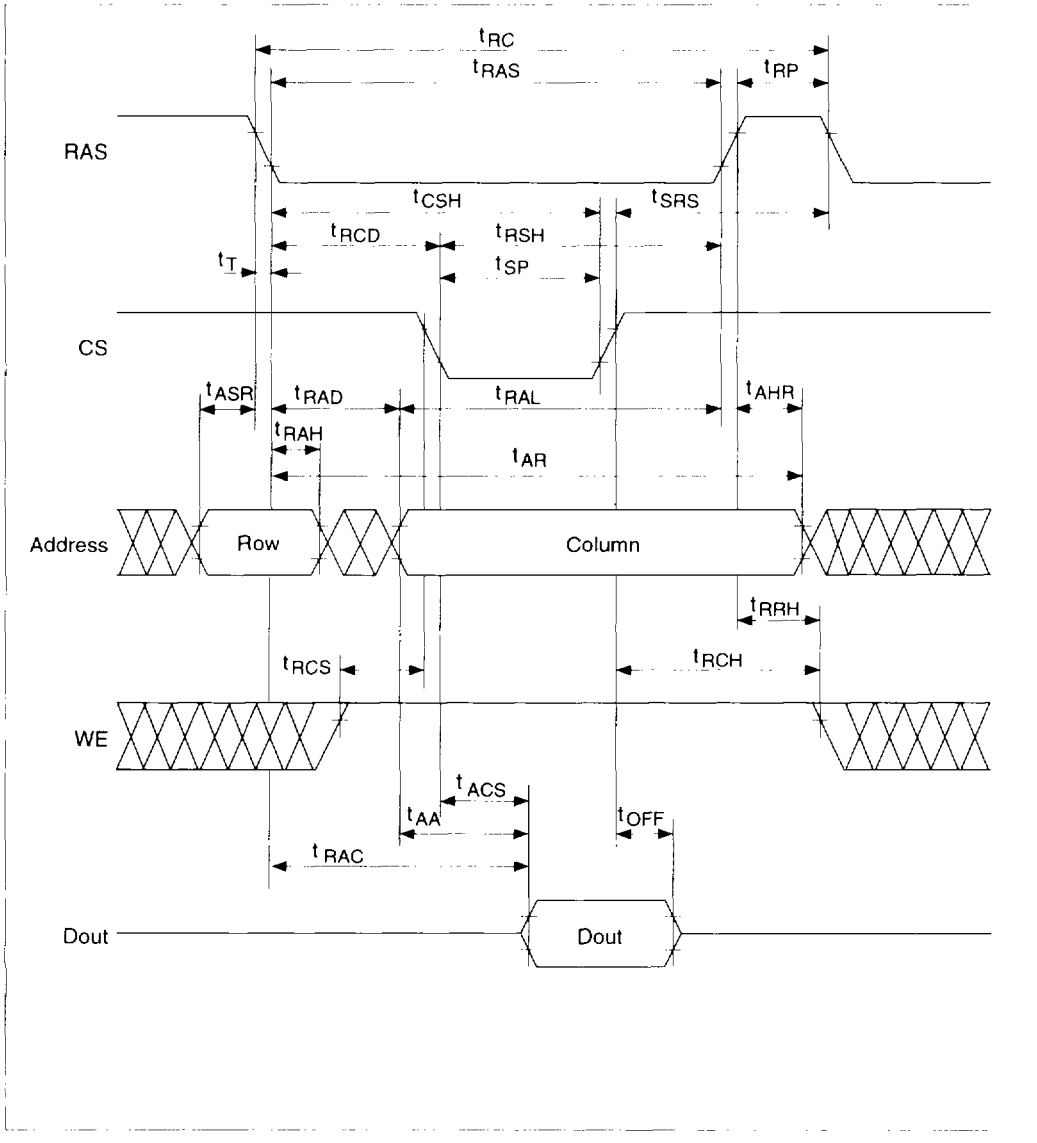
Counter Test Cycle

		HM514102C/CL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CS}$ precharge time in counter test cycle	t_{SIT}	40	—	40	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} > t_{CWD}$ (min) and $t_{AWD} > t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} defines the time at which the column address hold.
17. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CS}$-before-$\overline{RAS}$ refresh cycles is required.
18. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.
19. In a test mode read cycle, the value of t_{RAC}, t_{ACS}, t_{AA}, t_{OW} and t_{ALW} are delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
20. Either t_{RCH} or t_{RRH} must be satisfied.
21. t_{RAS} (min) = t_{RWD} (min) + t_{RWL} (min) + t_T in read-modify-write cycle.
22. t_{SP} (min) = t_{CWD} (min) + t_{CWL} (min) + t_T in read-modify-write cycle.

Timing Waveforms*23

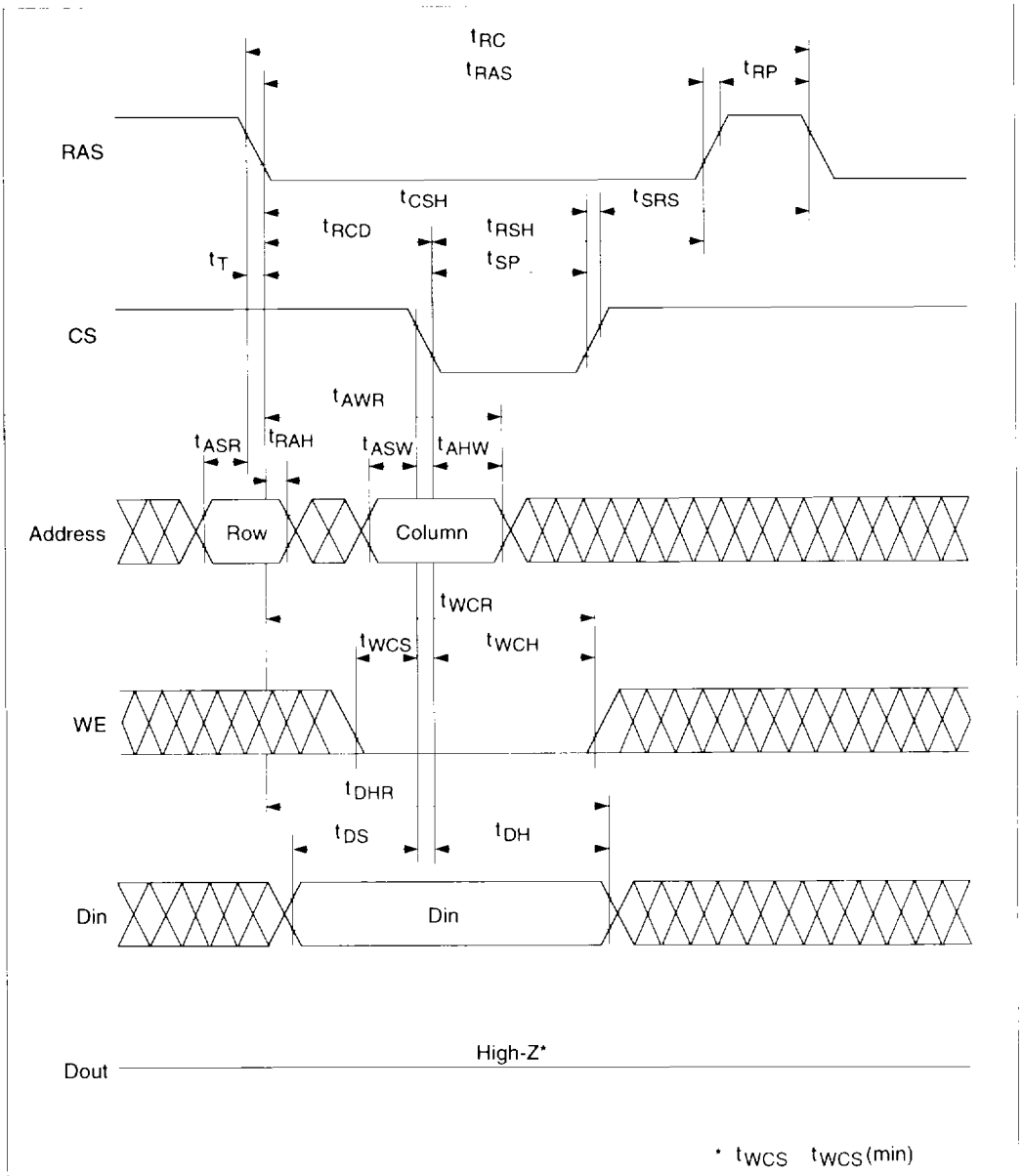
Read Cycle



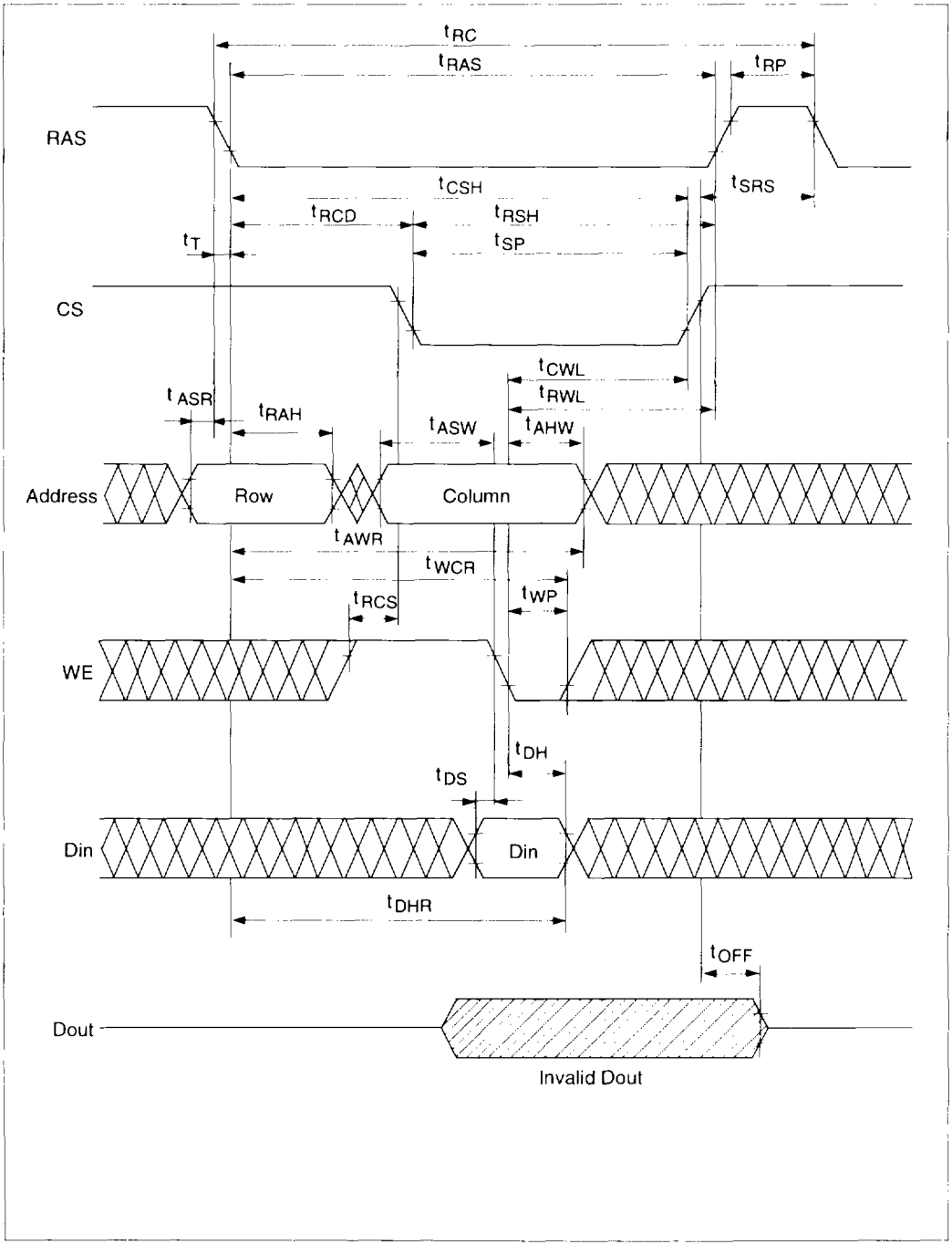
Note 23: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

Invalid Dout

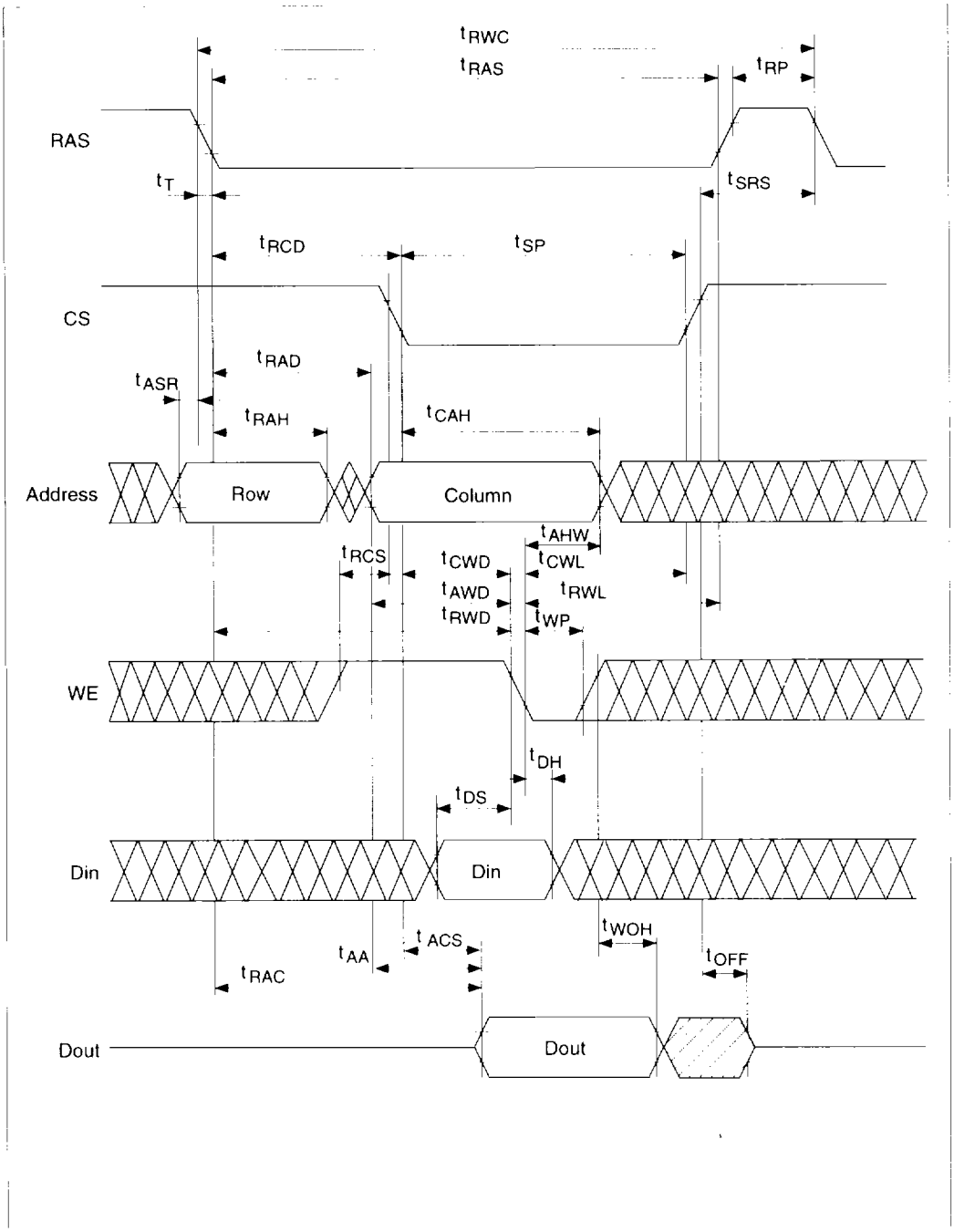
Early Write Cycle



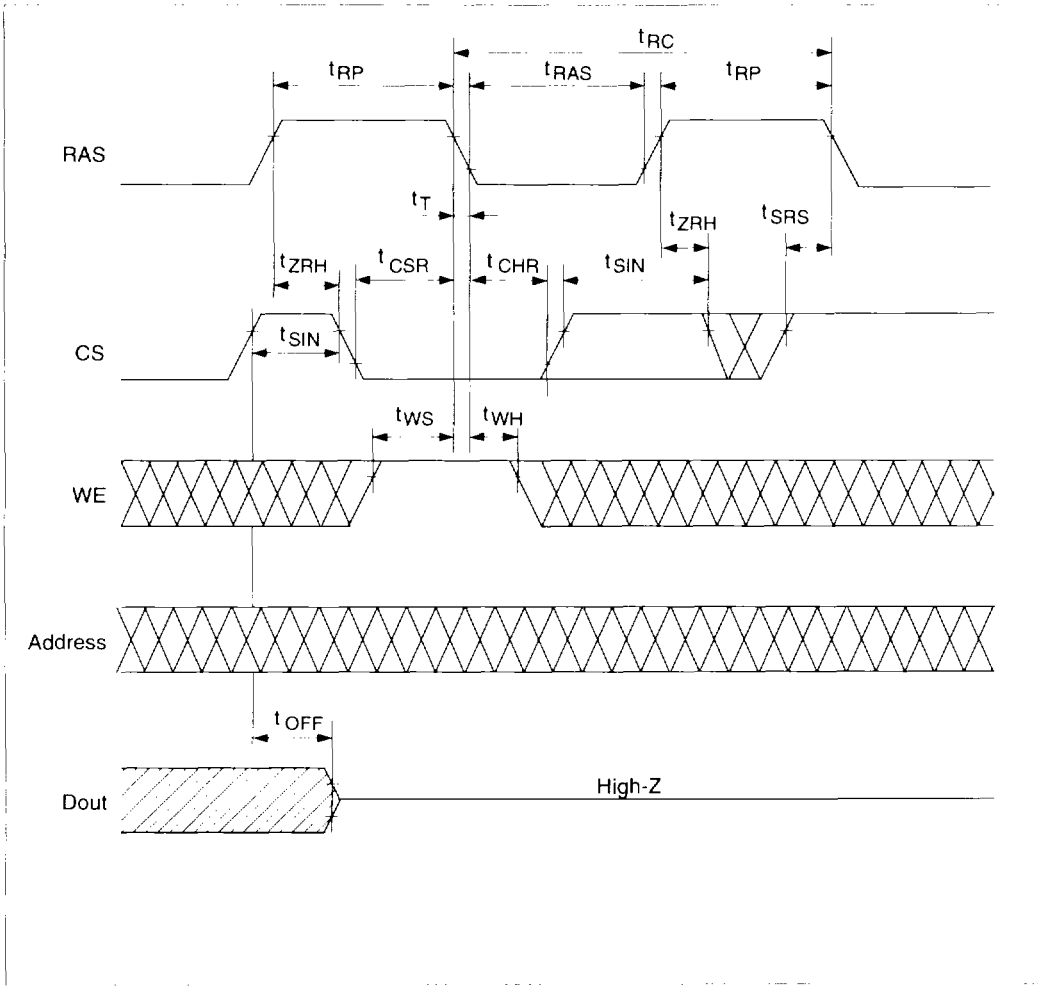
Delayed Write Cycle



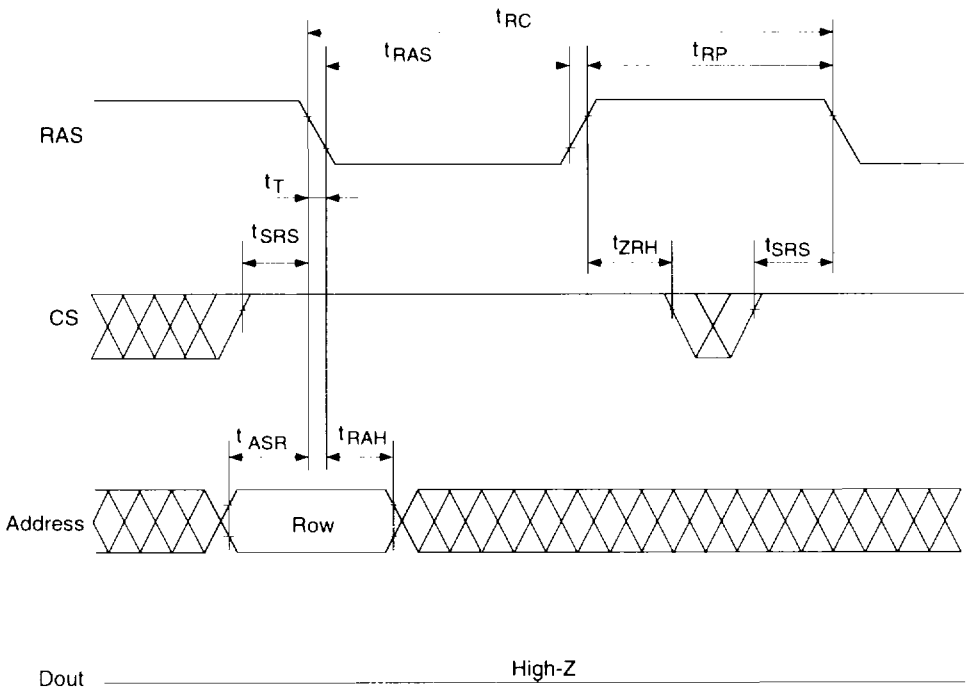
Read-Modify-Write Cycle



$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle



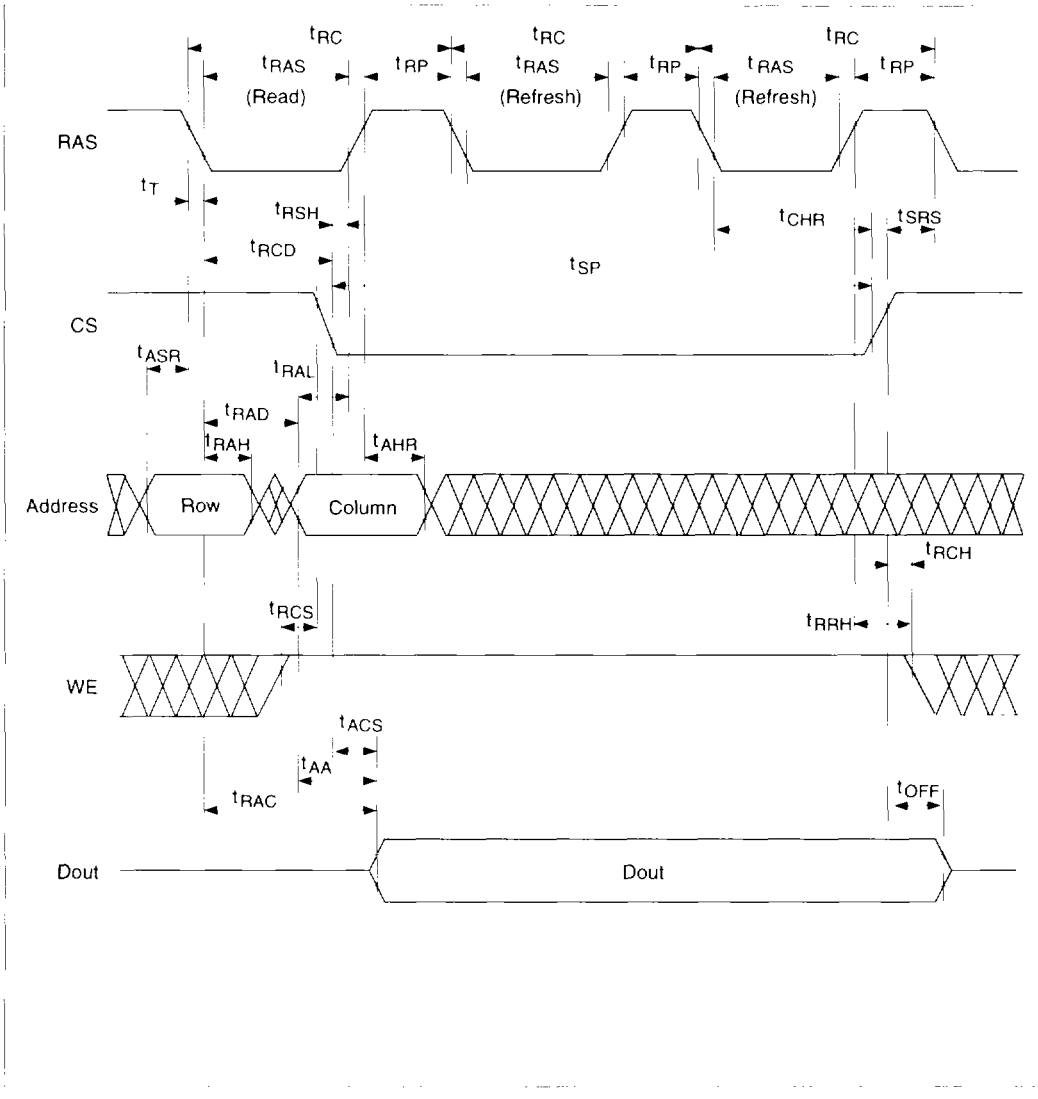
$\overline{\text{RAS}}$-Only Refresh Cycle



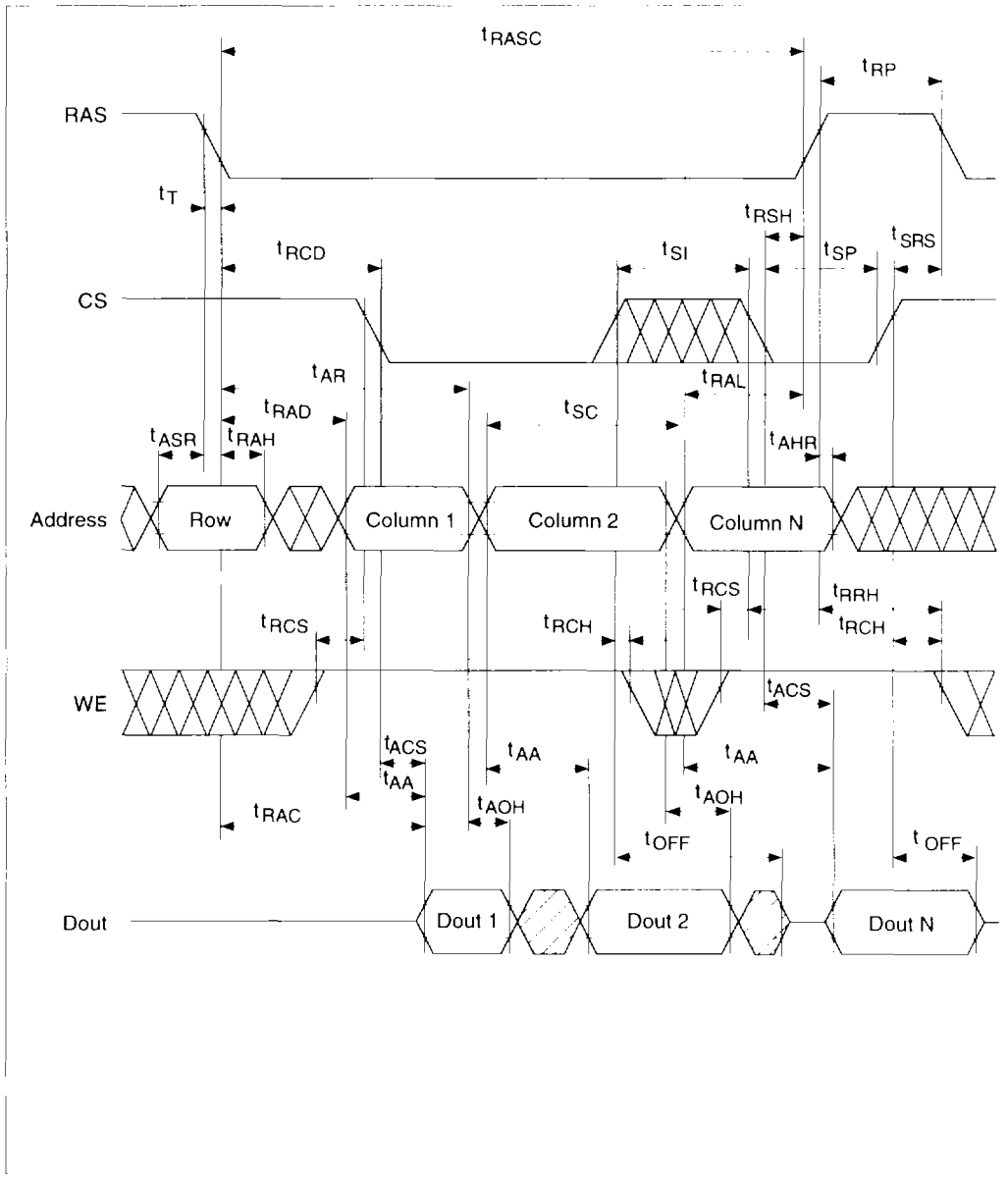
* Refresh address : A0 – A9 (AX0 – AX9)

** WE : H or L

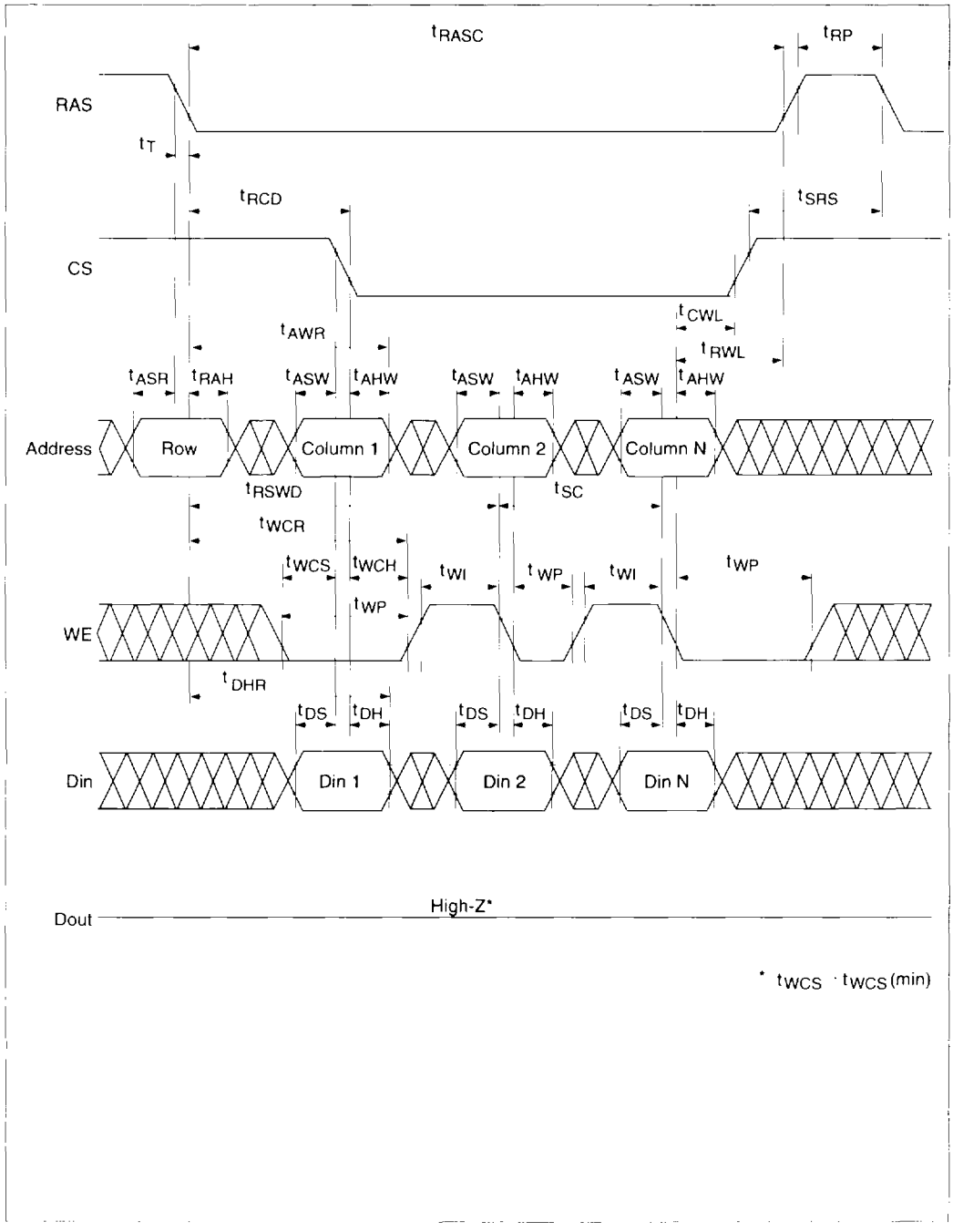
Hidden Refresh Cycle



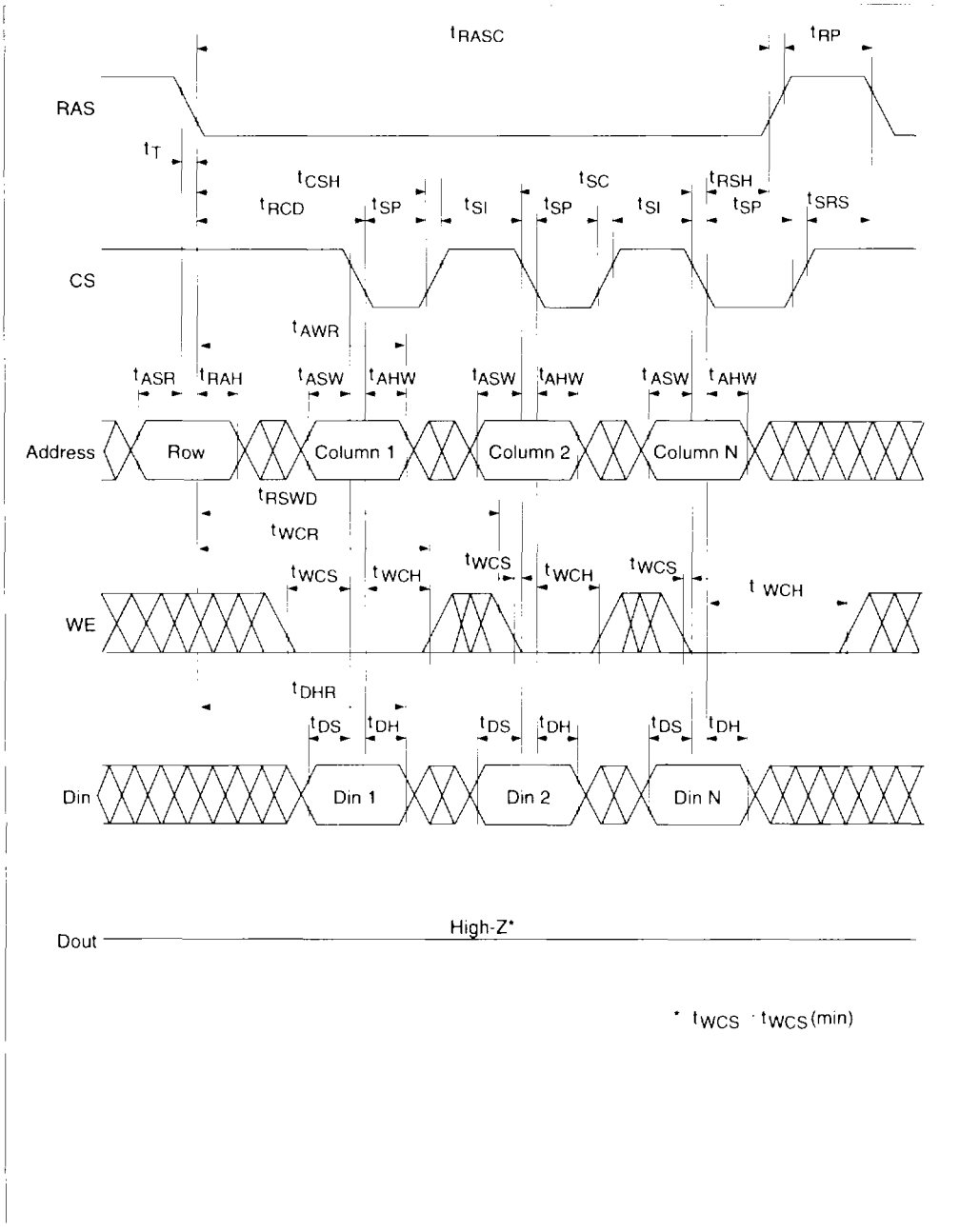
Static Column Mode Read Cycle



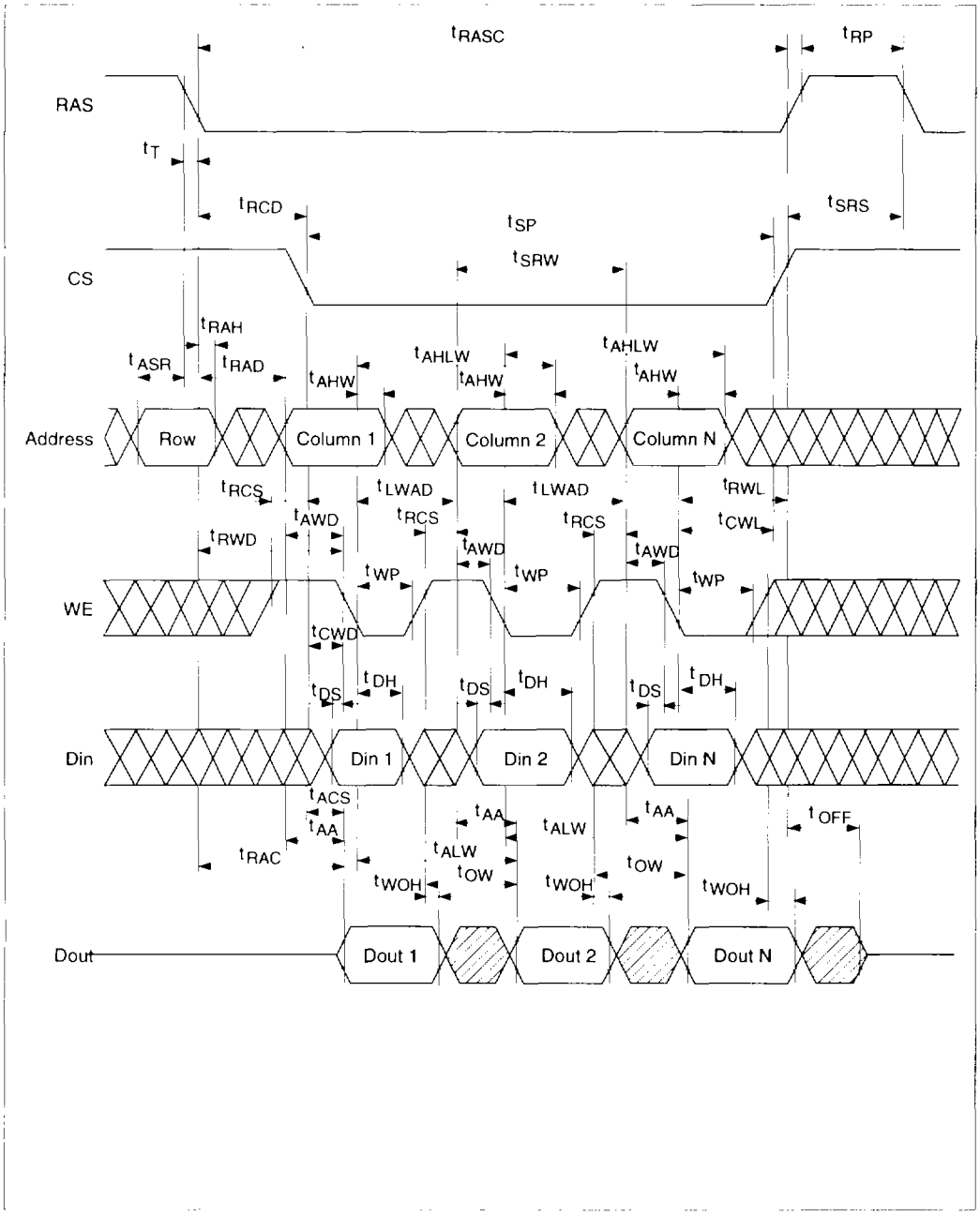
Static Column Mode Write Cycle (1)



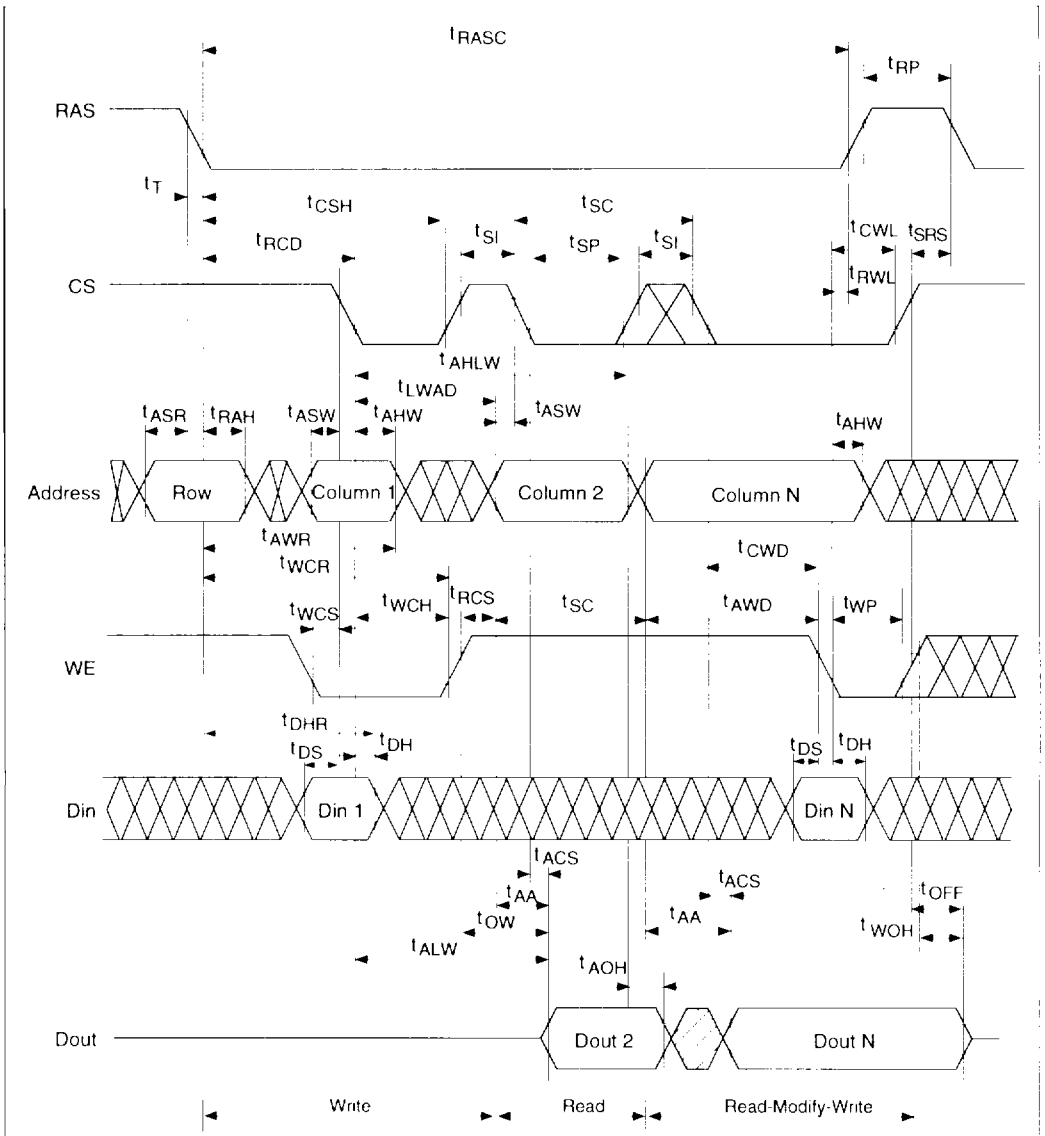
Static Column Mode Write Cycle (2)



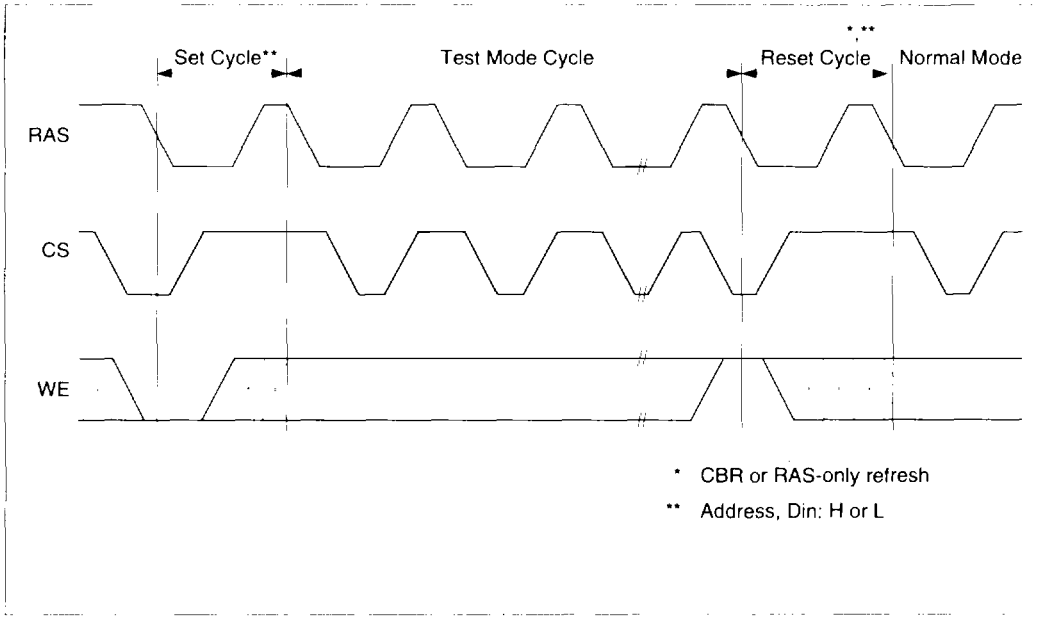
Static Column Mode Read-Modify-Write Cycle



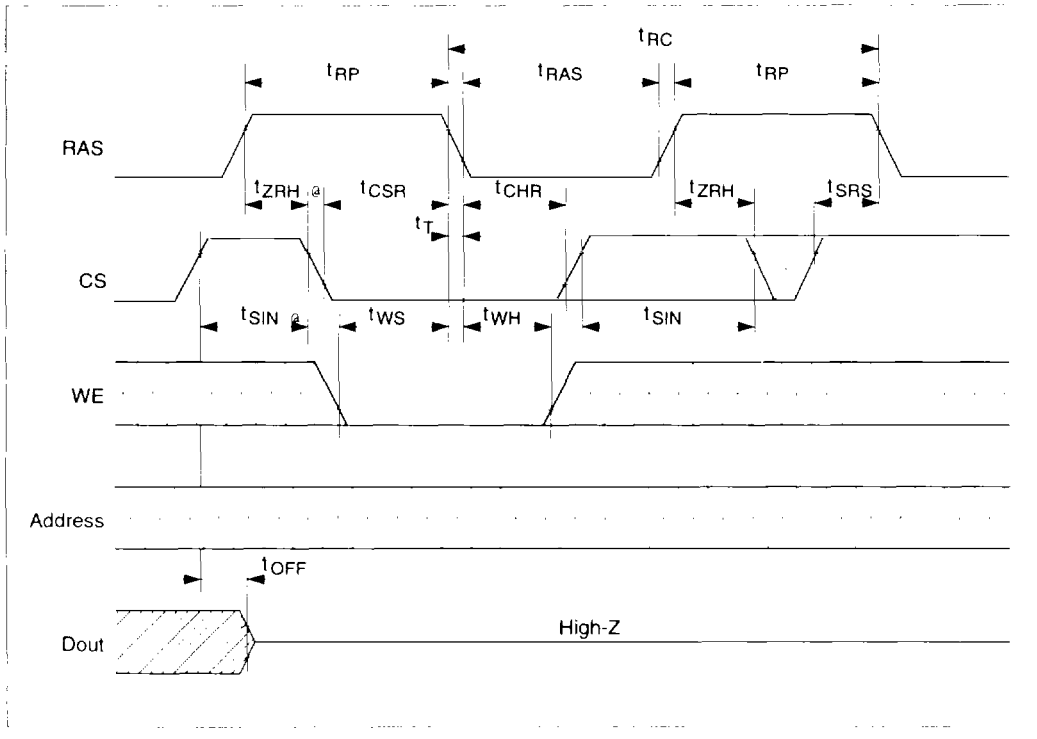
Static Column Mode Mixed Cycle



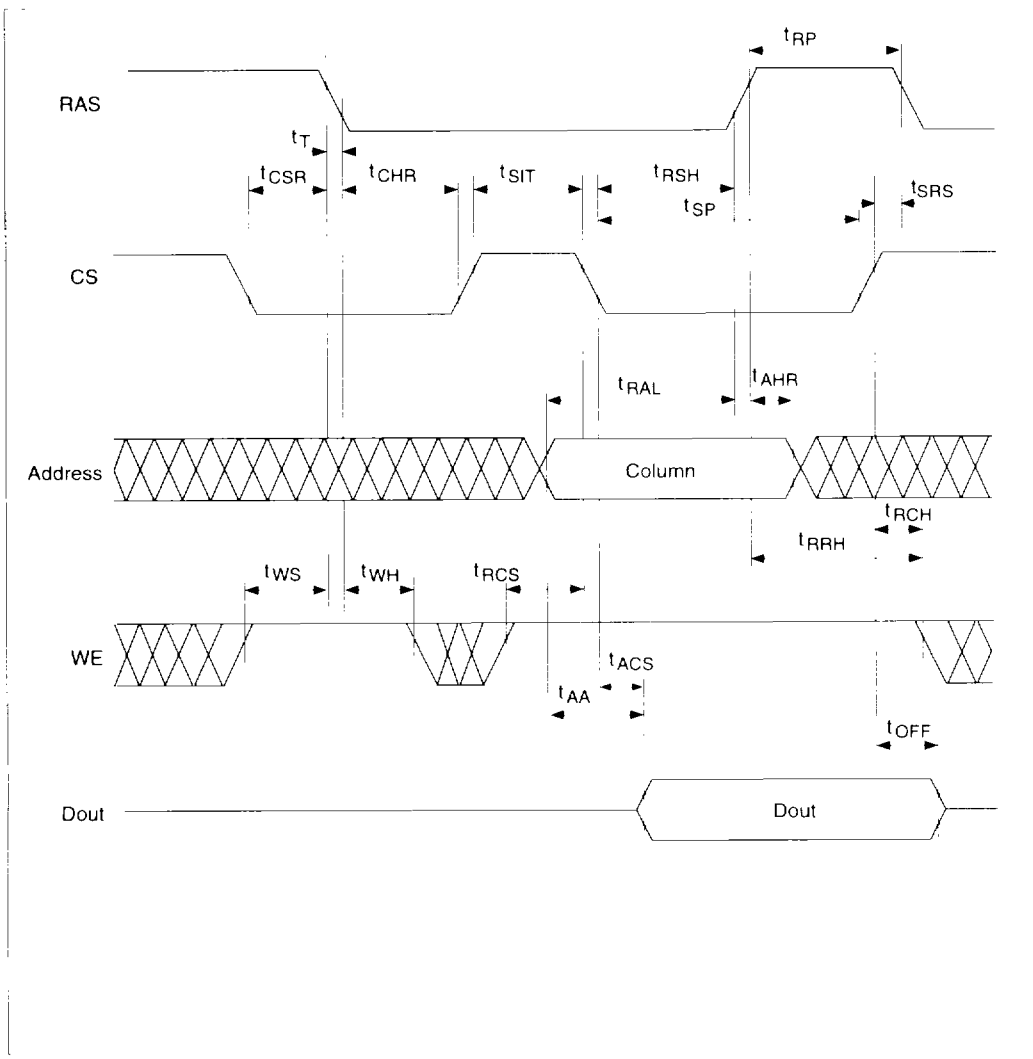
Test Mode Cycle



Test Mode Set Cycle



$\overline{CS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)