HSP48908/883

January 1994

Two Dimensional Convolver

Features

- **This Circuit is Processed In Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Single Chip 3 x 3 Kernel Convolution**
- **Programmable On-Chip Row Buffers**
- **DC to 27MHz Clock Rate**
- **Cascadable for Larger Kernels and Images**
- **On-Chip 8-Bit ALU**
- **Dual Coefficient Mask Registers, Switchable In a Single Clock Cycle**
- **8-Bit Signed or Unsigned Input and Coefficient Data**
- **20-Bit Extended Precision Output**
- **Standard µP Interface**

Applications

- **Image Filtering**
- **Edge Detection**
- **Adaptive Filtering**
- **Real Time Video Filters**

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HSP48908GM-20/883	-55°C to +125°C	84 Lead PGA
HSP48908GM-27/883	-55°C to +125°C	84 Lead PGA

Description

The Harris HSP48908/883 is a high speed Two Dimensional Convolver which provides a single chip implementation of a video data rate 3 x 3 kernel convolution on two dimensional data. It eliminates the need for external data storage through the use of the on-chip row buffers which are programmable for row lengths up to 1024 pixels.

There are internal register banks for storing two independent 3 x 3 filter kernels, thus facilitating the implementation of adaptive filters and multiple filter operations on the same data. The pixel data path also includes an on-chip ALU for performing real-time arithmetic and logical pixel point operations.

Data is provided to the HSP48908/883 in a raster scan non-interlaced fashion, and is internally buffered on images up to 1024 pixels wide for the 3 x 3 convolution operation. Images with larger rows and convolution with larger kernel sizes can be accommodated by using external row buffers and/or multiple HSP48908/883s. Coefficient and pixel input data are 8-bit signed or unsigned integers, and the 20-bit convolver output guarantees no overflow for kernel sizes up to 4 x 4. Larger kernel sizes can be implemented however, since the filter coefficients will normally be less than their maximum 8-bit values.

The HSP48908/883 is manufactured using an advanced CMOS process, and is a low power fully static design. The configuration of the device is controlled through a standard microprocessor interface and all inputs/outputs are TTL compatible.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2783.3**

Pinout

HSP48908/883 (PGA)
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	CASO6	DOUT0	DOUT1	GND	DOUT5	DOUT6	DOUT8	DOUT10	DOUT12	DOUT13	DOUT15
10	CASO4	CASO5	CASO7	DOUT2	DOUT4	DOUT9	GND	DOUT11	DOUT14	GND	DOUT17
9	CASO3	GND			DOUT3	DOUT7	V_{CC}			DOUT16	DOUT18
8	CASO1	CASO2								DOUT19	GND
7	OE#	GND	V_{CC}						CASI1	FRAME#	CASI0
6	DIN1	CASO0	DIN0		84 PIN PGA TOP VIEW				CASI2	V_{CC}	RESET#
5	DIN2	DIN3	DIN4						CASI5	CASI4	CASI3
4	DIN5	DIN6								CASI7	CASI6
3	DIN7	CIN1			CIN9	HOLD	LD#			CASI10	CASI8
2	CIN0	CIN3	CIN4	CIN7	GND	V_{CC}	A2	EALU	CASI13	CASI11	CASI9
1	CIN2	CIN5	CIN6	CIN8	CLK	A1	CS#	A0	CASI15	CASI14	CASI12

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied .... GND-0.5V to V_{CC}+0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10 sec) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic PGA Package	35.0°C/W	7.7°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package 1.45W
Gate Count ..... 190,000 Transistors

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Voltage Range ..... +4.5V to +5.5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Logical 1 Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.2	-	V
Logical 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Clock Input High	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	3.0	-	V
Clock Input Low	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 1)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	0.4	V
Input Leakage Current	I_I	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	µA
Output or I/O Leakage Current	I_O	$V_{OUT} = V_{CC}$ or GND V_{CC} = 5.5V	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5V Outputs Open (Note 4)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20.0MHz V_{CC} = 5.5V Outputs Open, (Notes 2, 4)	1, 2, 3	$-55°C \leq T_A \leq +125°C$	-	160.0	mA
Functional Test	FT	(Notes 3, 4)	7, 8	$-55°C \leq T_A \leq +125°C$	-	-	-

NOTES:
1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 8.0mA/MHz.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V, V_{IHC} = 3.4V, and V_{ILC} = 0.4V.
4. Loading is a specified in the test load circuit with C_L = 40pF.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C (Note 4)

PARAMETERS	SYMBOL	CONDI-TIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS				UNITS
					-27 (27MHz)		-20 (20MHz)		
					MIN	MAX	MIN	MAX	
Clock Period	T_{CYCLE}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	37	-	50	-	ns
Clock Pulse Width High	T_{PWH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
Clock Pulse Width Low	T_{PWL}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
Data Input Setup Time	T_{DS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	16	-	17	-	ns
Data Input Hold Time	T_{DH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Clock to Data Out	T_{OUT}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	19	-	28	ns
Address Setup Time	T_{AS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	15	-	ns
Address Hold Time	T_{AH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Configuration Data Setup Time	T_{CDS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	17	-	20	-	ns
Configuration Data Hold Time	T_{CDH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
LD# Pulse Width	T_{LPW}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	20	-	ns
LD# Setup Time	T_{LCS}	Note 1	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	37	-	ns
CIN7-0 Setup to CLK	T_{CS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	17	-	20	-	ns
CIN7-0 Hold from CLK	T_{CH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CS# Setup to LD#	T_{CSS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
CS# Hold from LD#	T_{CSH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
RESET# Pulse Width	T_{RPW}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	37	-	50	-	ns
FRAME# Setup to CLK	T_{FS}	Note 2	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	25	-	30	-	ns
FRAME# Pulse Width	T_{FPW}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	37	-	50	-	ns
EALU Setup Time	T_{ES}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	17	-	ns
EALU Hold Time	T_{EH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
HOLD Setup Time	T_{HS}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	13	-	14	-	ns
HOLD Hold Time	T_{HH}		9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	2	-	2	-	ns
Output Enable Time	T_{EN}	Note 3	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	19	-	28	ns

NOTES:

1. This specification applies only to the case where the HSP48908/883 is being written to during an active convolution cycle. It must be met in order to achieve predictable results at the next rising clock edge. In most applications, the configuration data and coefficients are loaded asynchronously and the T_{LCS} specification may be disregarded.
2. While FRAME# is an asynchronous signal, it must be deasserted a minimum of T_{FS} ns prior to the rising clock edge which is to begin loading pixel data for a new frame.
3. Transition is measured at ±200mV from steady state voltage with loading as specified in test load circuit with C_L = 40pF.
4. A.C. Testing is performed as follows: Input levels (CLK Input) 4.0V and 0V, Input levels (All other Inputs) 0V and 3.0V, Timing Reference Levels (CLK) = 2.0V, (Others) = 1.5V. Output load per test load circuit with C_L = 40pF. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS -27 MIN	LIMITS -27 MAX	LIMITS -20 MIN	LIMITS -20 MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	T_A = +25°C	-	10	-	10	pF
Output Capacitance	C_O	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	T_A = +25°C	-	12	-	12	pF
Output Disable Time	T_{OZ}		1, 2	-55°C ≤ T_A ≤ +125°C	-	35	-	40	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	-55°C ≤ T_A ≤ +125°C	-	6	-	6	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	-55°C ≤ T_A ≤ +125°C	-	6	-	6	ns

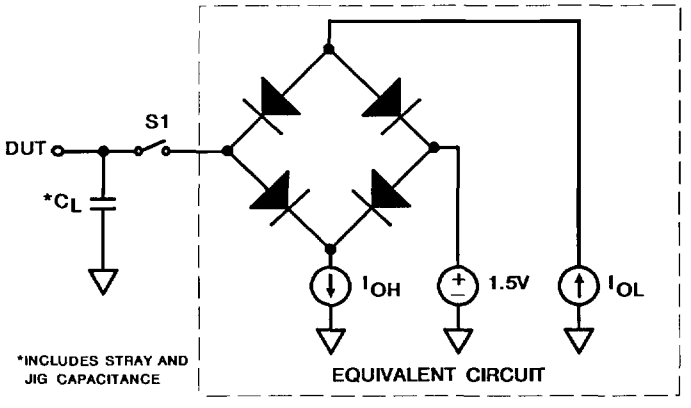
NOTES: 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

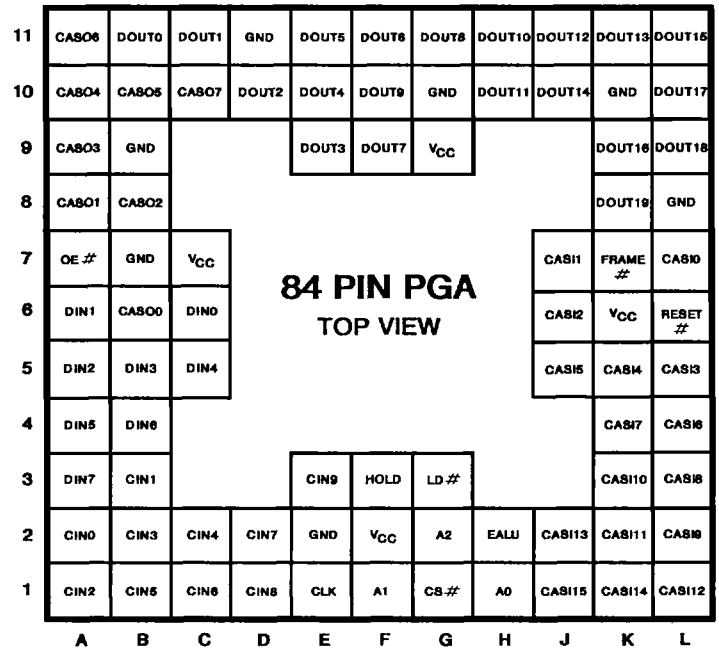
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit



Switch S1 Open for I_{CCSB} and I_{CCOP} Tests

Burn-In Circuit



PGA BURN-IN SCHEMATIC

PIN NAME	PGA PIN	BURN-IN SIGNAL
CIN2	A1	F13
CIN0	A2	F12
DIN7	A3	F7
DIN5	A4	F5
DIN2	A5	F2
DIN1	A6	F1
OE	A7	F10
CASO.1	A8	$V_{CC}/2$
CASO.3	A9	$V_{CC}/2$
CASO.4	A10	$V_{CC}/2$
CASO.6	A11	$V_{CC}/2$
CIN5	B1	F12
CIN3	B2	F13
CIN1	B3	F12
DIN6	B4	F6
DIN3	B5	F3
CASO.0	B6	$V_{CC}/2$
GND	B7	GND
CASO.2	B8	$V_{CC}/2$
GND	B9	GND
CASO.5	B10	$V_{CC}/2$
POUT0	B11	$V_{CC}/2$
CIN6	C1	F13
CIN4	C2	F13
DIN4	C5	F4
DIN0	C6	F0
V_{CC}	C7	V_{CC}
CASO.7	C10	$V_{CC}/2$

PIN NAME	PGA PIN	BURN-IN SIGNAL
POUT1	C11	$V_{CC}/2$
CIN8	D1	F14
CIN7	D2	F12
POUT2	D10	$V_{CC}/2$
GND	D11	GND
CLK	E1	F0
GND	E2	GND
CIN9	E3	F14
POUT3	E9	$V_{CC}/2$
POUT4	E10	$V_{CC}/2$
POUT5	E11	$V_{CC}/2$
A1	F1	F13
V_{CC}	F2	V_{CC}
HOLD	F3	F14
POUT7	F9	$V_{CC}/2$
POUT9	F10	$V_{CC}/2$
POUT6	F11	$V_{CC}/2$
CS	G1	F12
A2	G2	F14
LOAD	G3	F11
V_{CC}	G9	V_{CC}
GND	G10	GND
POUT8	G11	$V_{CC}/2$
A0	H1	F12
EALU	H2	F8
POUT11	H10	$V_{CC}/2$
POUT10	H11	$V_{CC}/2$
CASI.15	J1	F7

PIN NAME	PGA PIN	BURN-IN SIGNAL
CASI.13	J2	F5
CASI.5	J5	F5
CASI.2	J6	F2
CASI.1	J7	F1
POUT14	J10	$V_{CC}/2$
POUT12	J11	$V_{CC}/2$
CASI.14	K1	F6
CASI.11	K2	F3
CASI.10	K3	F2
CASI.7	K4	F7
CASI.4	K5	F4
V_{CC}	K6	V_{CC}
FRAME	K7	F15
POUT19	K8	$V_{CC}/2$
POUT16	K9	$V_{CC}/2$
GND	K10	GND
POUT13	K11	$V_{CC}/2$
CASI.12	L1	F4
CASI.9	L2	F1
CASI.8	L3	F0
CASI.6	L4	F6
CASI.3	L5	F3
RESET	L6	F16
CASI.0	L7	F0
GND	L8	GND
POUT18	L9	$V_{CC}/2$
POUT17	L10	$V_{CC}/2$
POUT15	L11	$V_{CC}/2$

NOTES:
1. $V_{CC}/2$ (2.7V ± 10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ± 0.5V.
4. 0.1µF (min) capacitor between V_{CC} and GND per position.
5. F0 = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2, 40-60% Duty Cycle.
6. Input Voltage Limits: V_{IL} = 0.8V max., V_{IH} = 4.5V ± 10%.

Die Characteristics

DIE DIMENSIONS:
341 x 322 x 19 ± 1 mils

METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

WORST CASE CURRENT DENSITY:
$2 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

Metallization Mask Layout

HSP48908/883