A66110/A66111

DIGITAL ARRAY SIGNAL PROCESSOR (DASP)

ARRAY Microsystems

PRELIMINARY DATA SHEET - REVISION 3.0, MARCH, 1991

FEATURES:

- Arithmetic throughput of up to 400 million operations per second
- Processes 16-bit real or 32-bit complex integer arrays
- 16 FFT specific and general purpose array processing functions
- 16 to 20 Bit fixed point arithmetic with full block floating point support for FFT functions
- 144 and 269 pin PGA package
- 2-3W typical power dissipation

RELATED PRODUCTS:

Programmable Array Controller (PAC): A66210/A66211

APPLICATIONS:

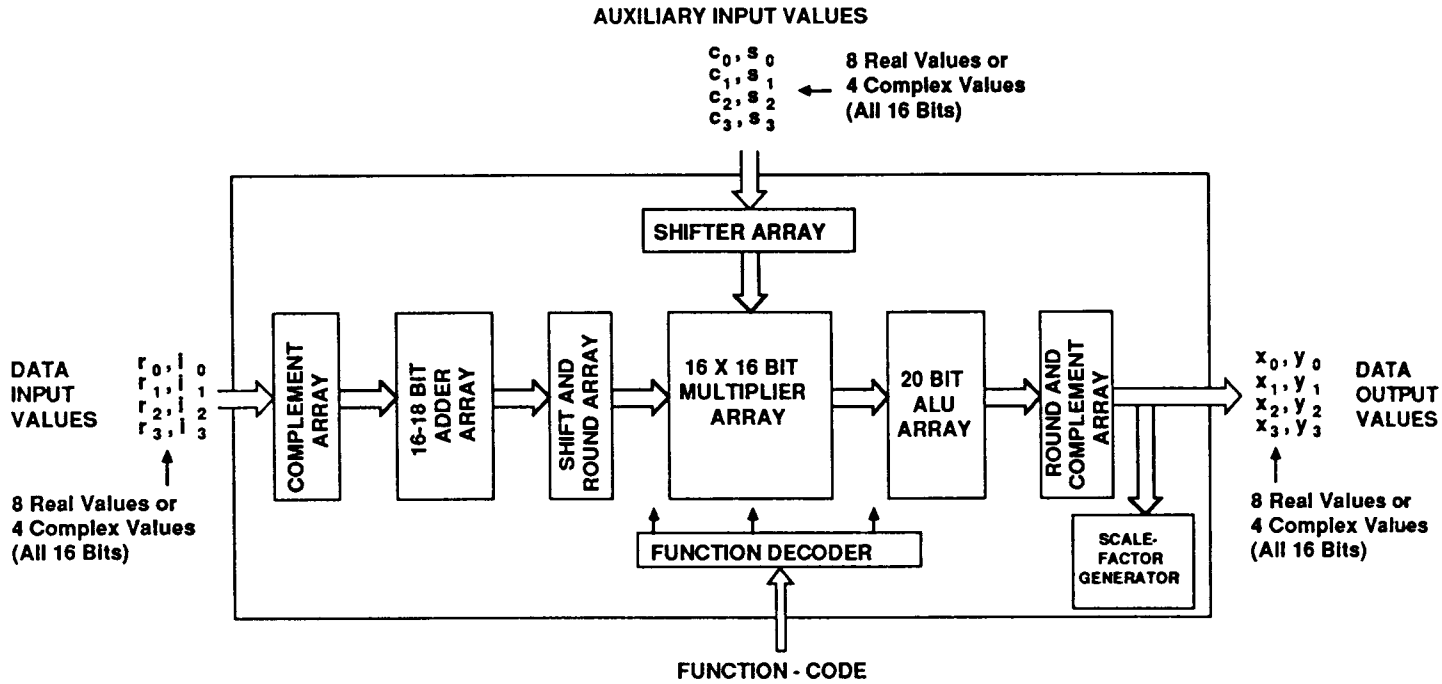
- Radar
- Sonar
- EW/ECM
- Digital Radio
- Test Instruments
- Medical Instruments
- Spectrum Analyzers
- Transmultiplexing
- Image Processing
- Image Compression
- Image Reconstruction
- Spread Spectrum Communications

GENERAL DESCRIPTION:

The DASP/PAC chip set is the first chip set in the A66XXX family of array processing devices. It is specifically designed to fulfill the numerical processing, memory address generation, program sequencing and storage requirements of very high performance, real time DSP systems, especially those involving the computation of the Fast Fourier Transform (FFT). The DASP is a pipelined complex arithmetic computing element which can be easily interfaced with static RAMs in ping-pong or unidirectional memory architectures.

The DASP is available in the commercial temperature range in two speed grades; military temperature range parts are also available in two speed grades, with one of the grades qualified to MIL-STD-883 levels. The A66110 is available in a 269 PGA, and the A66111 is available in a 144 PGA.

BLOCK DIAGRAM



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FUNCTIONAL OVERVIEW

The DASP is a very high speed, block floating-point array processor which is capable of performing FFT specific and general purpose operations on arrays of data. A detailed functional description of the DASP can be found in the **DASP User's Guide**.

Architecture

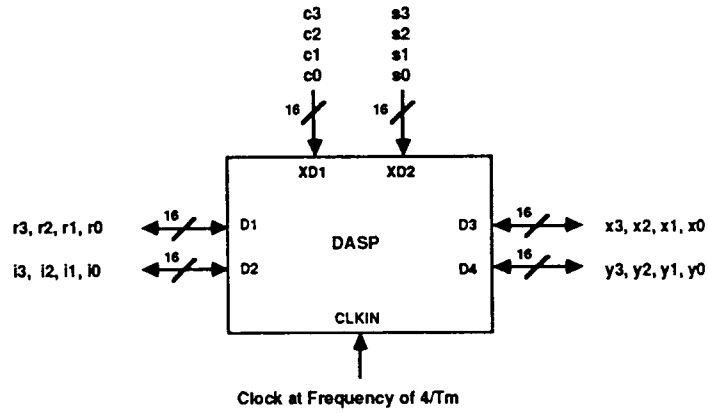
The DASP can process sixteen 16-bit real values (or 8 complex values), and output eight 16-bit real values (or 4 complex values) every machine cycle (Tm). The lower limit on Tm is 100 nanoseconds. A block diagram of the DASP, which shows the internal data paths and input/output values, is shown in on page 1. All the input/output values, shown in the block diagram, are transferred every DASP machine cycle. The values r0....r3, i0....i3, form the input data set which is fed to the DASP every machine cycle. In complex arithmetic operations (such as the FFT), these values represent a set of 4 complex numbers: (r0, i0), (r1, i1), (r2, i2), (r3, i3). Another set of eight 16-bit input operands, called auxiliary data, is designated as c0....c3, s0....s3. In complex arithmetic instructions, these values are complex numbers, [(c0, s0), (c1, s1), (c2, s2), (c3, s3)], representing data such as window coefficients or trigonometrical coefficients. After operating on the input operands, the DASP produces a set of eight 16-bit values x0....x3, y0....y3. Once again, these values represent a set of four complex numbers, [(x0, y0), (x1,y1), (x2, y2), (x3, y3)], for complex arithmetic instructions. In summary, there are three I/O ports (input data, input auxiliary data, and output data) on the DASP for data transfers.

The internal data paths of the DASP are also shown in the block diagram. First, the input data set is passed through an array of shifters to perform scaling, if desired. Then the scaled values are passed through an array of 18 bit adders; typically, these adders are used to perform the pre-multiplication additions associated with Decimation-In-Frequency (DIF) FFT Butterfly operations. The 18 bit sums are rounded to 16 bits and fed to an array of multipliers. At this stage, the multiplier array also receives a scaled set of values from the auxiliary input data port. After multiplication, the 20 most significant bits of each resulting product are retained. Next, the 20 bit products are processed by the ALU array. These ALUs are used to perform the post-multiplication additions associated with complex multiplications. In other instances, the ALUs can perform general purpose arithmetic and logical operations. The 20 bit outputs from the ALUs are finally rounded to 16 bits and fed to the data output port. The ALU outputs are also monitored by the on-chip scale-factor generator to implement the block floating point arithmetic which is discussed later. The data path operation is controlled by a function code which is externally applied (normally from the PAC chip). After setting up a function code, input data sets can be continuously passed through the DASP (one set every machine cycle, Tm). The DASP introduces a latency of four machine cycles from the main and auxiliary data inputs to the outputs. The impact of this latency is normally insignificant since the DASP primarily deals with data arrays on which a given function is applied to the entire array.

Input/Output

Transferring all the I/O data, mentioned in the previous section, can be accomplished using either one of two I/O bussing modes. One of the modes, which is called the dual bus mode, is shown in Figure 1. In this scheme, each of the three I/O ports appearing in the DASP block diagram is served by two 16 bit parallel buses. Each I/O port transfers 8 values at intervals of Tm, therefore each bus transfers a

FIGURE 1 — DASP DUAL BUS MODE



value at intervals of Tm/4. A clock signal at a frequency of 4/Tm is required to manage the DASP in the dual bus mode. The application of the dual bus DASP results in a simple system architecture since off-the-shelf single port memories can be used to serve every bus on the DASP. Also, the DASP input and output data ports (D1/D2, D3/D4) are bidirectional in the dual mode which means that the roles of buses D1/D2 and D3/D4 can be easily interchanged. During a given data pass, input data can be fed through the D1/D2 ports and outputs produced on the D3/D4 ports (Figure 1). In another pass, the inputs can be fed to the D3/D4 ports and outputs produced on the D1/D2 ports. This bidirectionality of the data ports makes the design of recursive ping-pong memory systems very easy. In such a system, arrays of data are passed through the DASP between pairs of memories, with one memory supplying the data to the DASP while the other

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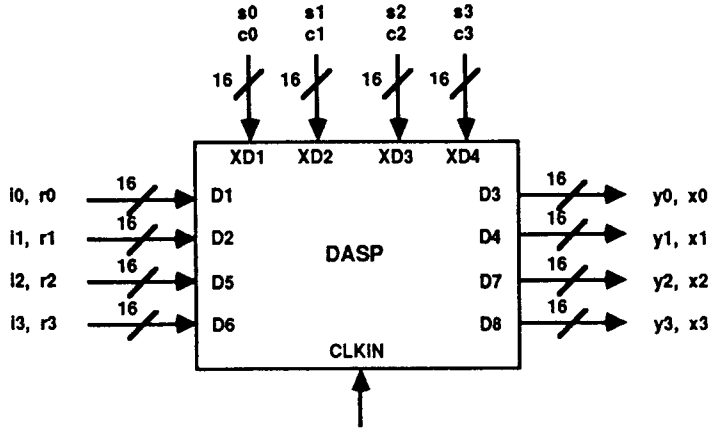
FIGURE 2 — DASP QUAD BUS OPTION



receives output data from the DASP. These memories alternate their read/write relationship on every pass, thereby implementing the data ping-pong. The DASP running in the dual mode can be used with Array Microsystems' Programmable Array Controller (PAC) chip in a wide variety of system architectures which are described in the **PAC User's Guide**.

Another I/O scheme, which is shown in Figure 2, is called the quad bus mode. In this mode, there are four buses associated with each port of the DASP. Therefore, each bus is operated at intervals of Tm/2, requiring an input clock to the DASP at a frequency of 2/Tm. In the quad mode, the access time on external memories is relaxed, however, the memory architecture will generally be more complicated compared to the dual I/O mode. A four port memory may be required in many applications for each of the three ports. In addition, the data I/O buses (D1/D2/D5/D6, D3/D4/D7/D8), as shown in Figure 2, are not bidirectional in the quad mode.

The DASP is offered in two pin grid array (PGA) packages. The A66110 supplies the DASP in a 269 PGA and supports both the dual and quad modes of operation; the quad bus mode is selected by applying a logic 1 to the QUAD pin on the device. The A66111 supplies the DASP in a 144 PGA and supports only the dual bus mode of operation which is the most commonly used. Aside from the differences regarding quad versus dual mode, the A66110 and A66111 are functionally identical.

Function Set

A total of 16 functions are supported on the DASP as listed in Table 1. Note that the DASP is capable of implementing each function every machine cycle (in period Tm). A function code on the pins FC(5:0) must be set up one machine cycle ahead of feeding the data to the processor. In typical array processing applications, such as FFTs, a function code is set up (e.g., BFLY4) and then the whole data array is clocked through the processor. Therefore, the applied function will be implemented on the whole array. There is a latency of four machine cycles in implementing each function on the DASP.

The complex arithmetic functions contain various functions to support FFT processing (Table 1). The BFLY4 and BFLY2 functions can be used to implement radix-4, radix-2 or mixed radix-4/radix-2 FFT algorithms. The functions FFTNN and FFT2N are useful for performing FFTs on real data [Reference 1 (p.166, 167)]. The FFTNN function can be used to process two frames of real data at a time, attaining an almost 2X performance advantage over complex data FFTs. The BMUL function can be used to perform windowing on an input data frame or used for general purpose complex multiplications as encountered in demodulation processes. The general arithmetic functions, listed in Table 1, can be used to implement various arithmetic functions on real and complex data. The function BSQSM can be used to determine the magnitude-squared of the frequency spectrum for FFT applications. The functions contained in the general logic class of Table 1 are useful for performing logic operations on arrays of data.

The DASP permits the conjugation of inputs and outputs during complex arithmetic functions which is especially useful for implementing inverse-FFTs. Similarly, the input and output data values can be complemented for the general arithmetic functions and logical functions. In addition, input values can be shifted during all functions. Data conjugation/complementation is controlled by bits 5 (for output data - referred to as "CO" in Table 1) and 4 (for input data - "CI" in Table 1) of the 6 bit function code FC(5:0). Shifting of input data is controlled via the SFI(2:0) input pins.

The detailed operation of each DASP function code outlined in Table 1 is covered in Section 4 of the **DASP User's Guide**.

Block Floating Point Arithmetic

Primarily, DASP input and output data are represented as 16 bit 2's complement values. However, on-chip intermediate values are up to 20 bits long and are rounded to 16 bits just prior to being output. This internal growth in data precision helps preserve an adequate signal-to-noise ratio for FFT-related computations. In addition, to avoid overflow problems, the DASP employs a block floating point scheme which applies data dependent scaling during an FFT to boost the dynamic range of the DASP's fixed point arithmetic. When a BFLY4 or BFLY2 function is running on the DASP, the device monitors the magnitude of complex data being produced at the output. After a complete pass through the data array, the device produces a scale factor on the SFO(2:0) pins, which should be used to scale the data on the next BFLY4/BFLY2 pass to prevent the DASP from overflowing. The scale

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factor is applied to the next data array by connecting the SFO output pins to the corresponding SFI input pins of the same or another DASP device. The DASP is also capable of accumulating the scale factors which appear on the SFO pins from one data pass to the next. The accumulated scale factor is produced on the ASFO(3:0) pins. The ASFO output from the final pass can then be used to normalize the final processed data array, if needed.

REFERENCES

Reference 1: **The Fast Fourier Transform**, E. O. Brigham, Prentice-Hall, 1974

TABLE 1 — DASP FUNCTIONS

Function Mnemonic	Opcode	Description
Complex Arithmetic Class		
BFLY4	CO CI 0000	Radix-4 Decimation in Frequency Butterfly
BFLY2	CO CI 0001	Two Radix-2 Decimation-in-Frequency Butterflies
FFT2N	CO CI 0010	Recombine N Complex-Point FFT to 2N Real-Point FFT
FFTNN	CO CI 0011	Recombine N Complex-Point FFT to two N Real Point FFTs
BMUL	CO CI 0101	Block Multiply Two Sets of Complex Numbers
General Arithmetic Class		
AFLOW	CO CI 0100	Arithmetic Flow Through
BSQSM	CO CI 0110	Block Square and Sum a Set of Complex Values
BADD	CO CI 0111	Block Add Two Sets of Real or Complex Values
BSUB	CO CI 1000	Block Subtract Two Sets of Real or Complex Values
BMULR	CO CI 1001	Block Multiply Two Sets of Real Numbers
BMULRA	CO CI 1011	Block Multiply Two Sets of Real Numbers and Partially Add
General Logic Class		
BCONS	CO X 1010	Generate a Block of Constants (Zero or One)
LFLOW	CO CI 1100	Logical Flow-Through (Pass Data)
BAND	CO CI 1101	Block AND Two Sets of Integer Values
BOR	CO CI 1110	Block OR Two Sets of Integer Values
BXOR	CO CI 1111	Block Exclusive-OR Two Sets of Integer Values

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ELECTRICAL CHARACTERISTICS

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are performed after device case reaches operating temperature.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_C = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

A66110 COMMERCIAL ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR)

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

A66110 COMMERCIAL TEMPERATURE RANGE

Test Conditions:

T_C =0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66110B MIN	A66110B TYP	A66110B MAX	A66110A MIN	A66110A TYP	A66110A MAX	UNITS
Input High Voltage(V_{IH}):									
QUAD Pin		I	3.5		V_{cc}	3.5		V_{cc}	V
All Other Pins		I	2.4		V_{cc}	2.9		V_{cc}	V
Input Low Voltage(V_{IL})		I			0.6			0.6	V
Output High Voltage(V_{OH})	I_{OH}=-4.0mA	I	3.7			3.7			V
Output Low Voltage(V_{OL})	I_{OL}=4.0mA	I			0.6			0.6	V
Input High Leakage Current	V_{cc} Max	I			120			120	µA
Input Low Leakage Current	V_{cc} Max	I			-40			-40	µA
Hi-Z Output Leakage Current (Ioz)	V_{cc} Max, .6V <V_{OUT}<2.7V	I	-20		20	-20		20	µA
Operating Supply Current(I_{CC})	V_{cc} Max, f_{CI} Max	I		375	425			650	mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V,T_C=25°C	V		10			10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V,T_C=25°C	V		10			10		pF

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Test Conditions:

T_C =0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).
MUXRW=low, NFT=low, EN=high

AC ELECTRICAL PARAMETERS [7]	TEST CONDITIONS	TEST LEVEL	A66110B MIN	A66110B TYP	A66110B MAX	A66110A MIN	A66110A TYP	A66110A MAX	UNITS
CLKIN Frequency(f_{CI})	QUAD = low QUAD = high	I I			25 12.5			40 20	MHz
CLKIN Period(t_{CP})	QUAD = low QUAD = high	I I	40 80			25 50			nS
CLKIN Rise and Fall Time(t_{RF})		IV			10			10	nS
CLKIN Pulse Width(t_{PW})		I	16			11			nS
CLKIN to CLKOUT Delay(t_{CC})		I	2		13	2	5	8	nS
CLKIN to MCLKOUT Delay(t_{CM})		I	2		15	2	6	10	nS
SYNC Set-up Time(t_{ISS})		I	30			18			nS
SYNC Hold Time(t_{IHS})		I	1			0			nS
RDX16 Set-up Time (t_{ISR})		I	25			20			nS
RDX16 Hold Time (t_{IHR})		I	0			0			nS
RVDIR to Data Valid(t_{DD})		IV			35			25	nS
OE' to Data Out Delay(t_{DS})		IV			35			25	nS
OE' to Data Hi-Z(t_{AS})		IV			35			25	nS
D-Bus Input Set-up Time(t_{ISD})[1]		I	16			14			nS
D-Bus Input Hold Time(t_{IHD})[1]		I	3			3			nS
D-Bus CLKIN to Data Out Delay(t_{PD})[2]	QUAD = low QUAD = high	I I	9 9		35 35	9 9		26 30	nS
XD-Bus Input Set-up Time (t_{ISX})[3]		I	14			12			nS
XD-Bus Input Hold Time (t_{IHX})[3]		I	3			3			nS
COMP Input Set-up Time (t_{ISC})		I	30			11			nS
COMP Input Hold Time (t_{IHC})		I	3			3			nS
SCALE FACTOR INPUTS [4]									
Input Set-up Time (t_{ISF})		I	20			11			nS
Input Hold Time (t_{IHF})		I	0			0			nS
ARRAY MARKING INPUTS [5]									
Input Set-up Time (t_{ISM})		I	20			13			nS
Input Hold Time (t_{IHM})		I	0			0			nS
SCALE FACTOR AND OVERFLOW OUTPUTS [6]									
CLKIN to Data Out Delay (t_{PS})	QUAD = low QUAD = high	I I	6 6		35 35	6 6		26 30	nS

NOTES:
1. "D-bus" refers to D1, D2 busses when RVDIR=low, and D3, D4 busses when RVDIR=high.
2. "D-bus" refers to D1, D2 busses when RVDIR=high, and D3, D4 busses when RVDIR=low.
3. "XD-bus" refers to XD1 and XD2 busses.
4. The input pins in this group include SFI(2:0), XSFI, and ASFI(3:0).
5. The input pins in this group include BOP, EOP, and INITPR.
6. The output pins in this group include SFO(2:0), ASFO(3:0), OVF, OVFA, and OVFP.
7. For all output delay times, MIN values refer to the minimum time old outputs are valid after the rising edge of CLKIN before new outputs are valid (see switching waveforms).

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A66110 MILITARY ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR)

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

A66110 MILITARY TEMPERATURE RANGE

Test Conditions:

T_C=-55°C to +125°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66110B MIN	A66110B TYP	A66110B MAX	A66110A MIN	A66110A TYP	A66110A MAX	UNITS
Input High Voltage(V_{IH}):									
QUAD Pin		I				3.5		Vcc	V
All Other Pins		I				2.7		Vcc	V
Input Low Voltage(V_{IL})		I						0.6	V
Output High Voltage(V_{OH})	I_{OH}=-4.0mA	I				3.7			V
Output Low Voltage(V_{OL})	I_{OL}=4.0mA	I						0.6	V
Input High Leakage Current	V_{cc} Max	I						120	µA
Input Low Leakage Current	V_{cc} Max	I						-40	µA
Hi-Z Output Leakage Current (Ioz)	V_{cc} Max, .6V <V_{OUT}<2.7V	I				-20		20	µA
Operating Supply Current(I_{CC})	V_{cc} Max, f_{CI} Max	I						650	mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V,T_C=25°C	V					10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V,T_C=25°C	V					10		pF

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Test Conditions:

T_c=-55°C to +125°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).
MUXRW=low, NFT=low, EN=high

AC ELECTRICAL PARAMETERS [7]	TEST CONDITIONS	TEST LEVEL	A66110B MIN	A66110B TYP	A66110B MAX	A66110A MIN	A66110A TYP	A66110A MAX	UNITS
CLKIN Frequency(f_{CI})	QUAD=low QUAD=high	I I			25 12.5			35 17.5	MHz
CLKIN Period(t_{CP})	QUAD=low QUAD=high	I I	40 80			28.5 57			nS
CLKIN Rise and Fall Time(t_{RF})		IV						10	nS
CLKIN Pulse Width(t_{PW})		I				12			nS
CLKIN to CLKOUT Delay(t_{CC})		I				2		9	nS
CLKIN to MCLKOUT Delay(t_{CM})		I				2		12	nS
SYNC Set-up Time(t_{ISS})		I				19			nS
SYNC Hold Time(t_{IHS})		I				0			nS
RDX16 Set-up Time (t_{ISR})		I				21			nS
RDX16 Hold Time (t_{IHR})		I				0			nS
RVDIR to Data Valid(t_{DD})		IV						50	nS
OE' to Data Out Delay(t_{DS})		IV						50	nS
OE' to Data Hi-Z(t_{AS})		IV						50	nS
D-Bus Input Set-up Time(t_{ISD})[1]		I				16			nS
D-Bus Input Hold Time(t_{IHD})[1]		I				3			nS
D-Bus CLKIN to Data Out Delay(t_{PD})[2]	QUAD=low QUAD=high	I I				8 8		28 32	nS
XD-Bus Input Set-up Time (t_{ISX})[3]		I				13			nS
XD-Bus Input Hold Time (t_{IHX})[3]		I				3			nS
COMP Input Set-up Time (t_{ISC})		I				13			nS
COMP Input Hold Time (t_{IHC})		I				3			nS
SCALE FACTOR INPUTS [4]									
Input Set-up Time (t_{ISF})		I				13			nS
Input Hold Time (t_{IHF})		I				0			nS
ARRAY MARKING INPUTS [5]									
Input Set-up Time (t_{ISM})		I				14			nS
Input Hold Time (t_{IHM})		I				0			nS
SCALE FACTOR AND OVERFLOW OUTPUTS [6]									
CLKIN to Data Out Delay (t_{PS})	QUAD=low QUAD=high	I I				5 5		28 32	nS

NOTES:
1. "D-bus" refers to D1, D2 busses when RVDIR=low, and D3, D4 busses when RVDIR=high.
2. "D-bus" refers to D1, D2 busses when RVDIR=high, and D3, D4 busses when RVDIR=low.
3. "XD-bus" refers to XD1 and XD2 busses.
4. The input pins in this group include SFI(2:0), XSFI, and ASFI(3:0).
5. The input pins in this group include BOP, EOP, and INITPR.
6. The output pins in this group include SFO(2:0), ASFO(3:0), OVF, OVFA, and OVFP.
7. For all output delay times, MIN values refer to the minimum time old outputs are valid after the rising edge of CLKIN before new outputs are valid (see switching waveforms).

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A66111 COMMERCIAL ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR)

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

A66111 COMMERCIAL TEMPERATURE RANGE

Test Conditions:

T_C=0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66111B MIN	A66111B TYP	A66111B MAX	A66111A MIN	A66111A TYP	A66111A MAX	UNITS
Input High Voltage(V_{IH})		I	2.8		V_{cc}	2.9		V_{cc}	V
Input Low Voltage(V_{IL})		I			0.6			0.4	V
Output High Voltage(V_{OH})	I_{OH}=-4.0mA	I	3.2			3.2			V
Output Low Voltage(V_{OL})	I_{OL}=4.0mA	I			0.6			0.6	V
Input High Leakage Current	V_{cc} Max	I			120			120	µA
Input Low Leakage Current	V_{cc} Max	I			-40			-40	µA
Hi-Z Output Leakage Current (Ioz)	V_{cc} Max, .6V <V_{OUT}<2.7V	I	-20		20	-20		20	µA
Operating Supply Current(I_{CC})	V_{cc} Max, f_{CI} Max	I		375	425			650	mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V,T_C=25°C	V		10			10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V,T_C=25°C	V		10			10		pF

ARRAY MICROSYSTEMS 1420 Quail Lake Loop, Colorado Springs, CO 80906 Telephone: (719) 540-7900 FAX (719) 540-7950

Test Conditions:

T_c =0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature).
MUXRW=low, NFT=low, EN=high

AC ELECTRICAL PARAMETERS [7]	TEST CONDITIONS	TEST LEVEL	A66111B MIN	A66111B TYP	A66111B MAX	A66111A MIN	A66111A TYP	A66111A MAX	UNITS
CLKIN Frequency(f_{CI})		I			25			40	MHz
CLKIN Period(t_{CP})		I	40			25			nS
CLKIN Rise and Fall Time(t_{RF})		IV			10			10	nS
CLKIN Pulse Width(t_{PW})		I	0.4(t_{CP})			0.4(t_{CP})			nS
CLKIN to CLKOUT Delay(t_{CC})		I	2		15	2		11	nS
CLKIN to MCLKOUT Delay(t_{CM})		I	2		15	2		11	nS
SYNC Set-up Time(t_{ISS})		I	20			15			nS
SYNC Hold Time(t_{IHS})		I	0			0			nS
RDX16 Set-up Time (t_{ISR})		I	25			20			nS
RDX16 Hold Time (t_{IHR})		I	0			0			nS
RVDIR to Data Valid (t_{DD})		IV			35			25	nS
OE' to Data Out Delay (t_{DS})		IV			35			25	nS
OE' to Data Hi-Z (t_{AS})		IV			35			25	nS
D-Bus Input Set-up Time (t_{ISD}) [1]		I	16			14			nS
D-Bus Input Hold Time (t_{IHD}) [1]		I	1			1			nS
D-Bus CLKIN to Data Out Delay(t_{PD})[2]		I	8		30	8		26	nS
XD-Bus Input Set-up Time (t_{ISX}) [3]		I	16			14			nS
XD-Bus Input Hold Time (t_{IHX}) [3]		I	1			1			nS
COMP Input Set-up Time (t_{ISC})		I	16			14			nS
COMP Input Hold Time (t_{IHC})		I	1			1			nS
SCALE FACTOR INPUTS [4]									
Input Set-up Time (t_{ISF})		I	20			13			nS
Input Hold Time (t_{IHF})		I	0			0			nS
ARRAY MARKING INPUTS [5]									
Input Set-up Time (t_{ISM})		I	20			13			nS
Input Hold Time (t_{IHM})		I	0			0			nS
SCALE FACTOR AND OVERFLOW OUTPUTS [6]									
CLKIN to Data Out Delay (t_{PS})		I	6		30	6		26	nS

NOTES:
1. "D-bus" refers to D1, D2 busses when RVDIR=low, and D3, D4 busses when RVDIR=high.
2. "D-bus" refers to D1, D2 busses when RVDIR=high, and D3, D4 busses when RVDIR=low.
3. "XD-bus" refers to XD1 and XD2 busses.
4. The input pins in this group include SFI(2:0), XSFI, and ASFI(3:0).
5. The input pins in this group include BOP, EOP, and INITPR.
6. The output pins in this group include SFO(2:0), ASFO(3:0), OVF, OVFA, and OVFP.
7. For all output delay times, MIN values refer to the minimum time old outputs are valid after the rising edge of CLKIN before new outputs are valid (see switching waveforms).

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SWITCHING WAVEFORMS

FIGURE 1 - BEGINNING OF PASS TIMING (DUAL MODE)

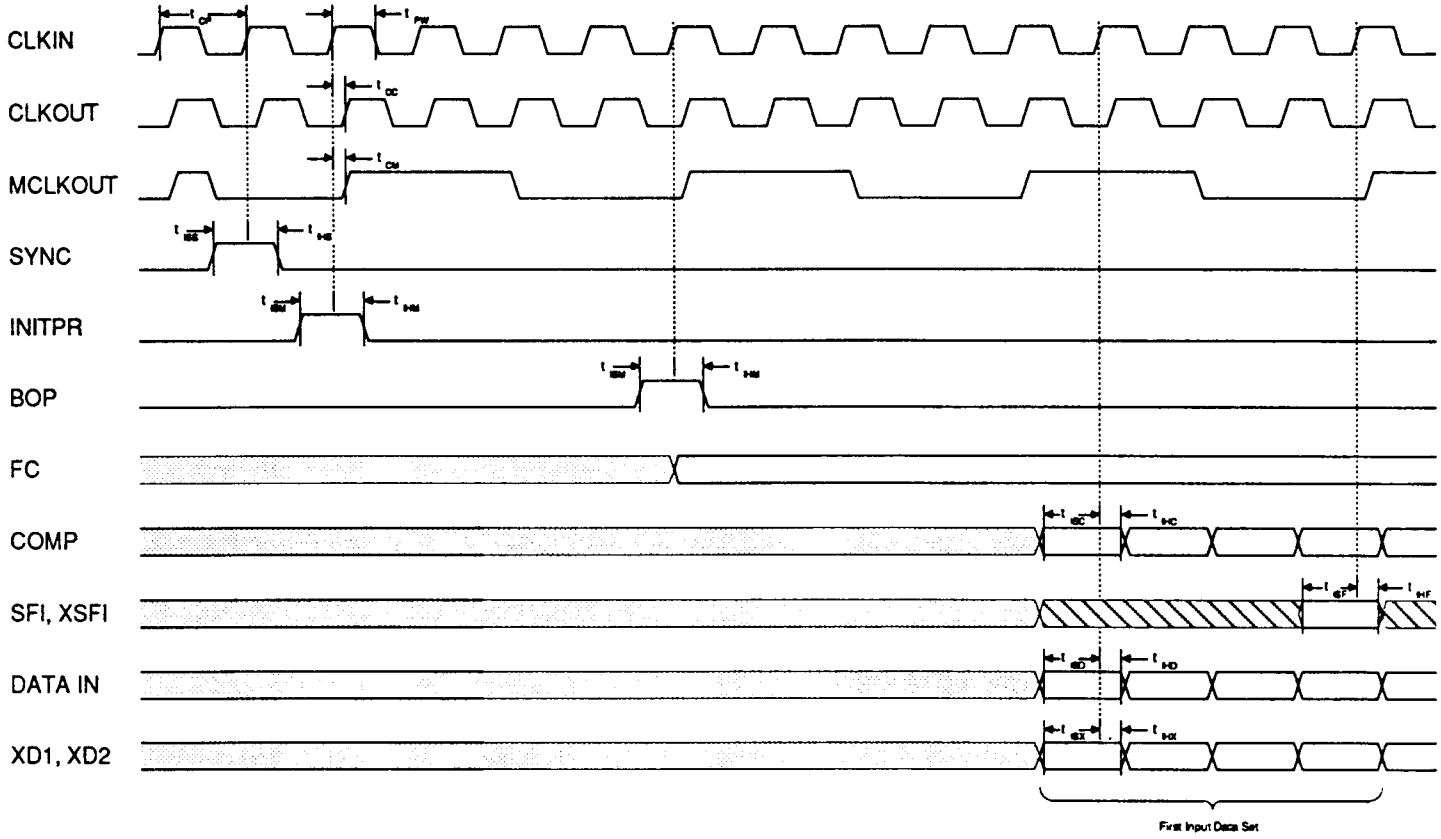

FIGURE 2 - BEGINNING OF PASS TIMING (QUAD MODE)

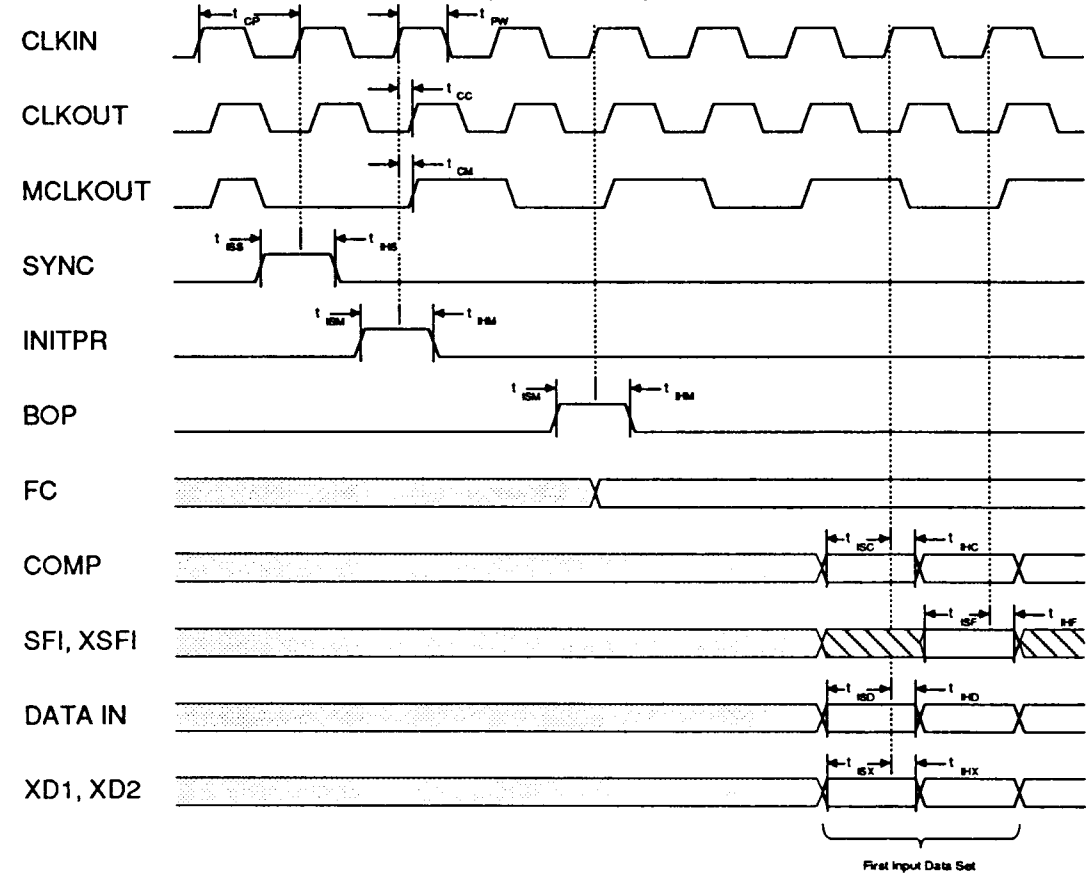

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FIGURE 3 - END OF PASS TIMING (DUAL MODE)

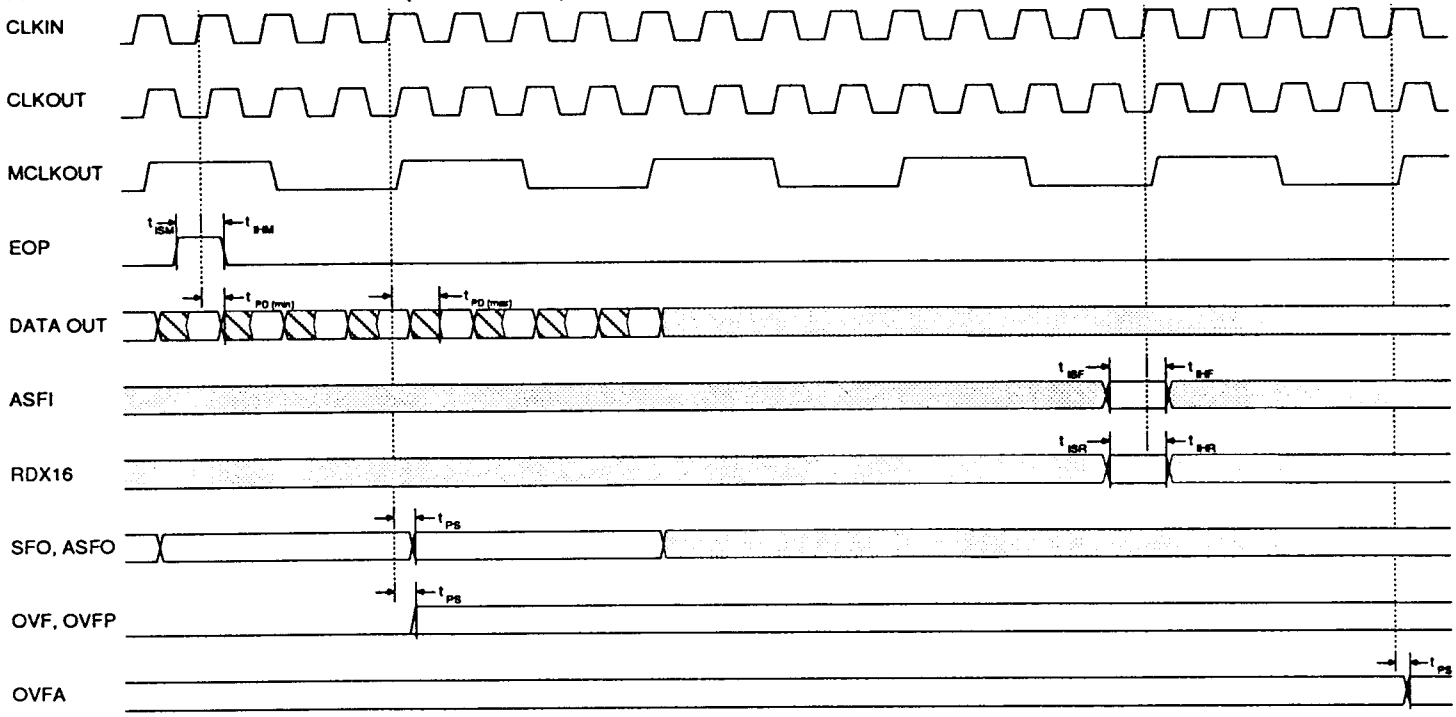


FIGURE 4 - END OF PASS TIMING (QUAD MODE)

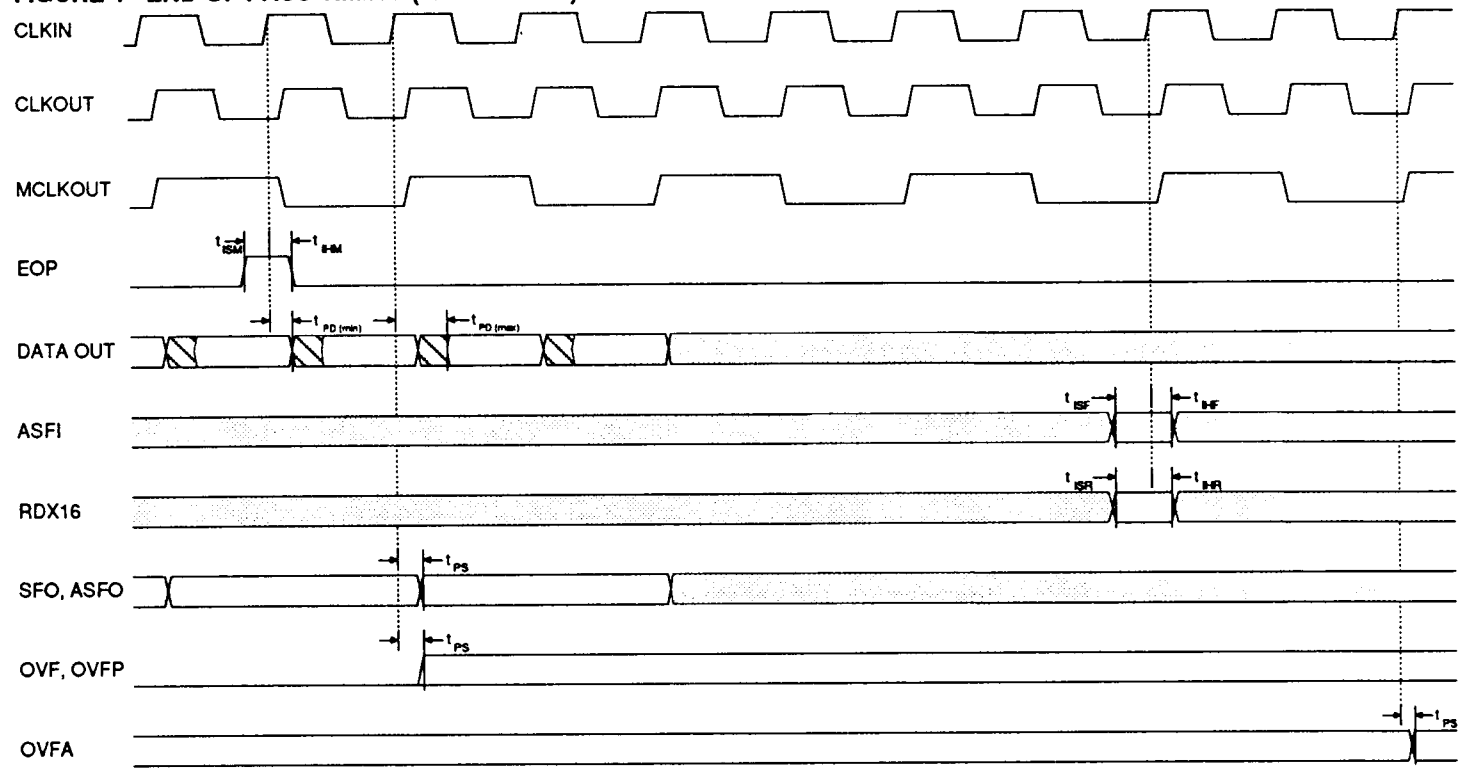
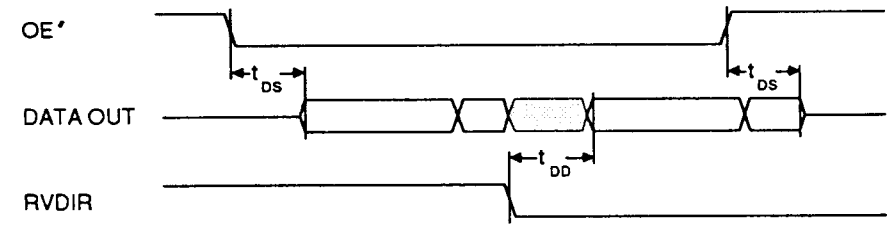


FIGURE 5 - OE' AND RVDIR TIMING



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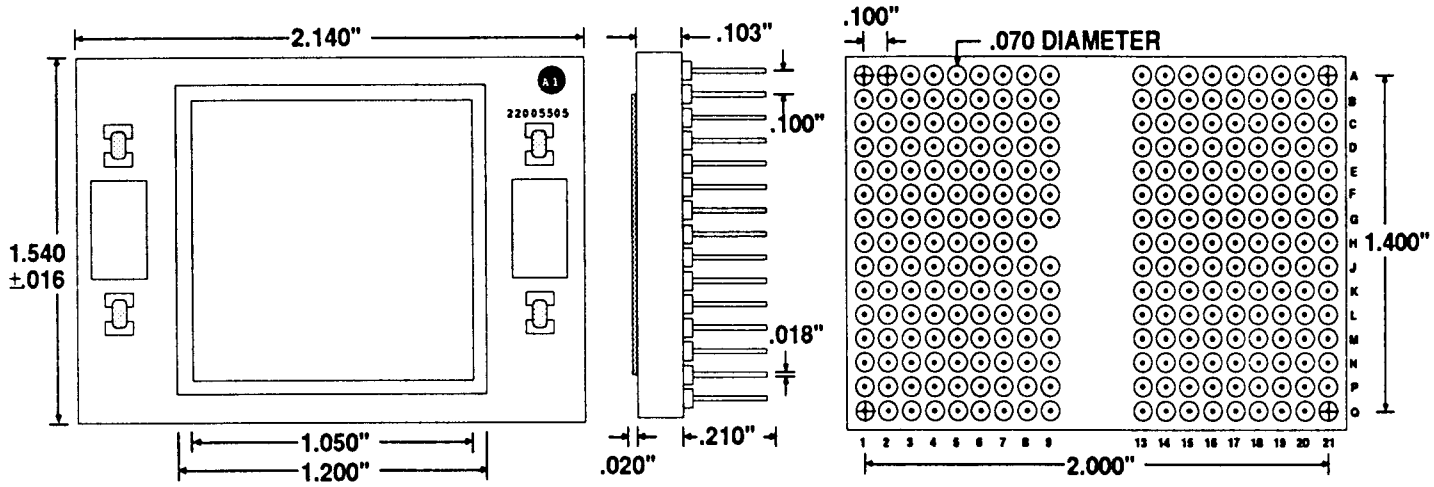
PACKAGING INFORMATION

A66110 Package Drawing



A66110 Pin Definitions

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED	
			QUAD MODE	DUAL MODE
DATA/AUX-DATA BUSES				
D1 (15:0)	I/O	I/O Data Bus	16	16
D2 (15:0)	I/O	I/O Data Bus	16	16
D3 (15:0)	I/O	I/O Data Bus	16	16
D4 (15:0)	I/O	I/O Data Bus	16	16
D5 (15:0)	I	Input Data Bus	16	None
D6 (15:0)	I	Input Data Bus	16	None
D7 (15:0)	O	Output Data Bus	16	None
D8 (15:0)	O	Output Data Bus	16	None
XD1 (15:0)	I	Input Aux Data Bus	16	16
XD2 (15:0)	I	Input Aux Data Bus	16	16
XD3 (15:0)	I	Input Aux Data Bus	16	None
XD4 (15:0)	I	Input Aux Data Bus	16	None
CONFIGURATION CONTROLS				
QUAD	I	Quad Bus Mode	1	1
MUXRW	I	Multiplexed Read Write (Single Memory System)	1	1
RVDIR	I	Reverses the Directionality of I/O Data Buses	1	1
OE'	I	Output Enable: Tristates All Data Buses if High	1	1
DATA CONTROLS				
FC (5:0)	I	Function - Code to Define Function	6	6
SFI (2:0)	I	Shift Input: Controls the Right Shift on Incoming Data	3	3
XSFI	I	Auxiliary Shift Input: Controls the Shift on Incoming Auxiliary Data	1	1
COMP (3:0)	I	Complement Control for the Input Data Buses	4	2
OVF/OVFP/ OVFA	O	Overflow Outputs from Internal Processors	3	3
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT				
SFO (2:0)	O	Scale Factor (SF) Output: Determines Scaling for the Next Pass	3	3
ASFI (3:0)	I	Accumulated SF Input	4	4
ASFO (3:0)	O	Accumulated SF Output	4	4

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED	
			QUAD MODE	DUAL MODE
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT (CONT.)				
INITPR	I	Initializes Scale Factor Processor	1	1
RDX16	I	Configures the Scale Factor Generator for Radix-16 Mode	1	1
TIMING CONTROLS				
CLKIN	I	Clock Input: At 4/Tm Frequency in Dual Bus Mode and 2/Tm Frequency in Quad Bus Mode	1	1
SYNC	I	System Clock Synchronization Signal	1	1
MCLKOUT	O	An Output Clock Signal at Machine Cycle Rate (Frequency 1/Tm)	1	1
CLKOUT	O	A Delayed Version of CLKIN, Compensated for Clock to Output Data Delay. Useful for Memory Writes.	1	1
BOP	I	Beginning of Pass Signal	1	1
EOP	I	End of Pass Signal	1	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)				
NFT	I	NFT in Progress	1	1
SIN	I	Serial Scan Input	1	1
SOUT	O	Serial Scan Output	1	1
NFTR	I	Reset Registers for NFT	1	1
NFTS	I	NFT Shift in Progress	1	1
EN	I	Enable Registers for Normal Operation	1	1
SUPPLY				
VCC	I	Voltage Supply	6	6
GND	I	Ground	6	6
TOTAL PINS USED ON THE PACKAGE			250	152

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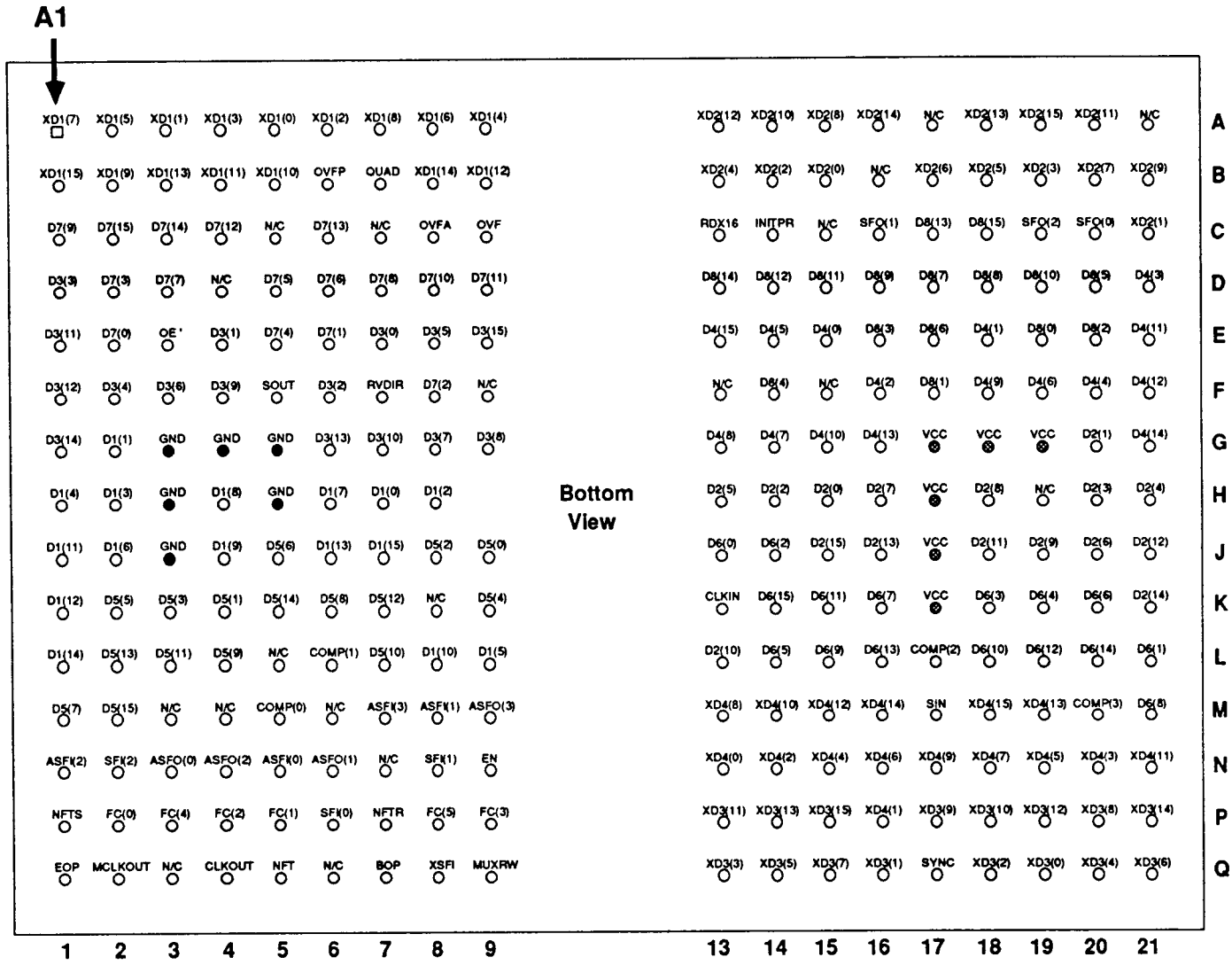
A66110 Pinout



ARRAY MICROSYSTEMS 1420 Quail Lake Loop, Colorado Springs, CO 80906 Telephone: (719) 540-7900 FAX (719) 540-7950

A66110 Pin Assignments

Pin Name	Pin #	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#
D1(0)	H7	D2(0)	H15	D3(0)	E7	D4(0)	E15
D1(1)	G2	D2(1)	G20	D3(1)	E4	D4(1)	E18
D1(2)	H8	D2(2)	H14	D3(2)	F6	D4(2)	F16
D1(3)	H2	D2(3)	H20	D3(3)	D1	D4(3)	D21
D1(4)	H1	D2(4)	H21	D3(4)	F2	D4(4)	F20
D1(5)	L9	D2(5)	H13	D3(5)	E8	D4(5)	E14
D1(6)	J2	D2(6)	J20	D3(6)	F3	D4(6)	F19
D1(7)	H6	D2(7)	H16	D3(7)	G8	D4(7)	G14
D1(8)	H4	D2(8)	H18	D3(8)	G9	D4(8)	G13
D1(9)	J4	D2(9)	J19	D3(9)	F4	D4(9)	F18
D1(10)	L8	D2(10)	L13	D3(10)	G7	D4(10)	G15
D1(11)	J1	D2(11)	J18	D3(11)	E1	D4(11)	E21
D1(12)	K1	D2(12)	J21	D3(12)	F1	D4(12)	F21
D1(13)	J6	D2(13)	J16	D3(13)	G6	D4(13)	G16
D1(14)	L1	D2(14)	K21	D3(14)	G1	D4(14)	G21
D1(15)	J7	D2(15)	J15	D3(15)	E9	D4(15)	E13
D5(0)	J9	D6(0)	J13	D7(0)	E2	D8(0)	E19
D5(1)	K4	D6(1)	L21	D7(1)	E6	D8(1)	F17
D5(2)	J8	D6(2)	J14	D7(2)	F8	D8(2)	E20
D5(3)	K3	D6(3)	K18	D7(3)	D2	D8(3)	E16
D5(4)	K9	D6(4)	K19	D7(4)	E5	D8(4)	F14
D5(5)	K2	D6(5)	L14	D7(5)	D5	D8(5)	D20
D5(6)	J5	D6(6)	K20	D7(6)	D6	D8(6)	E17
D5(7)	M1	D6(7)	K16	D7(7)	D3	D8(7)	D17
D5(8)	K6	D6(8)	M21	D7(8)	D7	D8(8)	D18
D5(9)	L4	D6(9)	L15	D7(9)	C1	D8(9)	D16
D5(10)	L7	D6(10)	L18	D7(10)	D8	D8(10)	D19
D5(11)	L3	D6(11)	K15	D7(11)	D9	D8(11)	D15
D5(12)	K7	D6(12)	L19	D7(12)	C4	D8(12)	D14
D5(13)	L2	D6(13)	L16	D7(13)	C6	D8(13)	C17
D5(14)	K5	D6(14)	L20	D7(14)	C3	D8(14)	D13
D5(15)	M2	D6(15)	K14	D7(15)	C2	D8(15)	C18
XD1(0)	A5	XD2(0)	B15	XD3(0)	Q19	XD4(0)	N13
XD1(1)	A3	XD2(1)	C21	XD3(1)	Q16	XD4(1)	P16
XD1(2)	A6	XD2(2)	B14	XD3(2)	Q18	XD4(2)	N14
XD1(3)	A4	XD2(3)	B19	XD3(3)	Q13	XD4(3)	N20
XD1(4)	A9	XD2(4)	B13	XD3(4)	Q20	XD4(4)	N15
XD1(5)	A2	XD2(5)	B18	XD3(5)	Q14	XD4(5)	N19
XD1(6)	A8	XD2(6)	B17	XD3(6)	Q21	XD4(6)	N16
XD1(7)	A1	XD2(7)	B20	XD3(7)	Q15	XD4(7)	N18
XD1(8)	A7	XD2(8)	A15	XD3(8)	P20	XD4(8)	M13
XD1(9)	B2	XD2(9)	B21	XD3(9)	P17	XD4(9)	N17
XD1(10)	B5	XD2(10)	A14	XD3(10)	P18	XD4(10)	M14
XD1(11)	B4	XD2(11)	A20	XD3(11)	P13	XD4(11)	N21
XD1(12)	B9	XD2(12)	A13	XD3(12)	P19	XD4(12)	M15
XD1(13)	B3	XD2(13)	A18	XD3(13)	P14	XD4(13)	M19
XD1(14)	B8	XD2(14)	A16	XD3(14)	P21	XD4(14)	M16
XD1(15)	B1	XD2(15)	A19	XD3(15)	P15	XD4(15)	M18
SFI(0)	P6	ASFI(0)	N5	SFO(0)	C20	ASFO(0)	N3
SFI(1)	N8	ASFI(1)	M8	SFO(1)	C16	ASFO(1)	N6
SFI(2)	N2	ASFI(2)	N1	SFO(2)	C19	ASFO(2)	N4
		ASFI(3)	M7			ASFO(3)	M9
FC(0)	P2	COMP(0)	M5	QUAD	B7	OVFA	C8
FC(1)	P5	COMP(1)	L6	CLKIN	K13	CLKOUT	Q4
FC(2)	P4	COMP(2)	L17	INITPR	C14	RVDIR	F7
FC(3)	P9	COMP(3)	M20	NFT	Q5	SYNC	Q17
FC(4)	P3			EN	N9	XSFI	Q8
FC(5)	P8	GND	G3	SOUT	F5	NFTR	P7
VCC	G17	GND	G4	SIN	M17	NFTS	P1
VCC	G18	GND	G5	MCLKOUT	Q2	OE'	E3
VCC	G19	GND	H3	OVFP	B6	OVF	C9
VCC	H17	GND	H5	MUXRW	Q9	EOP	Q1
VCC	J17	GND	J3	BOP	Q7	RDX16	C13
VCC	K17						

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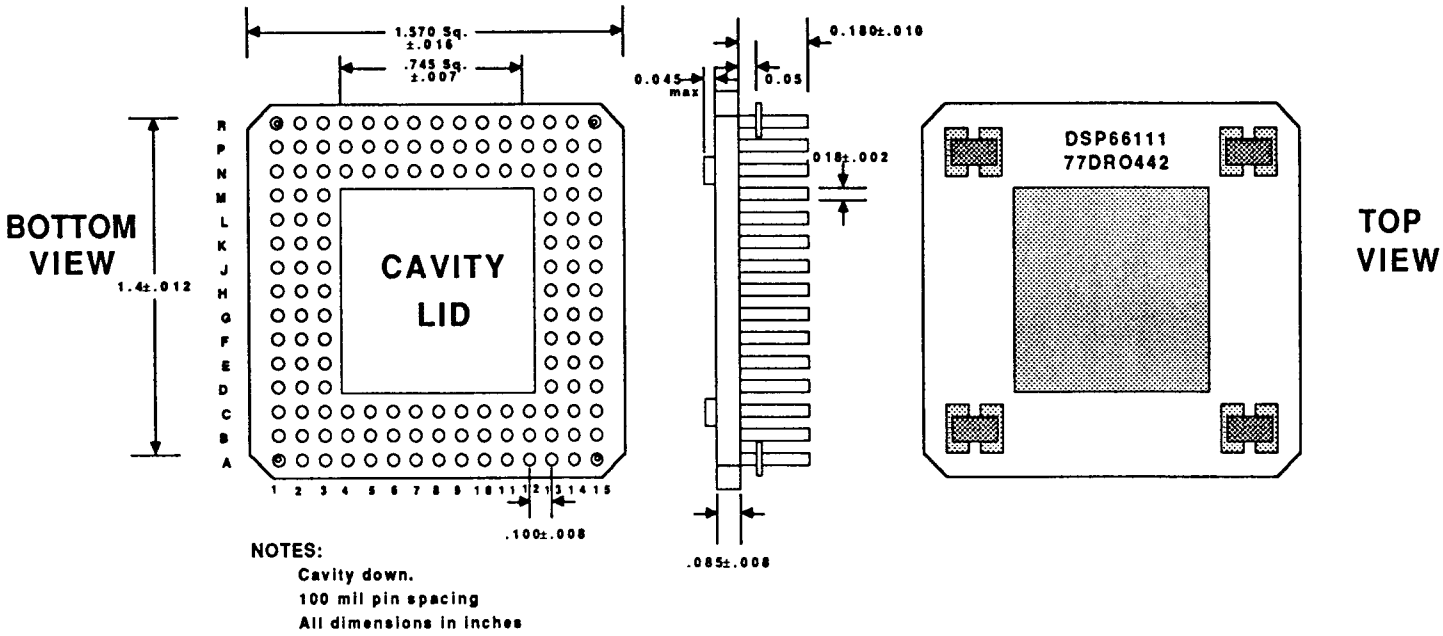
A66111 Package Drawing



NOTES:
Cavity down.
100 mil pin spacing
All dimensions in inches

A66111 Pin Definitions

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
DATA/AUX-DATA BUSES			
D1 (15:0)	I/O	I/O Data Bus	16
D2 (15:0)	I/O	I/O Data Bus	16
D3 (15:0)	I/O	I/O Data Bus	16
D4 (15:0)	I/O	I/O Data Bus	16
XD1 (15:0)	I	Input Aux Data Bus	16
XD2 (15:0)	I	Input Aux Data Bus	16
CONFIGURATION CONTROLS			
MUXRW	I	Multiplexed Read Write (Single Memory System)	1
RVDIR	I	Reverses the Directionality of I/O Data Buses	1
OE'	I	Output Enable: Tristates All Data Buses if High	1
DATA CONTROLS			
FC (5:0)	I	Function - Code to Define Function	6
SFI (2:0)	I	Shift Input: Controls the Right Shift on Incoming Data	3
XSFI	I	Auxiliary Shift Input: Controls the Shift on Incoming Auxiliary Data	1
COMP (1:0)	I	Complement Control for the Input Data Buses	2
OVF/OVFP/ OVFA	O	Overflow Outputs from Internal Processors	3
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT			
SFO (2:0)	O	Scale Factor (SF) Output: Determines Scaling for the Next Pass	3
ASFI (3:0)	I	Accumulated SF Input	4
ASFO (3:0)	O	Accumulated SF Output	4

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT (CONT.)			
INITPR	I	Initializes Scale Factor Processor	1
RDX16	I	Configures the Scale Factor Generator for Radix-16 Mode	1
TIMING CONTROLS			
CLKIN	I	Clock Input: At 4/Tm Frequency in Dual Bus Mode and 2/Tm Frequency in Quad Bus Mode	1
SYNC	I	System Clock Synchronization Signal	1
MCLKOUT	O	An Output Clock Signal at Machine Cycle Rate (Frequency 1/Tm)	1
CLKOUT	O	A Delayed Version of CLKIN, Compensated for Clock to Output Data Delay. Useful for Memory Writes.	1
BOP	I	Beginning of Pass Signal	1
EOP	I	End of Pass Signal	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)			
NFTR	I	Global Reset Registers	1
SUPPLY			
VCC	I	Voltage Supply	4
GND	I	Ground	5
TOTAL PINS USED ON THE PACKAGE			**143**

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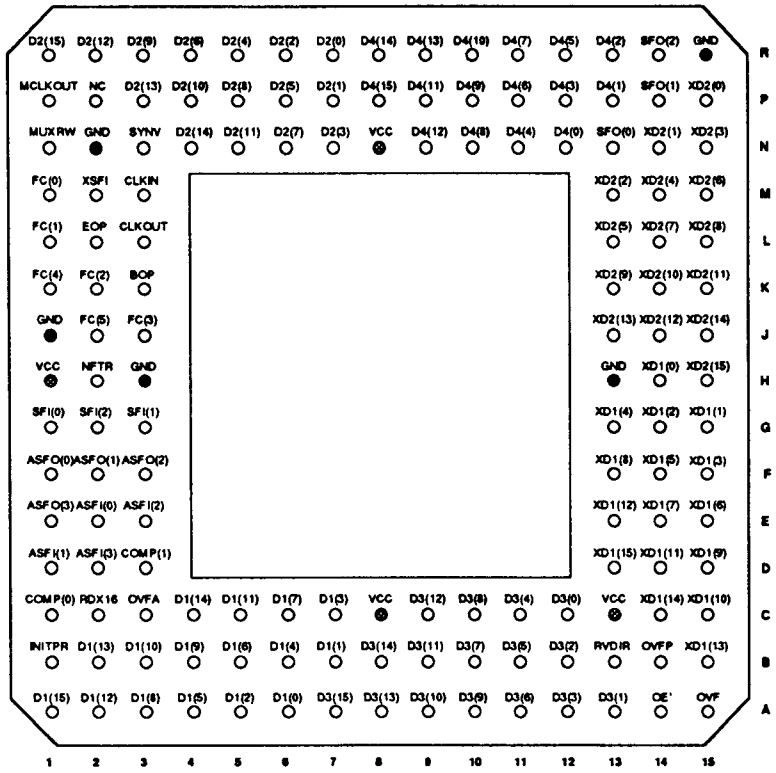
A66111 Pinout



Bottom View

A66111 Pin Assignments

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
D1(0)	A6	D2(0)	R7	D3(0)	C12	D4(0)	N12	XD1(0)	H14	XD2(0)	P15
D1(1)	B7	D2(1)	P7	D3(1)	A13	D4(1)	P13	XD1(1)	G15	XD2(1)	N14
D1(10)	B3	D2(10)	P4	D3(10)	A9	D4(10)	R10	XD1(10)	C15	XD2(10)	K14
D1(11)	C5	D2(11)	N5	D3(11)	B9	D4(11)	P9	XD1(11)	D14	XD2(11)	K15
D1(12)	A2	D2(12)	R2	D3(12)	C9	D4(12)	N9	XD1(12)	E13	XD2(12)	J14
D1(13)	B2	D2(13)	P3	D3(13)	A8	D4(13)	R9	XD1(13)	B15	XD2(13)	J13
D1(14)	C4	D2(14)	N4	D3(14)	B8	D4(14)	R8	XD1(14)	C14	XD2(14)	J15
D1(15)	A1	D2(15)	R1	D3(15)	A7	D4(15)	P8	XD1(15)	D13	XD2(15)	H15
D1(2)	A5	D2(2)	R6	D3(2)	B12	D4(2)	R13	XD1(2)	G14	XD2(2)	M13
D1(3)	C7	D2(3)	N7	D3(3)	A12	D4(3)	P12	XD1(3)	F15	XD2(3)	N15
D1(4)	B6	D2(4)	R5	D3(4)	C11	D4(4)	N11	XD1(4)	G13	XD2(4)	M14
D1(5)	A4	D2(5)	P6	D3(5)	B11	D4(5)	R12	XD1(5)	F14	XD2(5)	L13
D1(6)	B5	D2(6)	R4	D3(6)	A11	D4(6)	P11	XD1(6)	E15	XD2(6)	M15
D1(7)	C6	D2(7)	N6	D3(7)	B10	D4(7)	R11	XD1(7)	E14	XD2(7)	L14
D1(8)	A3	D2(8)	P5	D3(8)	C10	D4(8)	N10	XD1(8)	F13	XD2(8)	L15
D1(9)	B4	D2(9)	R3	D3(9)	A10	D4(9)	P10	XD1(9)	D15	XD2(9)	K13
CLKIN	M3	OVF	A15	FC(0)	M1	SFI(0)	G1	ASFI(0)	E2	VCC	C8
CLKOUT	L3	OVFA	C3	FC(1)	L1	SFI(1)	G3	ASFI(1)	D1	VCC	C13
MCLKOUT	P1	OVFP	B14	FC(2)	K2	SFI(2)	G2	ASFI(2)	E3	VCC	H1
SYNC	N3			FC(3)	J3	SFO(0)	N13	ASFI(3)	D2	VCC	N8
				FC(4)	K1	SFO(1)	P14	ASFO(0)	F1	GND	H3
INITPR	B1	OE'	A14	FC(5)	J2	SFO(2)	R14	ASFO(1)	F2	GND	H13
BOP	K3	MUXRW	N1	COMP(0)	C1			ASFO(2)	F3	GND	J1
EOP	L2	RDX16	C2	COMP(1)	D3			ASFO(3)	E1	GND	N2
		RVDIR	B13					XSFI	M2	GND	R15
		NFTR	H2							N/C	P2

ARRAY MICROSYSTEMS 1420 Quail Lake Loop, Colorado Springs, CO 80906 Telephone: (719) 540-7900 FAX (719) 540-7950

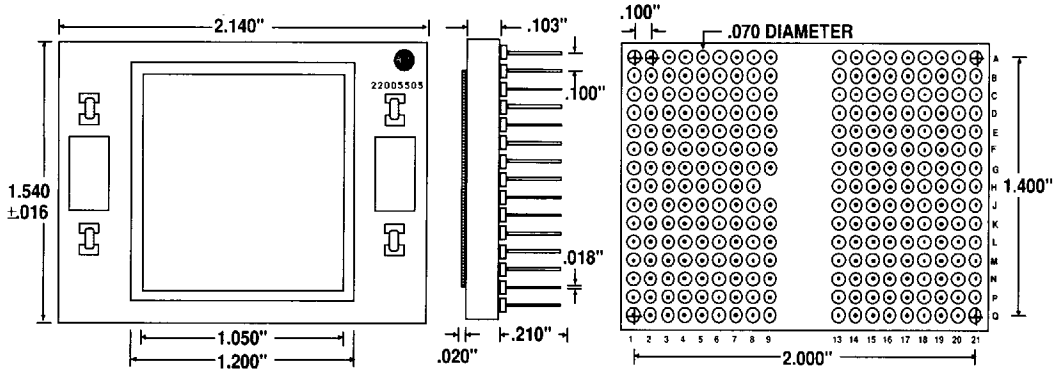
Ordering Information

Product Number	Speed Dual Mode	Speed Quad Mode	Temperature Range(Case)	Voltage Range	Number of Pins	Package Type
A66110BCG	25 MHz	12.5 MHz	0° C to +70° C	4.75V - 5.25V	269	Pin Grid Array
A66110BMG/H	25 MHz	12.5 MHz	-55° C to +125° C	4.75V - 5.25V	269	Pin Grid Array
A66110ACG	40 MHz	20 MHz	0° C to +70° C	4.75V - 5.25V	269	Pin Grid Array
A66110AMG/H	35 MHz	17.5 MHz	-55° C to +125° C	4.75V - 5.25V	269	Pin Grid Array
A66111BCG	25 MHz	-	0° C to +70° C	4.75V - 5.25V	144	Pin Grid Array
A66111ACG	40 MHz	-	0° C to 70° C	4.75V - 5.25V	144	Pin Grin Array

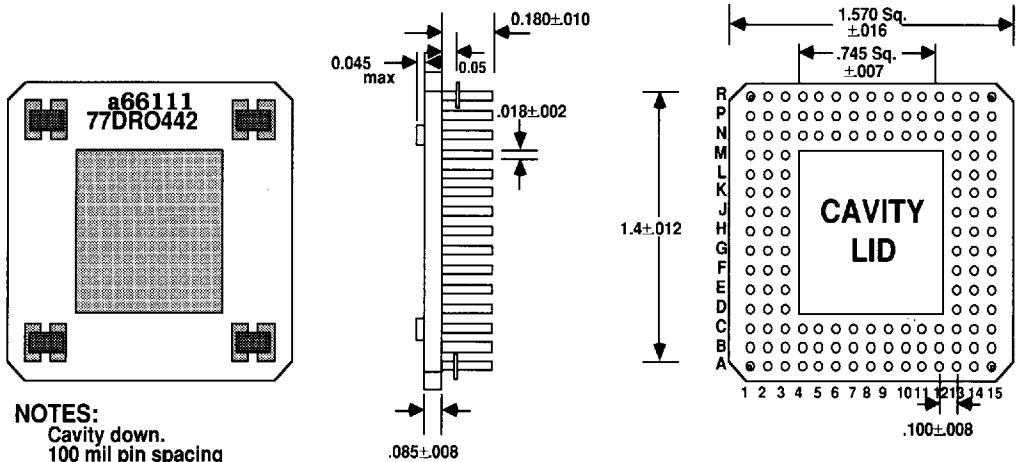
Package Drawings

T-90-20

a66110 DaSP (269 PGA)



a66111 DaSP (144 PGA)



NOTES:
Cavity down.
100 mil pin spacing
All dimensions in inches

a664XX Memory Module (92-pin Zip)