

MOS INTEGRATED CIRCUIT MC-422000LFB72F

3.3 V OPERATION 2 M-WORD BY 72-BIT DYNAMIC RAM MODULE HYPER PAGE MODE (EDO)

Description

The MC-422000LFB72F is a 2,097,152 words by 72 bits dynamic RAM module on which 9 pieces of 16 M DRAM: μ PD4217805L are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- Hyper page mode (EDO)
- 2,097,152 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode (EDO) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-422000LFB72-A60	60 ns	104 ns	25 ns	3.28 W	147.6 mW (CMOS level input)
MC-422000LFB72-A70	70 ns	124 ns	30 ns	2.95 W	

- 2,048 refresh cycles/32 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V \pm 0.3 V power supply

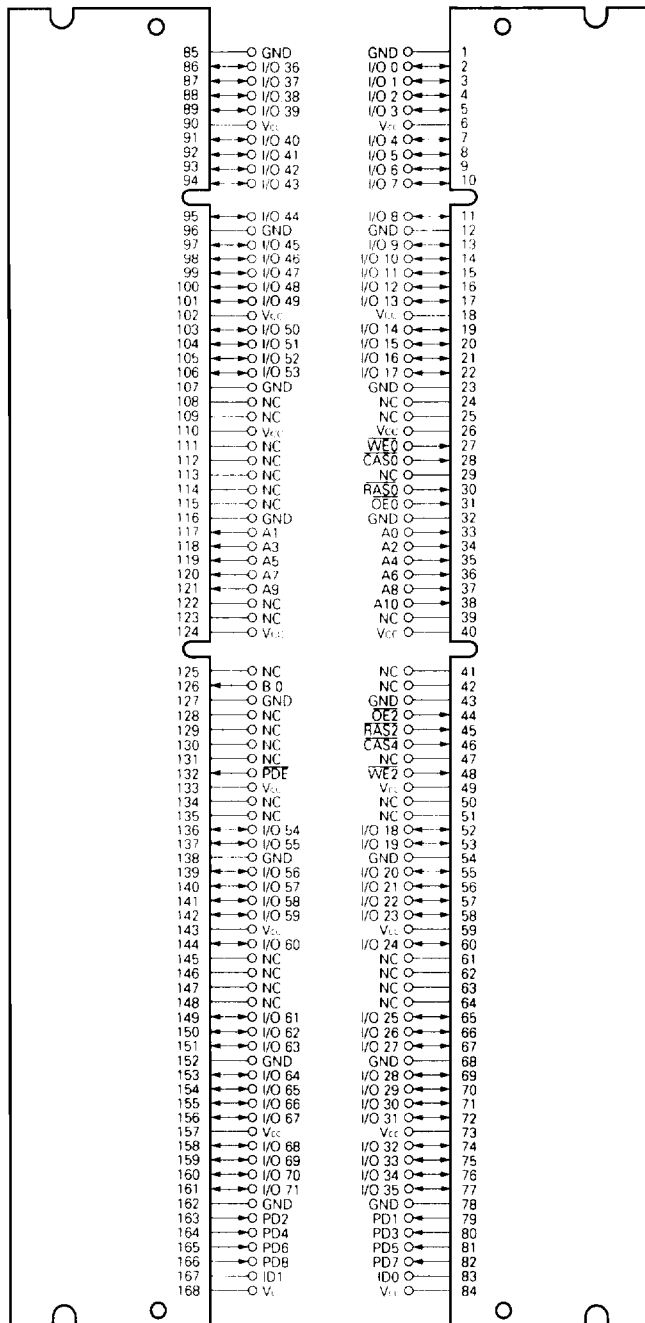
Ordering Information

Part number	Access time (MAX.)	Package	Mounted devices
MC-422000LFB72F-A60	60 ns	168-pin Dual In-line Memory Module (Socket Type)	9 pieces of μ PD4217805LG5 (400 mil TSOP(II))
MC-422000LFB72F-A70	70 ns	Edge connector: Gold plating	[Double side]

The information in this document is subject to change without notice.

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plating)



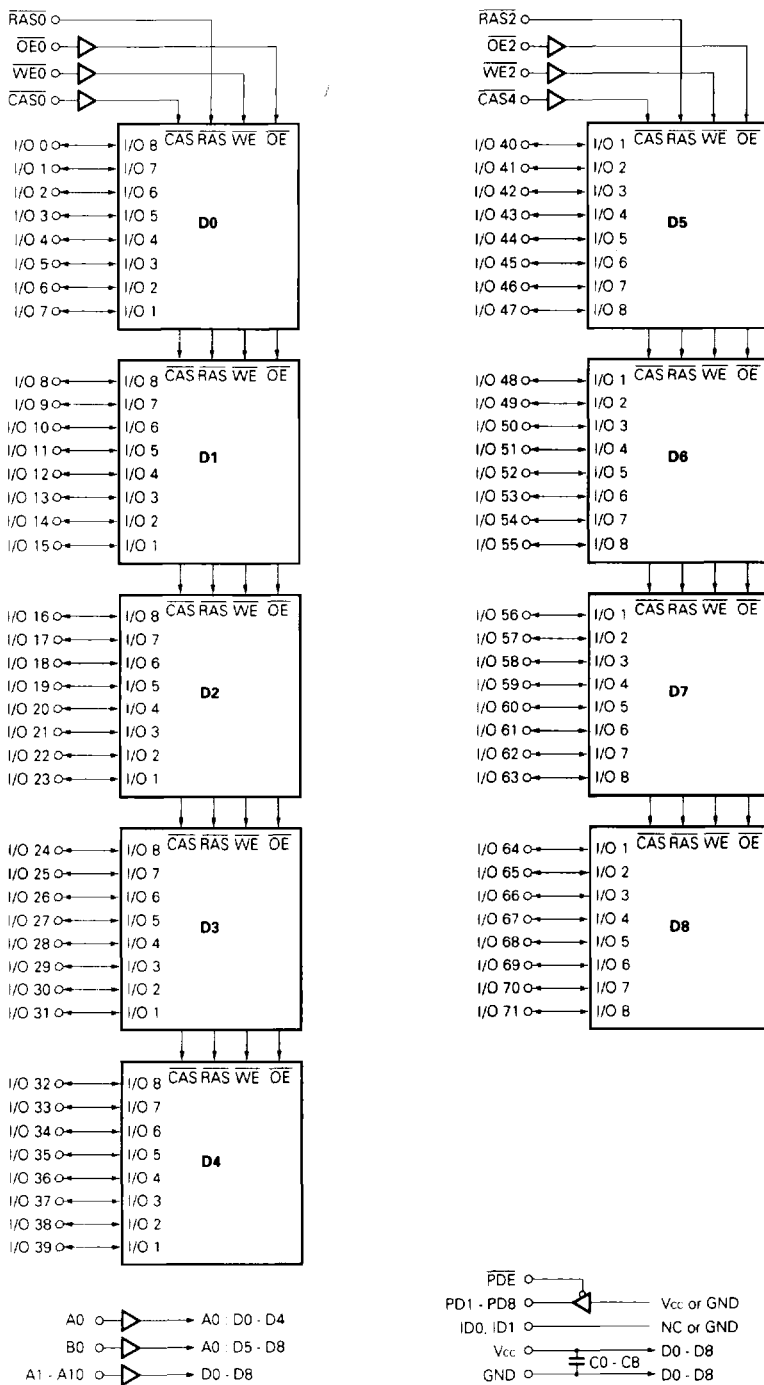
PD and ID Table

Pin Name	Pin No.	Access Time	
		60 ns	70 ns
PD1	79	H	H
PD2	163	L	L
PD3	80	L	L
PD4	164	H	H
PD5	81	H	H
PD6	165	H	L
PD7	82	H	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : VoH, L : VoL

- A0 - A10, B0 : Address Inputs
- I/O 0 - I/O 71 : Data Inputs/Outputs
- RAS0, RAS2 : Row Address Strobe
- CAS0, CAS4 : Column Address Strobe
- WE0, WE2 : Write Enable
- OE0, OE2 : Output Enable
- PDE : Presence Detect Enable
- PD1 - PD8 : Presence Detect Pins
- ID0, ID1 : Identity Pins
- Vcc : Power Supply
- GND : Ground
- NC : No connection

Block Diagram



Remark D0 - D8 : μ PD4217805L

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN)}$), wait more than 100 μs (\overline{RAS} , \overline{CAS} inactive) and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_I		-0.5 to +4.6	V
Supply voltage	V_{CC}		-0.5 to +4.6	V
Output current	I_O		20	mA
Power dissipation	P_D		11	W
Operating ambient temperature	T_A		0 to +70	$^{\circ}C$
Storage temperature	T_{STG}		-55 to +125	$^{\circ}C$

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		$V_{CC} + 0.3$	V
Low level input voltage	V_{IL}		-0.3		+0.8	V
Operating ambient temperature	T_A		0		70	$^{\circ}C$

Capacitance ($T_A = 25^{\circ}C$, $f = 1$ MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0-A10, B0			20	pF
	C_{I2}	$\overline{WE0}$, $\overline{WE2}$			20	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			50	
	C_{I4}	$\overline{CAS0}$, $\overline{CAS4}$			20	
	C_{I5}	$\overline{OE0}$, $\overline{OE2}$			20	
Data input/output capacitance	$C_{I/O}$	I/O0-I/O71			20	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

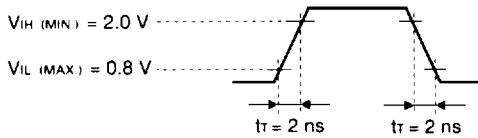
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}, I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	910	mA	1, 2, 3
			$t_{RAC} = 70 \text{ ns}$	820		
Standby current	I _{CC2}	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}$ $I_O = 0 \text{ mA}$		82	mA	
		$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ $I_O = 0 \text{ mA}$		41		
\overline{RAS} only refresh current	I _{CC3}	\overline{RAS} Cycling, $\overline{CAS} \geq V_{IH(MIN)}$ $t_{RC} = t_{RC(MIN)}, I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	910	mA	1, 2, 3, 4
			$t_{RAC} = 70 \text{ ns}$	820		
Operating current (Hyper page mode (EDO))	I _{CC4}	$\overline{RAS} \leq V_{IL(MAX)}, \overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN)}, I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	820	mA	1, 2, 5
			$t_{RAC} = 70 \text{ ns}$	730		
\overline{CAS} before \overline{RAS} refresh current	I _{CC5}	\overline{RAS} Cycling $t_{RC} = t_{RC(MIN)}, I_O = 0 \text{ mA}$	$t_{RAC} = 60 \text{ ns}$	910	mA	1, 2
			$t_{RAC} = 70 \text{ ns}$	820		
Input leakage current	I _{I(L)}	$V_I = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V	\overline{RAS}	-5	+5	μA
			Others	-5	+1	
Output leakage current	I _{O(L)}	$V_O = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage	V _{OH}	$I_O = -2.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_O = +2.0 \text{ mA}$		0.4	V	

- Notes**
- I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
 - Specified values are obtained with outputs unloaded.
 - I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX)}$ and $\overline{CAS} \geq V_{IH(MIN)}$.
 - I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 - I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

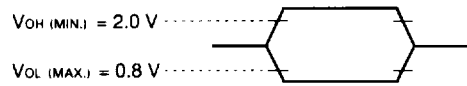
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

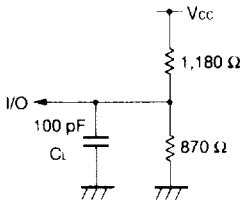
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{RC}	104	-	124	-	ns	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	-	50	-	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CPN}	10	-	10	-	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10,000	12	10,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	-	17	-	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	-	50	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	14	45	14	52	ns	1
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	30	12	35	ns	1
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	-	10	-	ns	2
Row Address Setup Time	t _{ASR}	5	-	5	-	ns	
Row Address Hold Time	t _{RAH}	10	-	10	-	ns	
Column Address Setup Time	t _{ASC}	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	10	-	12	-	ns	
$\overline{\text{OE}}$ Lead Time Referenced to $\overline{\text{RAS}}$	t _{OES}	0	-	0	-	ns	
$\overline{\text{CAS}}$ to Data Setup Time	t _{CLZ}	0	-	0	-	ns	
$\overline{\text{OE}}$ to Data Setup Time	t _{OLZ}	0	-	0	-	ns	
$\overline{\text{OE}}$ to Data Delay Time	t _{OED}	13	-	15	-	ns	
Transition Time (Rise and Fall)	t _r	1	50	1	50	ns	
Refresh Time	t _{REF}	-	32	-	32	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$
$t_{\text{RAD}} > t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{AA}(\text{MAX})}$	$t_{\text{RAD}} + t_{\text{AA}(\text{MAX})}$
$t_{\text{RCD}} > t_{\text{RCD}(\text{MAX})}$	$t_{\text{CAC}(\text{MAX})}$	$t_{\text{RCD}} + t_{\text{CAC}(\text{MAX})}$

$t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}(\text{MAX})}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \geq t_{\text{RCD}(\text{MAX})}$ will not cause any operation problems.

- $t_{\text{CRP}(\text{MIN})}$ requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.

Read Cycle

Parameter	Symbol	$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	-	60	-	70	ns	1
Access Time from $\overline{\text{CAS}}$	t_{CAC}	-	20	-	23	ns	1
Access Time from Column Address	t_{AA}	-	35	-	40	ns	1
Access Time from $\overline{\text{OE}}$	t_{OEA}	-	20	-	23	ns	
Column Address Lead Time Referenced to $\overline{\text{RAS}}$	t_{RAL}	30	-	35	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	0	-	0	-	ns	2
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{RCH}	0	-	0	-	ns	2
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	ns	3
$\overline{\text{CAS}}$ Hold Time to $\overline{\text{OE}}$	t_{CHO}	5	-	5	-	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$	$t_{\text{RAC}(\text{MAX})}$
$t_{\text{RAD}} > t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \leq t_{\text{RCD}(\text{MAX})}$	$t_{\text{AA}(\text{MAX})}$	$t_{\text{RAD}} + t_{\text{AA}(\text{MAX})}$
$t_{\text{RCD}} > t_{\text{RCD}(\text{MAX})}$	$t_{\text{CAC}(\text{MAX})}$	$t_{\text{RCD}} + t_{\text{CAC}(\text{MAX})}$

$t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}(\text{MAX})}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC} , t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{\text{RAD}} \geq t_{\text{RAD}(\text{MAX})}$ and $t_{\text{RCD}} \geq t_{\text{RCD}(\text{MAX})}$ will not cause any operation problems.

- Either $t_{\text{RCH}(\text{MIN})}$ or $t_{\text{RRH}(\text{MIN})}$ should be met in read cycles.
- $t_{\text{OEZ}(\text{MAX})}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL} .

Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
\overline{WE} Hold Time Referenced to \overline{CAS}	t _{WCH}	10	–	10	–	ns	1
\overline{WE} Pulse Width	t _{WP}	10	–	10	–	ns	1
\overline{WE} Lead Time Referenced to \overline{RAS}	t _{RWL}	15	–	17	–	ns	
\overline{WE} Lead Time Referenced to \overline{CAS}	t _{CWL}	10	–	12	–	ns	
\overline{WE} Setup Time	t _{WCS}	0	–	0	–	ns	2
\overline{OE} Hold Time	t _{OEH}	0	–	0	–	ns	
Data-in Setup Time	t _{DS}	0	–	0	–	ns	3
Data-in Hold Time	t _{DH}	10	–	10	–	ns	3

- Notes**
1. t_{WP}(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH}(MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS}(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS}(MIN.) and t_{DH}(MIN.) are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the \overline{WE} falling edge.

Read Modify Write Cycle

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t _{RWC}	148	–	172	–	ns	
\overline{RAS} to \overline{WE} Delay Time	t _{RWD}	87	–	99	–	ns	1
\overline{CAS} to \overline{WE} Delay Time	t _{CWD}	32	–	37	–	ns	1
Column Address to \overline{WE} Delay Time	t _{AWD}	52	–	59	–	ns	1

- Note**
1. If t_{WCS} ≥ t_{WCS}(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD}(MIN.), t_{CWD} ≥ t_{CWD}(MIN.), t_{AWD} ≥ t_{AWD}(MIN.) and t_{CPWD} ≥ t_{CPWD}(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode (EDO)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t _{HPC}	25	-	30	-	ns	1
$\overline{\text{RAS}}$ Pulse Width	t _{RASP}	60	125,000	70	125,000	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{H_{CAS}}	10	10,000	12	10,000	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	-	10	-	ns	
Access Time from $\overline{\text{CAS}}$ Precharge	t _{ACP}	-	40	-	45	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t _{CPWD}	52	-	59	-	ns	2
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	40	-	45	-	ns	
Read Modify Write Cycle Time	t _{HPRWC}	66	-	75	-	ns	
Data Output Hold Time	t _{DHC}	5	-	5	-	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Hold Time	t _{OCH}	5	-	5	-	ns	4
$\overline{\text{OE}}$ Precharge Time	t _{OEP}	5	-	5	-	ns	
Output Buffer Turn-off Delay from $\overline{\text{WE}}$	t _{WEZ}	0	13	0	15	ns	3,4
$\overline{\text{WE}}$ Pulse Width	t _{WPZ}	10	-	10	-	ns	4
Output Buffer Turn-off delay from $\overline{\text{RAS}}$	t _{OF_R}	0	13	0	15	ns	3,4
Output Buffer Turn-off delay from $\overline{\text{CAS}}$	t _{OF_C}	0	13	0	15	ns	3,4

Notes 1. t_{HPC}(MIN.) is applied to $\overline{\text{CAS}}$ access.

2. If t_{WCS} ≥ t_{WCS}(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD}(MIN.), t_{CWD} ≥ t_{CWD}(MIN.), t_{AWD} ≥ t_{AWD}(MIN.) and t_{CPWD} ≥ t_{CPWD}(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. t_{OFC}(MAX.), t_{OF_R}(MAX.) and t_{WEZ}(MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive (at the end of the read cycle)

$\overline{\text{WE}}$: inactive, $\overline{\text{OE}}$: active

t_{OFC} is effective when $\overline{\text{RAS}}$ is inactivated before $\overline{\text{CAS}}$ is inactivated.

t_{OF_R} is effective when $\overline{\text{CAS}}$ is inactivated before $\overline{\text{RAS}}$ is inactivated.

(2) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are active or either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ is active (in read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: inactive t_{WEZ} is effective.

(3) Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are inactive or $\overline{\text{RAS}}$ is active and $\overline{\text{CAS}}$ is inactive (at the end of read cycle)

$\overline{\text{WE}}$, $\overline{\text{OE}}$: active and either t_{RRH} or t_{RCH} must be met t_{WEZ} and t_{WPZ} are effective.

(4) $\overline{\text{WE}}$: inactive (in read cycle)

$\overline{\text{CAS}}$: inactive, $\overline{\text{OE}}$: active t_{CHO} is effective.

$\overline{\text{CAS}}$, $\overline{\text{OE}}$: active t_{OCH} is effective.

Refresh Cycle

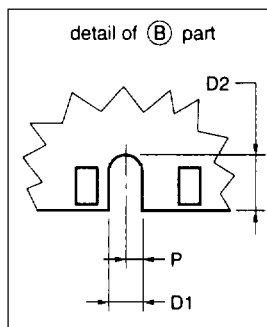
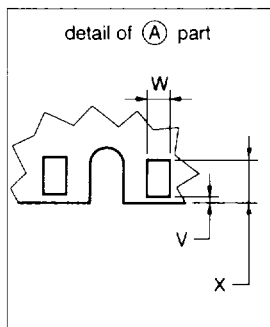
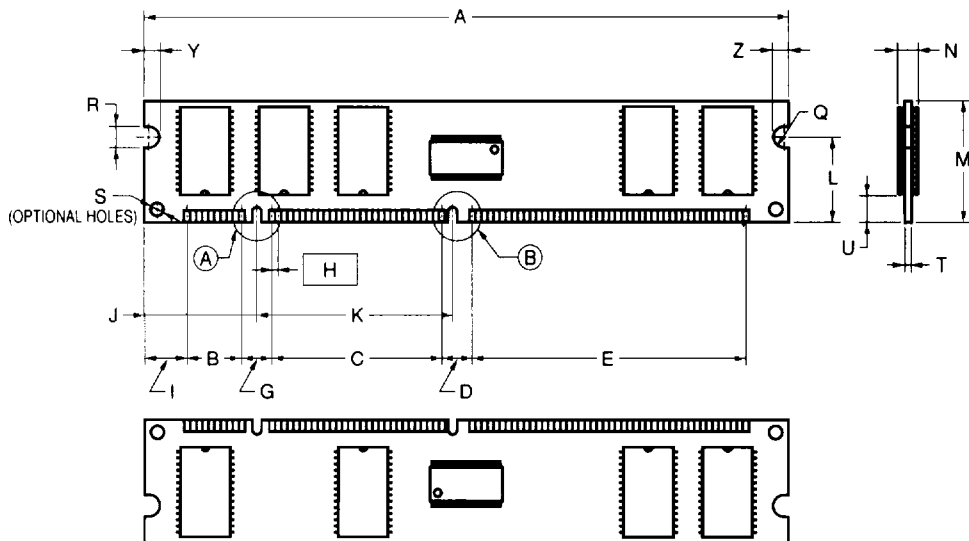
Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
CAS Setup Time	t _{CSR}	10	-	10	-	ns	
CAS Hold Time (CAS before RAS Refresh)	t _{CHR}	10	-	10	-	ns	
RAS Precharge CAS Hold Time	t _{RPC}	5	-	5	-	ns	
WE Setup Time	t _{WSR}	15	-	15	-	ns	
WE Hold Time	t _{WHR}	15	-	15	-	ns	

Timing Chart

Please refer to Timing Chart 2, page 381.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.26±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.50	0.925
K	43.18	1.70
L	17.78	0.700
M	25.4±0.13	1.000±0.006
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A6