MOS INTEGRATED CIRCUIT
μPD6452

12 LINE × 24 COLUMN ON-SCREEN CHARACTER DISPLAY CMOS LSI FOR S-VCR

DESCRIPTION

The μPD6452 is on-screen character display CMOS LSI which is combined with microcomputers and used for S-VCR to display program reserved information, chapter numbers, etc. on screens.

This product is most suitable for the S-VCR because composite video signal or component video singal (Y/C signals) can be input and output. Character format is 12 dots x 18 dots, and one character enables displaying numbers kanji and hiragana. And this LSI can generate video signal internally so that characters can be displayed without external signals.

NEC provides two standard types — μPD6452CS-002 and μPD6452GT-102. Using same characters, μPD6452CS-002 is a 24-pin shrink DIP and μPD6452 GT-102 is a 24-pin SOP package.

FEATURES

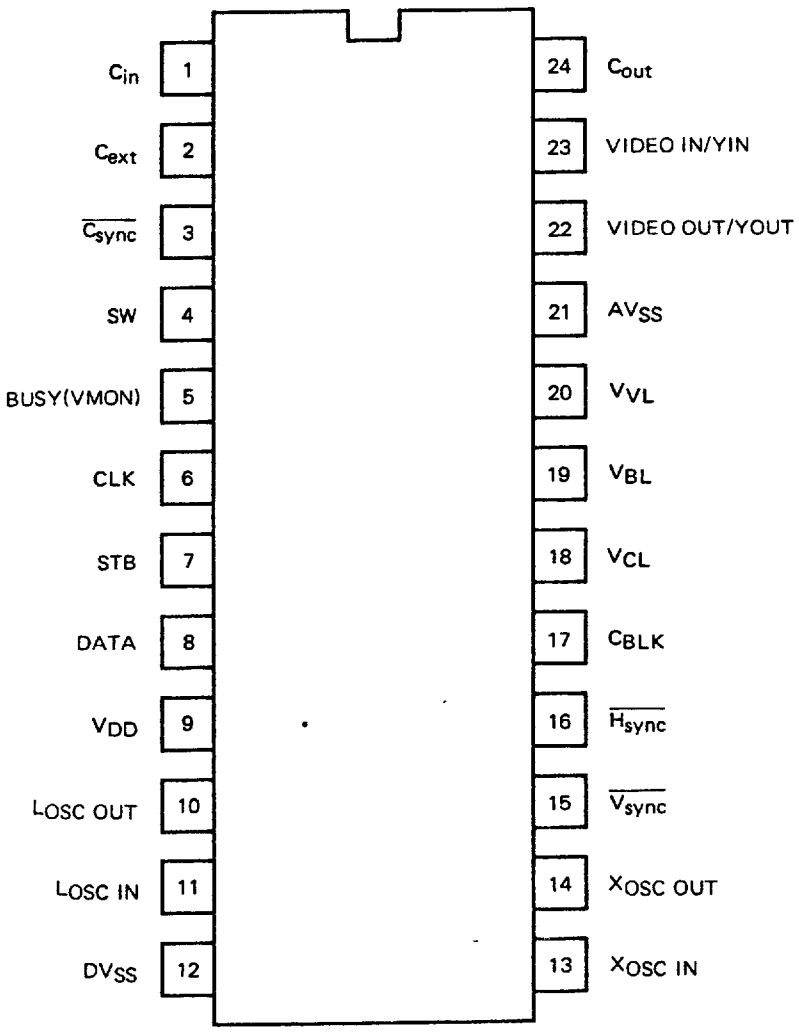
- Number of displayed character : 12 lines 24 columns
- Kinds of character : 128 (ROM)
- Character size : 1 dot-1H, 2H, 3H or 3H
- Dot matrix : 12 18 dots-with no clearance between neighboring characters
- Blinking ratio : 1:1, 3:1, or 1:3
- Input/Output of video signal : Composite video signal or Y/C signal
- Background : No background, black fringe, black square background, black solid background
- Internal video signal : Characters can be displayed on internal video signal (white, black, red, green, or blue) Internal video signal is noninterlaced video signal.
- Interface with microcomputer : 8-bit serial input format with BUSY signal
- Power supply : 5 V single
- Structure : Low-power-consumption CMOS

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPD6452CS-002	24 pin plastic shrink DIP (300 mil)
μPD6452GT-102	24 pin plastic SOP (375 mil)

Document No. IC-2624
(O. D. No. ID-8020)
Date Published July 1990 P

CONNECTION DIAGRAM (Top View)



Note: This bracket shows terminal arrangement for the mask code option when terminal 5 of μPD6452 is used for the synchronization protection monitor output (V_{MON})

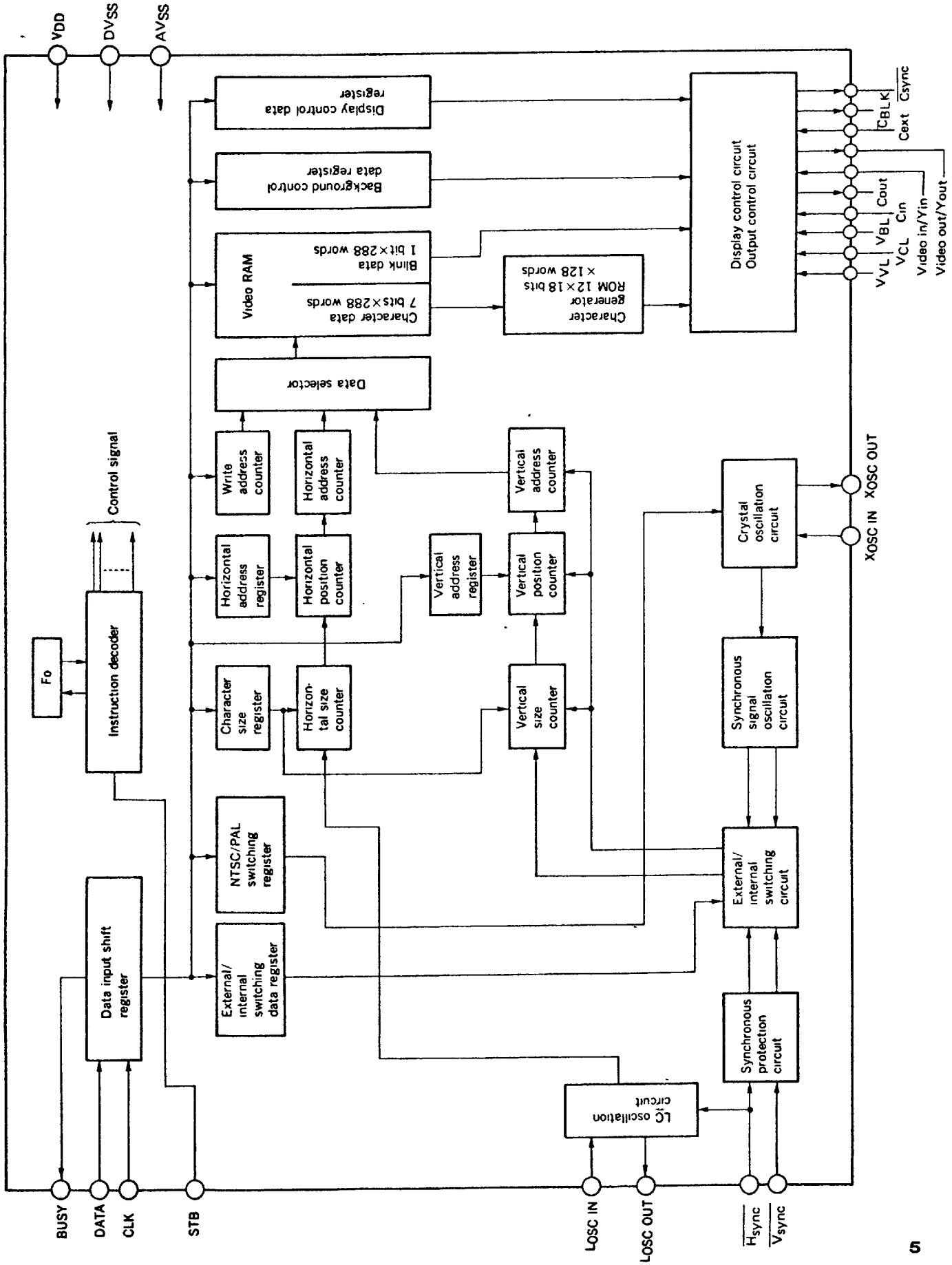
PIN DESCRIPTION

Pin No.	Symbol	Name	Function
1	C_{in}	C signal input termianl	This terminal is used to input component C signals.
2	C_{ext}	Cross color prevention capacitor terminal	This terminal is used to connect a cross color prevention capacitor.
3	$\overline{C_{sync}}$	Composite synchronous signal output terminal	This terminal is used to output a composite synchronous signal when an internal synchronous signal is generated (negative: synchronized).
4	SW	Composite/component switching input terminal	This terminal is used to input a component signal when the level becomes high; a composite signal when the level becomes low.
5	BUSY	BUSY signal output terminal	This output terminal is used to notify the microcomputer of whether a strobe signal may be input after input of serial data. When the level is low, a strobe signal may be input.
	V_{MON} Note	Synchronous protection monitor output terminal	This output terminal is used to output synchronous protection moniter output. (Mask code option)
6	CLK	Clock pulse input terminal	This terminal is used to input a clock signal for reading data. At the rising edge of a clock pulse, the data sent to the DATA terminal is input.
7	STB	Strobe signal input terminal	This input terminal is used to input a strobe signal after input of serial data. At the rising edge of the pulse sent to the STB terminal, 8-bit data is read.
8	DATA	Serial data input terminal	This terminal is used to input control data in sync. with the clock pulse applied to the CLK terminal.
9	V_{DD}	Power supply terminal	This terminal is used to supply +5 V.
10 11	$L_{OSC\ OUT}$ $L_{OSC\ IN}$	LC oscillation terminal	This terminal is used to connect the coil and capacitor of the dot clock frequency oscillator.
12	DV_{SS}	Digital ground terminal	This terminal is connected to the ground of the system.
13 14	$X_{OSC\ IN}$ $X_{OSC\ OUT}$	X'tal oscillation terminal	This is an X'tal oscillation terminal of the oscillator for generating an internal synchronous signal.
15	$\overline{V_{sync}}$	Vertical synchronous signal input terminal	This terminal is used to input a vertical synchronous signal (active low).
16	$\overline{H_{sync}}$	Horizontal synchronous signal input terminal	This terminal is used to input a vertical synchronous signal (active low). Oscillation occurs at the rising edge of the $\overline{H_{sync}}$ signal.
17	C_{BLK}	Color signal blanking signal output terminal	This terminal is used to output a blanking signal that cuts a video color signal during input of an external component signal.
18	V_{CL}	Character level adjusting terminal	This terminal is used to adjust the character signal level (white level).
19	V_{BL}	Background level adjusting terminal	This terminal is used to adjust the background signal level (black level).
20	V_{VL}	Internal video signal/Y-signal level adjusting terminal	This input terminal is used to adjust the level (sync chip level) of the generated internal video signal/Y-signal.
21	AV_{SS}	Analog ground terminal	This terminal is connected to the ground of the system.
22	VIDEO OUT/ YOUT	video/Y signal output terminal	The case of the internal mode: This terminal is used to output the composite video singal (SW=0) or the component Y signal (SW=1) mixed with the character signal. The case of the external mode: This terminal is used to output the composite video signal (SW=0) or the component Y signal (SW=1) mixed with the character signal. These composite video signal and Y signal are input from terminal 23 (Video in/Y in).
23	VIDEO IN/YIN	Video/Y signal input terminal	This terminal is used to input a composite video signal or component Y signal (negative: synchronized, positive: video).

Pin No.	Symbol	Name	Function
24	C_{out}	C signal output terminal	The case of the internal mode: This terminal is used to output the component C signal mixed with the character signal (SW=1). The output becomes open as inputting the composite video signal (SW=0). The case of the external mode: This terminal is used to output the component C signal mixed with the character signal (SW=1). This component C signal is input from terminal 1 (Cin). The output becomes open as inputting the composite video signal (SW=0).

Note: The BUSY output can be switched to the synchronous protection monitor output terminal (V_{MON}) with a mask code option.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	$V_{DD}-V_{SS}$	7	V
Input Voltage	V_{IN}	$V_{DD}+0.3 > V_{IN} > V_{SS}-0.3$	V
Output Voltage	V_{OUT}	$V_{DD}+0.3 > V_{OUT} > V_{SS}-0.3$	V
Operation Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C
Output Current	I_D	±5	mA

RECOMMENDED OPERATION RANGE

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	5.5	V
LC Oscillation Frequency	f_{osc}	4	7	10	MNz
Control Input High-level Voltage	V_{IH}	2.4			V
Control Input Low-level Voltage	V_{IL}			0.8	V
Synchronization Signal Input High-level Voltage	V_{IH}	2.4			V
Synchronization Signal Input Low-level Voltage	V_{IL}			0.8	V
External Vido Signal Input Voltage	V_i	0		V_{DD}	V
Character Signal Level Set Voltage	V_{CL}	0		V_{DD}	V
Background Signal Level Set Voltage	V_{BL}	0		V_{DD}	V
Internal Video Signal Level Set Voltage	V_{VL}	2.5		V_{DD}	V

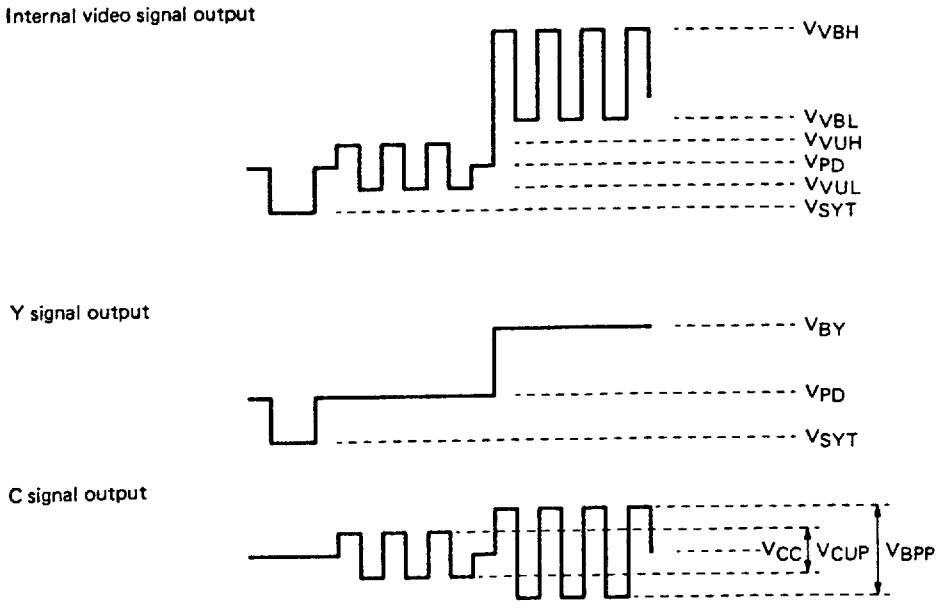
ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 5.0 V, V_{SS} = 0 V RH ≦ 70 %, L_{OSC} = 39/56 μH, C_{OUT} = 30 pF, C_{IN} = 5 to 30 pF)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Operating Voltage Range	V_{DD}-V_{SS}	4.5	5.0	5.5	V	f_{osc} = 10 MHz
Comsumed Current	I_{DD}			15	mA	f_{osc} = 10 MHz
Xtal Operating Oscillation Frequency (1)	f_{scn}		14.318180		MHz	NTSC mode
Xtal Operating Oscillation Frequency (2)	f_{scp}		17.734476		MHz	PAL mode
Control Output High-level Voltage (Note)	V_{OH}	4.5			V	I_O=–0.5 mA
Control Output Low-level Voltage (Note)	V_{OL}			0.5	V	I_O = 0.5 mA
Blue Background High-level Voltage (*)	V_{VBA}	1.56	1.73	1.90	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Blue Background Low-level Voltage (*)	V_{VBL}	1.16	1.29	1.42	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Color Burst High-level Voltage(*)	V_{VUH}	1.30	1.44	1.58	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Color Burst Low-level Voltage (*)	V_{VUL}	1.02	1.13	1.24	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Brightness Background Blue Level Voltage (*)	V_{BY}	1.35	1.50	1.65	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Blue Background Amplitude (*)	V_{BPP}	0.35	0.44	0.53	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Background Color Burst Amplitude (*)	V_{CUP}	0.35	0.44	0.53	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Color Center Level Voltage (*)	V_{CC}	1.13	1.25	1.38	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Pedestal Level Voltage (*)	V_{PD}	1.16	1.29	1.42	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V
Synchronous Level Voltage (*)	V_{SYT}	0.90	1.00	1.10	V	V_{DD} = 5.0 V, V_{VL} = 2.5 V

(*) INT mode signal output.
Note: Control output signals . . . . . BUSY, $\overline{C_{sync}}$, C_{BLK}.

This bracket shows terminal arrangement for the mask code option when terminal 5 of μPD6452 is used for the synchronization protection monitor output (V_{MON}).

INT mode output level



Type of Command

Control commands are eight-bit serial input types. Commands are executed by STB pulse input after serial input of eight-bit data. Before executing a program always issue a format reset command (format and Synchronous protection mode assignment command "FR = 1") to release the test mode.

COMMAND LIST FOR μPD6452

CONTENT	F_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Character Data	0	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Blink Data for Each Character	0	1	0	0	0	Blink	0	0	0
Character Display Line Address	0	1	0	0	1	AR_3	AR_2	AR_1	AR_0
Character Display Column Address	0	1	0	1	AC_4	AC_3	AC_2	AC_1	AC_0
Color Assignment for Background/ Internal Video Signal	0	1	1	0	BS_4	BS_3	R_V	G_V	B_V
Display ON/OFF, Blink, LC Oscillation Control	0	1	1	1	0	DO	BL_2	BL_1	L_{OSC}
NTSC/PAL Switching, External/Internal Video Switching, Crystal Oscillation Control	0	1	1	1	1	0	N/P	Ex/In	X_{OSC}
Format and Synchronous Protection Mode Assignment	X	1	1	1	1	1	FF	F_0	FR
Display Position Vertical Address	1	0	1	0	V_4	V_3	V_2	V_1	V_0
Display Position Horizontal Address	1	1	1	0	H_4	H_3	H_2	H_1	H_0
Character Size Assignment Note	1	1	0	S_5	S_4	AR_3	AR_2	AR_1	AR_0
Test Mode Set	1	1	1	1	0	T_3	T_2	T_1	T_0

Format Assignment and Format Reset (Test Mode Release)

Although commands for μPD6452 consist of nine bits, they are separated into two banks because serial interface shift register uses eight bits. Switching of banks is made by bit 1 (F_0) of the format assignment command.

Command for bank '0' (F_0 = 0)

- Displayed character data
- Blink data for each character
- Character display line address
- Character display column address
- Color assignment for background/internal video signal
- Display ON/OFF, Blink, LC Oscillation Control
- NTSC/PAL Switching, External/Internal Video Switching, Crystal Oscillation Control

Command for bank '1' (F_0 = 1)

- Display position vertical address
- Display position horizontal address
- Character size assignment
- Test mode set

Format Reset (Test Mode Release)

Setting bit 0 (F_R) of format and synchronous protection mode assignment command to "1" releases the test command mode and resets the following command. Since the test command mode stops normal commands from being received, always perform format reset to release test command mode before program execution. If format resetting is carried out during character display (display on), the display may be disturbed. Be sure to excute display off command before format resetting.

Reset Command

Size register ($AR_{0\text{-}3}$) on every row is set to "(S_5, S_4) = (0, 0)."
(Minimum size is assigned on every line.)

To release the test command mode without resetting the command above, use the test command mode release statement (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 1, 1, 1, 0, 0, 0, 0, 0).

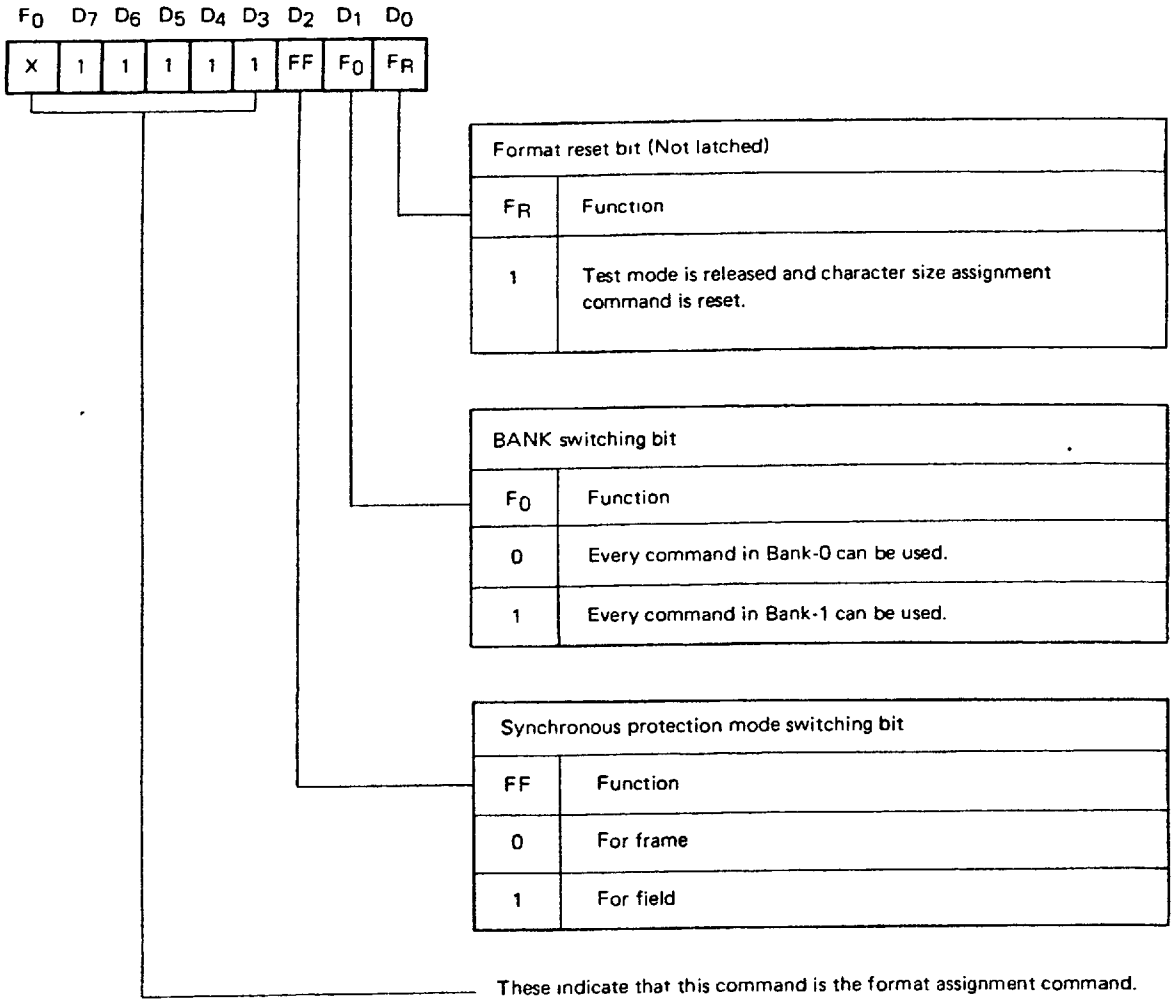
Synchronous protection mode

The Synchronous protection mode, "for frame" or "for field" may be selected with "format, synchronous protection mode assignment" command "FF".

"0" : for frame
"1" : for field

Please refer to the page 28 about synchronization protection.

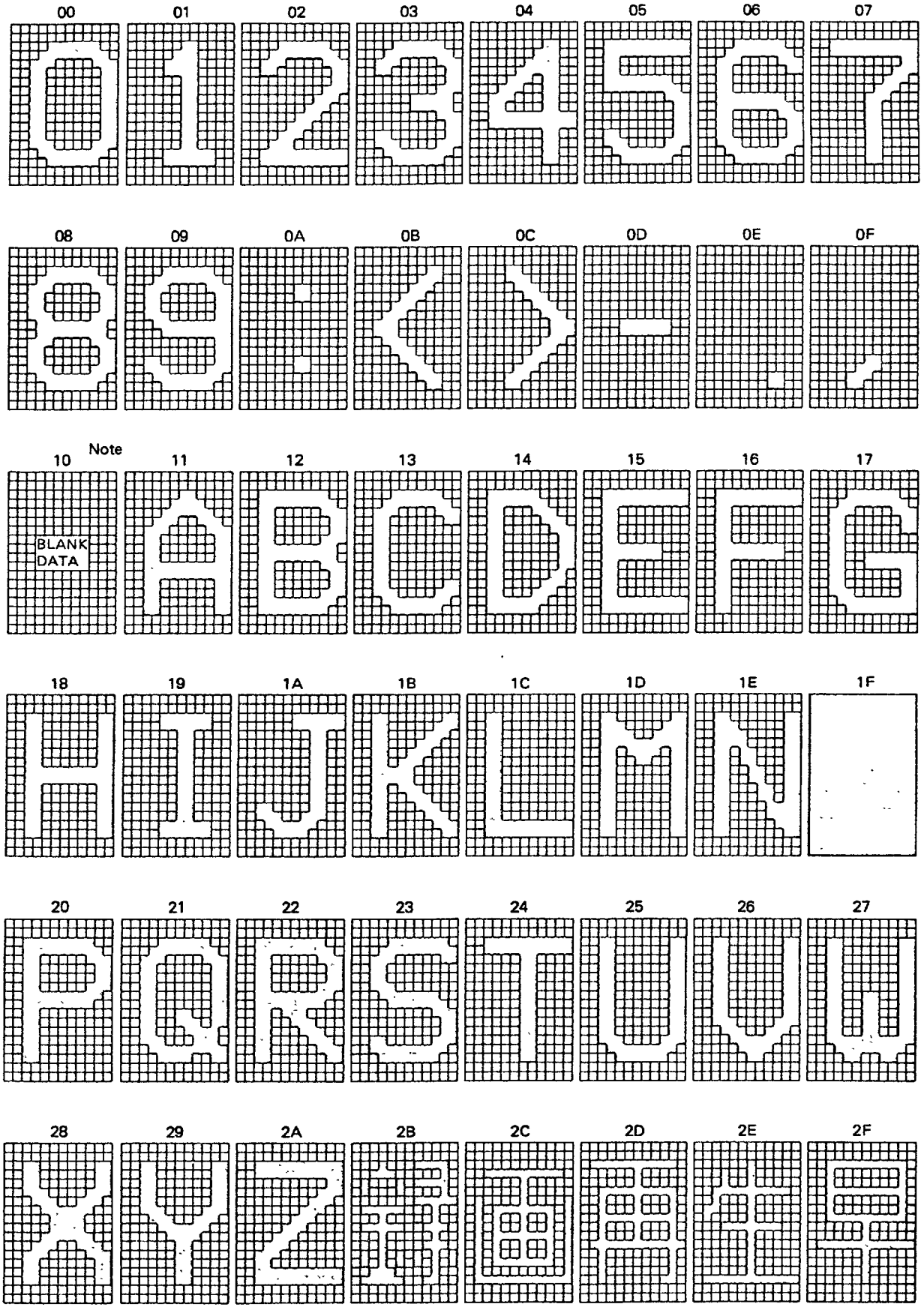
Format and Synchronous Protection Mode Assignment Command

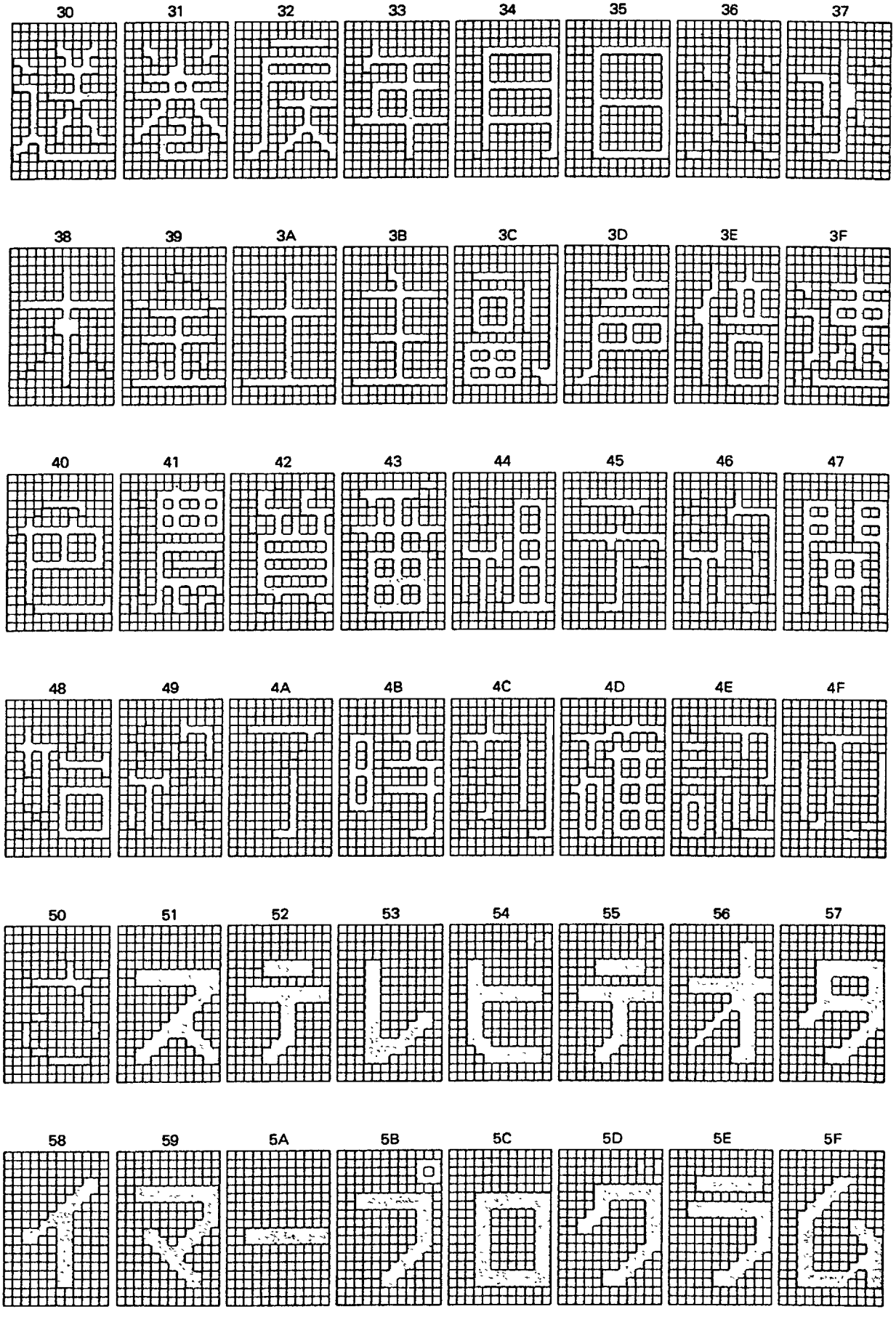


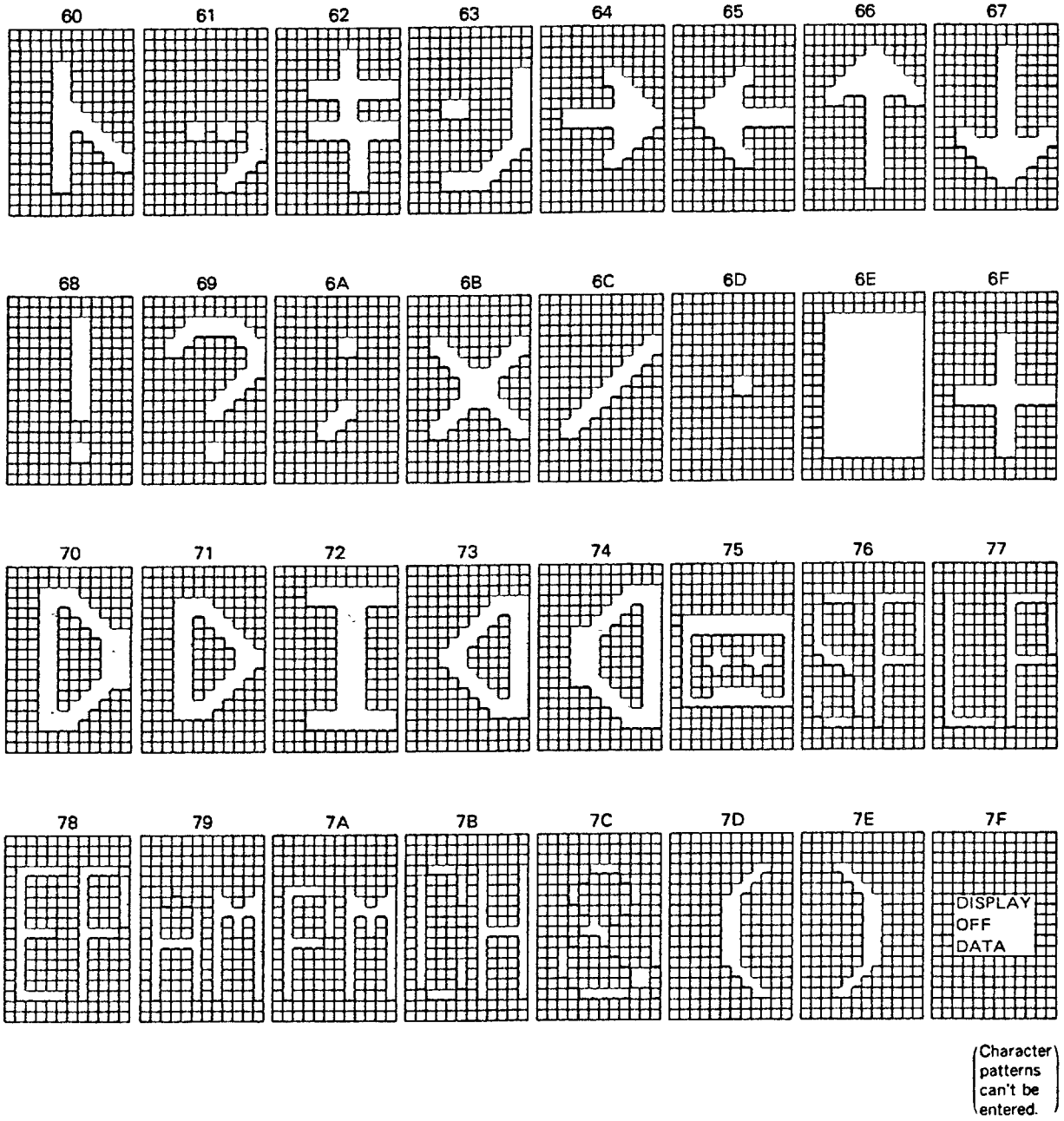
Character Patterns of μPD6452CS-002 and μPD6452GT-102

The μPD6452CS-002 and μPD6452GT-102 can display 128 character patterns (numbers, letters, kanji, etc.) as follows page11. Character codes 0H-7EH can be changed by mask code option. Character code 7FH is fixed on display OFF code, so that character patterns can't be entered. Although μPD6452CS-002 and μPD6452GT-102 have different package, the character patterns in character generator ROM are the same.

Character Patterns of μPD6452CS-002 & 6452GT-102




30
31
32
33
34
35
36
37
38
39
3A
3B
3C
3D
3E
3F
40
41
42
43
44
45
46
47
48
49
4A
4B
4C
4D
4E
4F
50
51
52
53
54
55
56
57
58
59
5A
5B
5C
5D
5E
5F



(Character patterns can't be entered.)

Note: In black block background and total black background mode, blank data (10H) generates background but no characters. DISPLAY OFF DATA (7FH) doesn't generate background or characters. If no-background or black trimmed character background mode is selected, BLANK DATA (10H) and DISPLAY OFF DATA (7FH) don't generate background or characters.

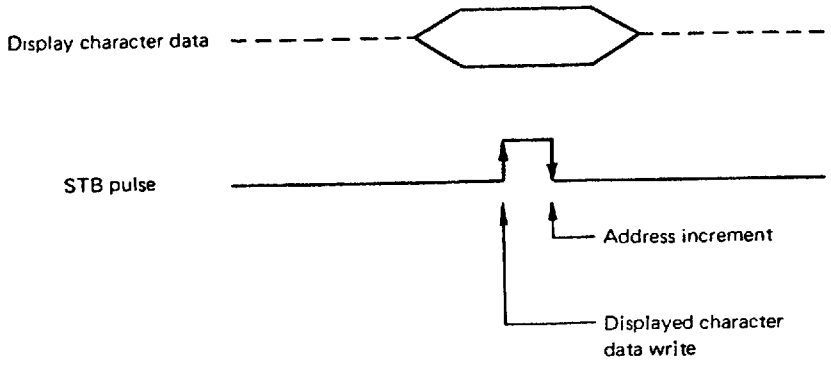
Character Display

There 12 lines by 24 columns of characters displayed (288 characters in all) as follows:

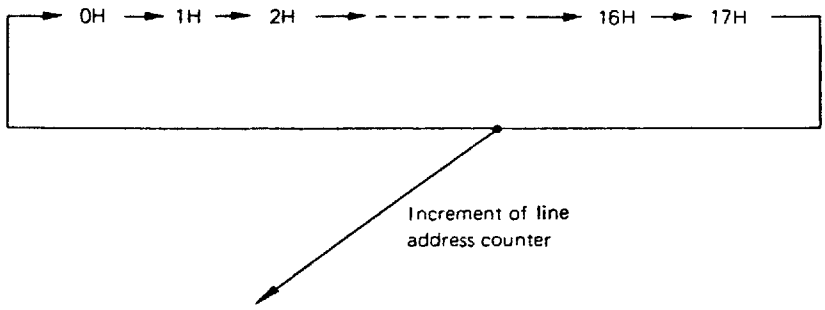
AC4, AC3 AC2 AC1, AC0	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101	10110	10111
AR3 AR2 AR1 AR0 0000																								
0001																								
0010																								
0011																								
0100																								
0101																								
0110																								
0111																								
1000																								
1001																								
1010																								
1011																								

Writing Displayed Character Data and Blink Data for Each Character

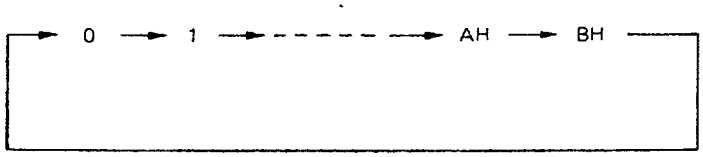
The data write address can be set directly into the address counter by the character display line address command and character display column address command. After setting write address, feed blink data for each character with the blink data command. Blink data is stored by character in an internal register. After that, input displayed character data with the displayed character data command. Blink data and displayed data which has been stored in an internal register is written in video RAM in synchronization with dot clock (signal) at the rise of the STB pulse input at the end of displayed character data command. The write address is incremented as follows after displayed data is written in video RAM. To continue to write displayed character data without changing blink data, input the displayed character data command.



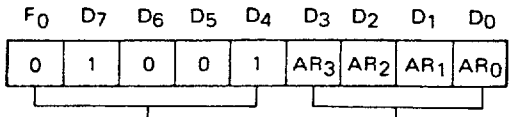
Column address counter $AC_4, AC_3, AC_2, AC_1, AC_0$



Line address counter AR_3, AR_2, AR_1, AR_0



Character Display Line Address Command

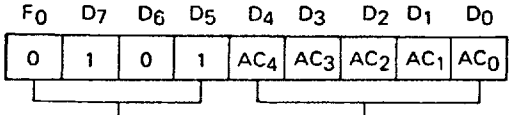


Row address assignment bit				
AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The first line is set.
0	0	0	1	The second line is set.
⌇				⌇
1	0	1	1	The 12th line is set.

Enter only addresses OH – BH.

These show that this command is the character display line address command.

Character Display Column Address Command

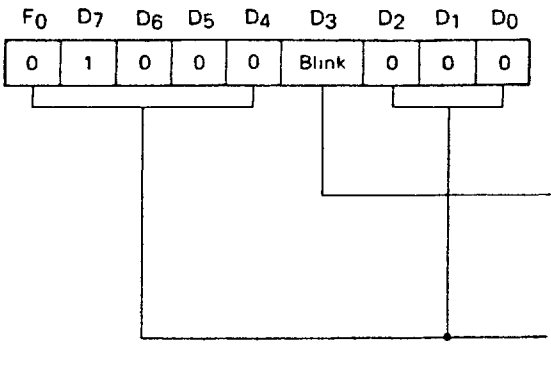


Column address assignment bit					
AC_4	AC_3	AC_2	AC_1	AC_0	Function
0	0	0	0	0	The first column is set.
0	0	0	0	1	The second column is set.
⌇					⌇
1	0	1	1	1	The 24th column is set.

Set only address 0H – 17H.

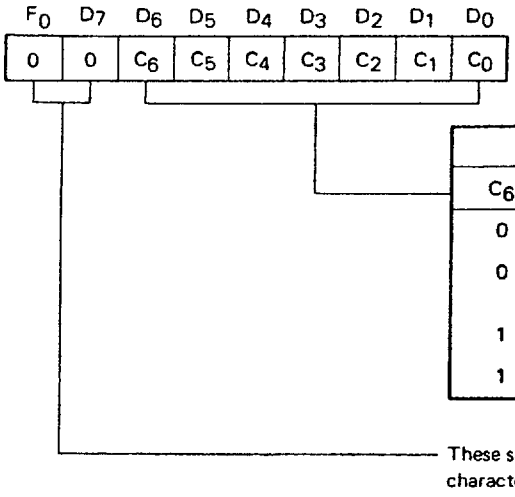
These show that this command is the character display column address command.

Blink Data Command for Each Character



Blink assignment bit for each character	
Blink	Function
0	No blinking
1	Blinking

Displayed Character Data Command



Character assignment bit							
C_6	C_5	C_4	C_3	C_2	C_1	C_0	Function
0	0	0	0	0	0	0	Data of character code 00H is output.
0	0	0	0	0	0	1	Data of character code 01H is output.
			⌇				⌇
1	1	1	1	1	1	0	Data of character code 7EH is output.
1	1	1	1	1	1	1	Display OFF data.

Turning Total Display ON or OFF

The display can be partially turned off with Blank data or display off data. The total display turned off with display ON/OFF, blink, and LC oscillation control commands. When display OFF is set with this command, characters and backgrounds are not output.

Display ON or OFF is executed in synchronization with $\overline{V_{sync}}$. A command transferred between the display ON/OFF command and V_{sync} is executed first.

If an attempt is made to transfer display OFF command data in the display-on state and write character data with a character data command before $\overline{V_{sync}}$ is input, the character data is written first in the display-on state.

Character Blinking

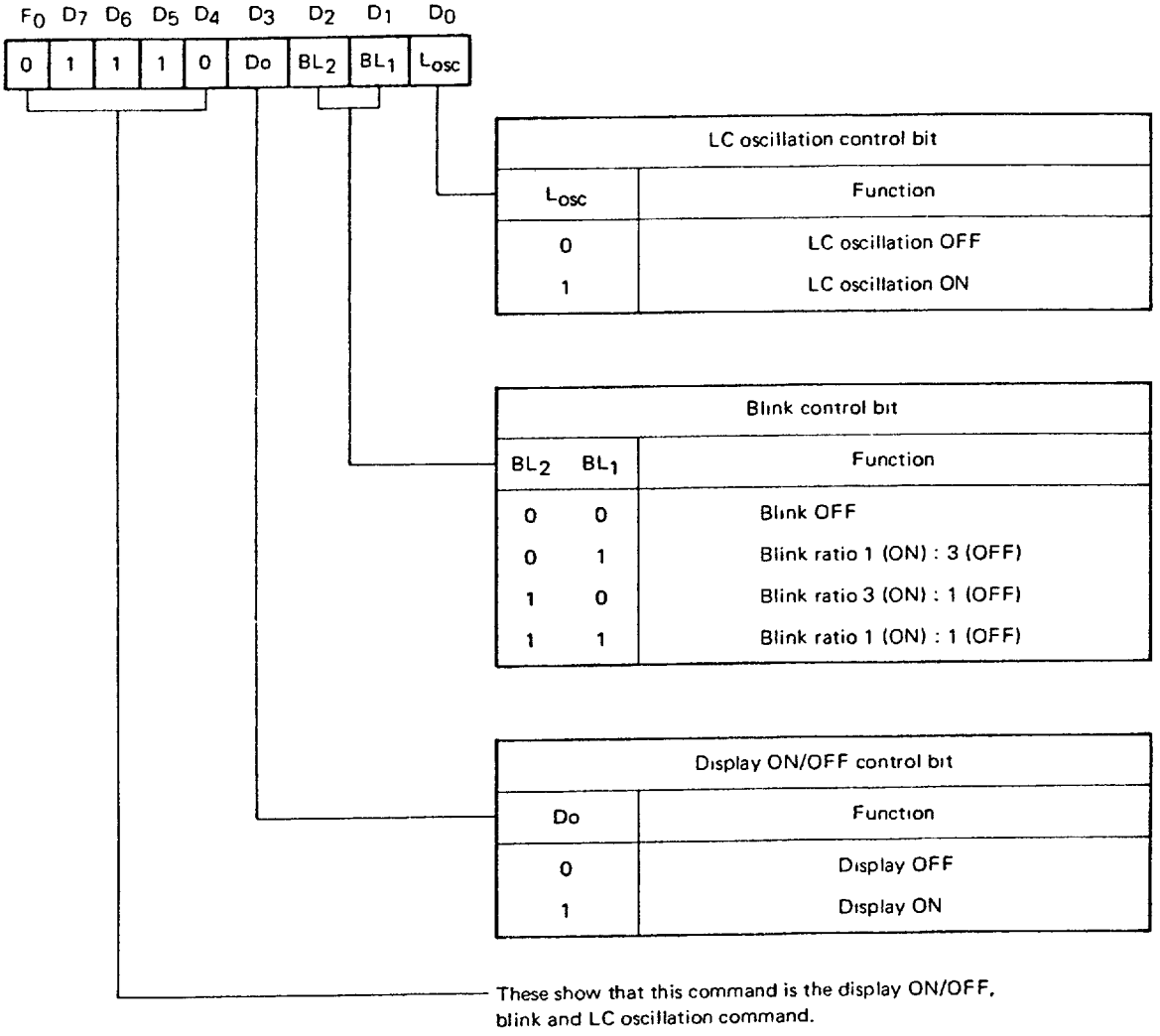
This IC enables blinking for each character with display ON/OFF, blink, and LC oscillation control commands. Blinking characters are determined with the character blink data command. The blinking period is about 1 second (64 times longer than 1 vertical cycle), and three blinking ratios (1:1, 3:1, and 1:3) are available.

LC Oscillation Control

Since this IC enables control of LC oscillation with display ON/OFF, blink, and LC oscillation control commands, oscillation can be suspended while characters aren't displayed, so that power can be saved. Since character output isn't reliable after suspension of oscillation, set the display ON/OFF control bit (Do) to "0" (display OFF).

Note: When display is ON, the oscillation synchronizes $\overline{H_{sync}}$, so the oscillation is stopping at the low level term of $\overline{H_{sync}}$. When display is OFF, the oscillation keeps on irrespective of $\overline{H_{sync}}$.

Display ON/OFF, Blink, and LC Oscillation Commands



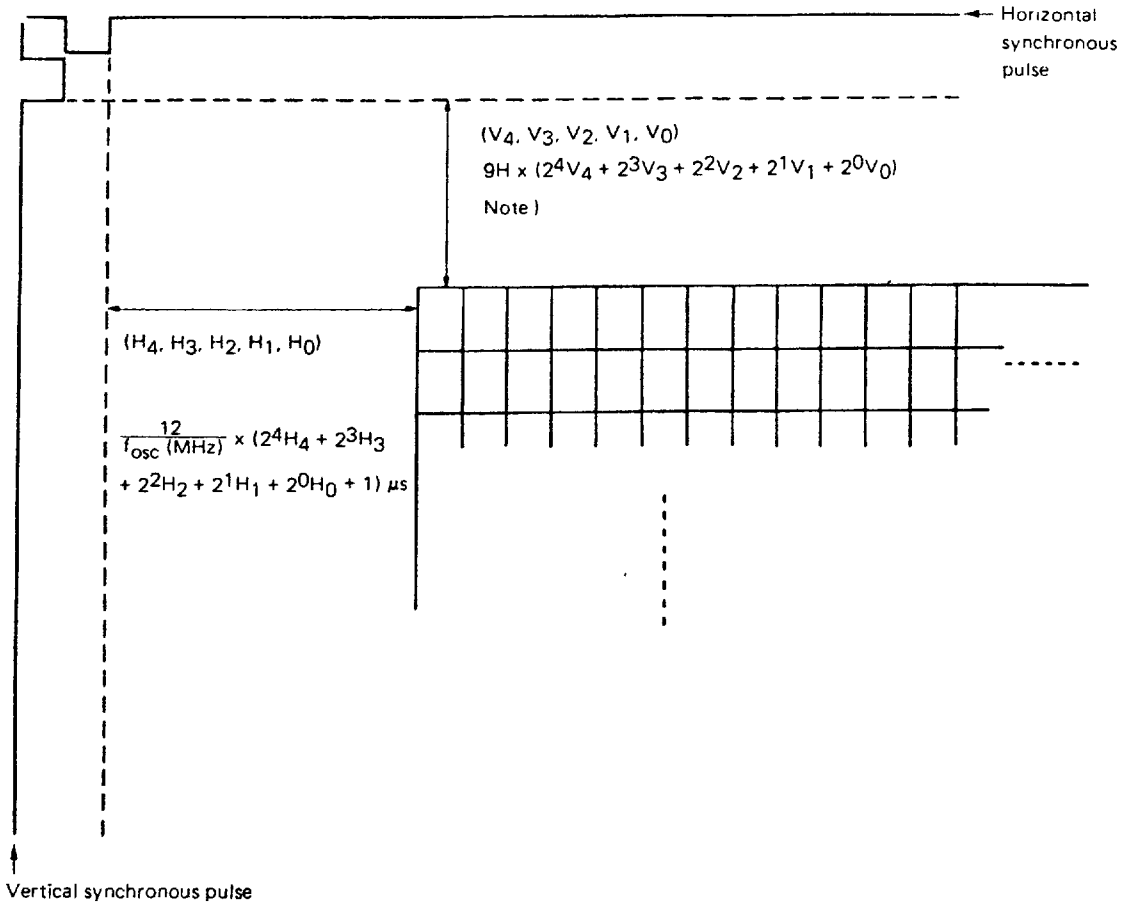
LC oscillation control bit	
L_{osc}	Function
0	LC oscillation OFF
1	LC oscillation ON

Blink control bit		
BL_2	BL_1	Function
0	0	Blink OFF
0	1	Blink ratio 1 (ON) : 3 (OFF)
1	0	Blink ratio 3 (ON) : 1 (OFF)
1	1	Blink ratio 1 (ON) : 1 (OFF)

Display ON/OFF control bit	
Do	Function
0	Display OFF
1	Display ON

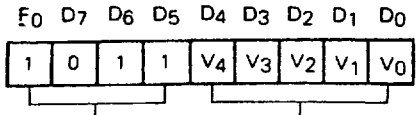
Character Display Address

Character display starting address is determined as follows with values assigned by both the display position vertical address command (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 0, 1, 1, V_4, V_3, V_2, V_1, V_0) and the display position horizontal address command (F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0) = (1, 1, 1, 0, H_4, H_3, H_2, H_1, H_0).



Note: Vertical address counter is incremented by the leading edge of the horizontal synchronous pulse.

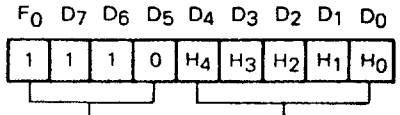
Assignment Command for Display Position Vertical Address



Vertical address assignment bits					
V_4	V_3	V_2	V_1	V_0	Start address
0	0	0	0	0	From the trailing edge of the vertical synchronous pulse 9 x 0H
0	0	0	0	1	From the trailing edge of the vertical synchronous pulse 9 x 1H
⋮					⋮
1	1	1	1	1	From the trailing edge of the vertical synchronous pulse 9 x 31H

These show that this command is the assignment command for the display position address.

Assignment Command for Display Position Horizontal Address



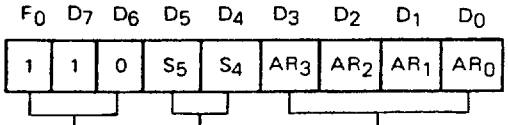
Horizontal address assignment bits					
H_4	H_3	H_2	H_1	H_0	Start address
0	0	0	0	0	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 1 [μs]
0	0	0	0	1	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 2 [μs]
⋮					⋮
1	1	1	1	1	From the trailing edge of the horizontal synchronous pulse $12/f_{osc}$(MHz) x 32 [μs]

These show that this command is the assignment command for the display position horizontal address.

Assignment of Character Size

Character size for each line can be selected from 1H, 2H, 3H or 4H of 1 dot. Row and character size is assigned with the character size assignment command.

Character Size Assignment Command



Row address selection bit				
AR_3	AR_2	AR_1	AR_0	Function
0	0	0	0	The first line is selected.
0	0	0	1	The second line is selected.
⋮				⋮
1	0	1	1	The 12th line is selected.

Enter only addresses OH to BH.

Character size specification bit				
S_5	S_4	Character dot size		
0	0	Longitudinal	1 H	Lateral t_{dot}
0	1		2 H	$2 \cdot t_{dot}$
1	0		3 H	$3 \cdot t_{dot}$
1	1		4 H	$4 \cdot t_{dot}$

$$t_{dot} = \frac{1}{f_{osc}(MHz)}\ \mu s$$

These show that this command is the character size assignment command.

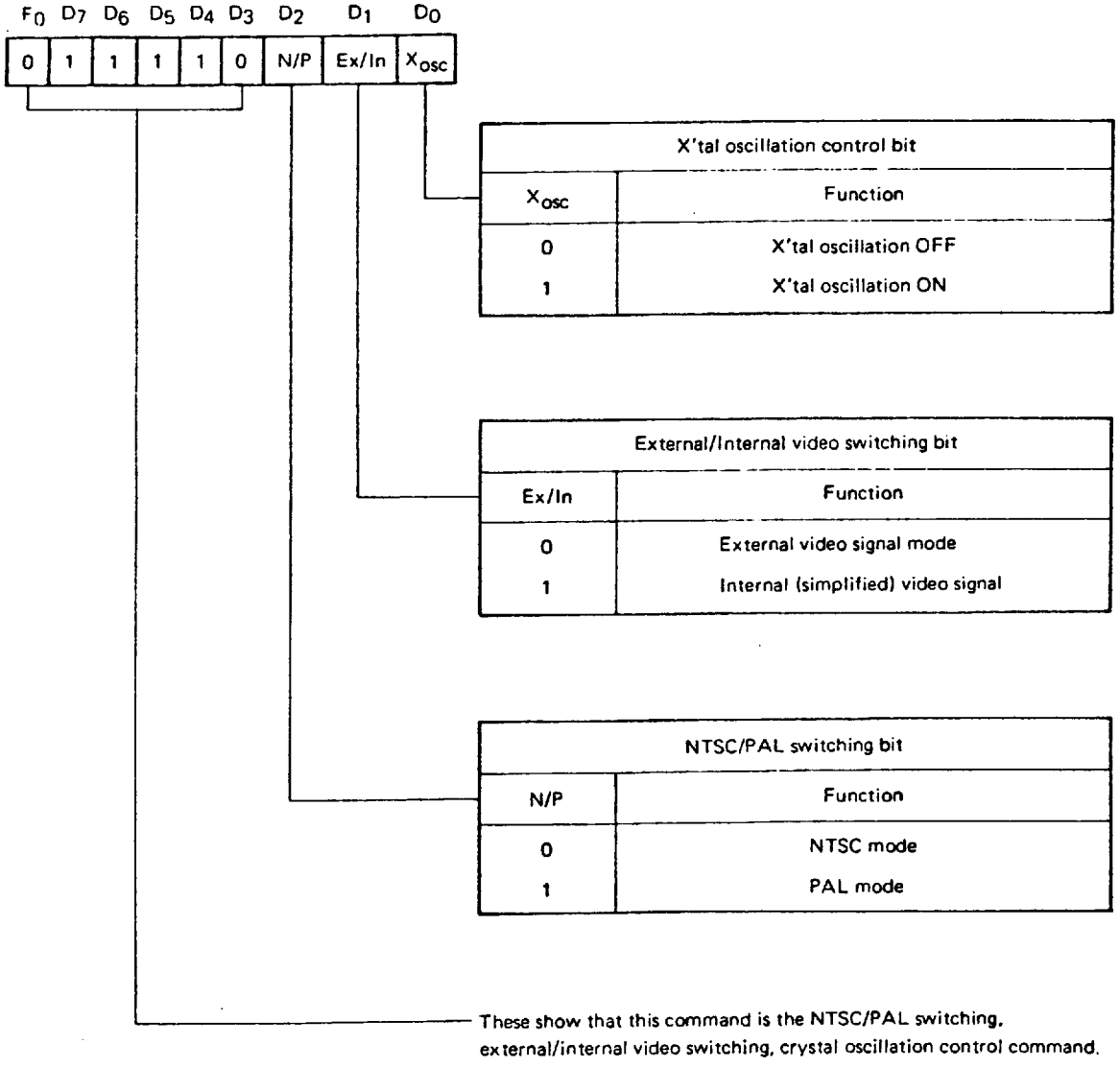
External/Internal Video Switching

When TV broadcasting signal can't be received or when unprerecorded tape is being played, synchronization is poor and mixing of the character signal results in poor character display. In such cases an internal simplified video signal (raster signal of one color out of white, black, red, green and blue) should be generated with NTSC/PAL switching, external/internal video switching, or crystal oscillation control command, so that mixing of the character signal becomes possible. When an external video signal is used, crystal oscillation can be stopped by setting the crystal oscillation control bit (X_{osc}) to "0." This reduces power consumption. Internal video signal is noninterlaced video signal.

NTSC/PAL Switching

The internal simplified video signal shown above can be used in both NTSC and PAL systems by changing NTSC/PAL switching bit with the NTSC/PAL switching, external/internal video switching, or X'tal oscillation control command and by changing the external X'tal (14.318 18 MHz for NTSC, 17.734 476 MHz for PAL).

External/Internal Video Switching, X'tal Oscillation Control Command

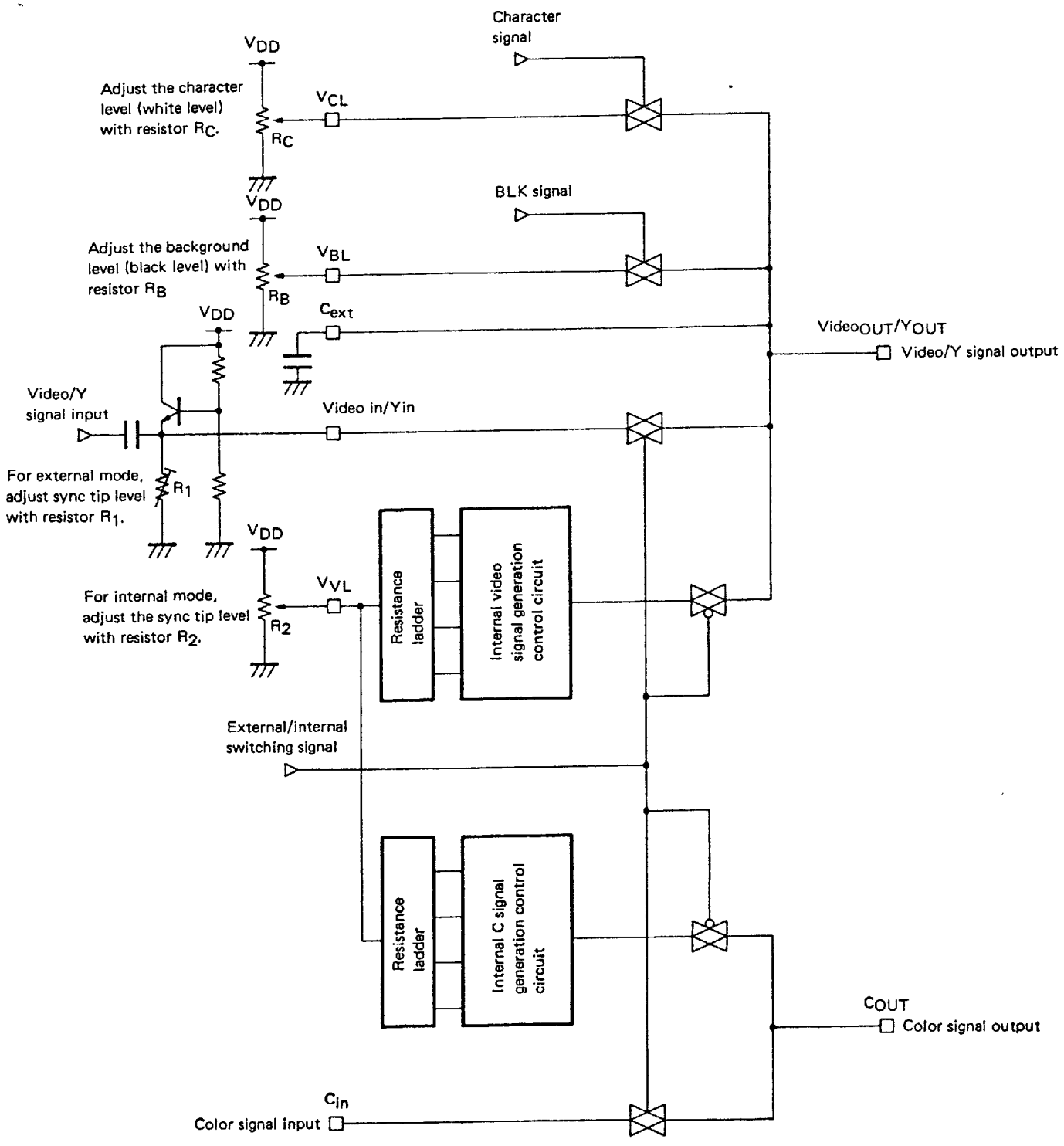


X'tal oscillation control bit	
X_{osc}	Function
0	X'tal oscillation OFF
1	X'tal oscillation ON

External/Internal video switching bit	
Ex/In	Function
0	External video signal mode
1	Internal (simplified) video signal

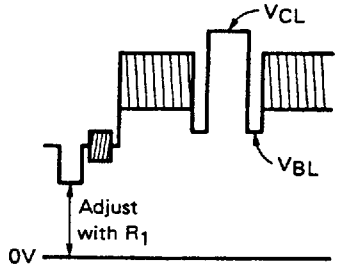
NTSC/PAL switching bit	
N/P	Function
0	NTSC mode
1	PAL mode

Adjusting Sync tip level, Character level, and Background level

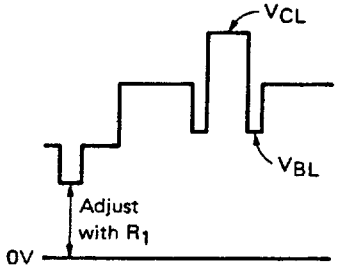


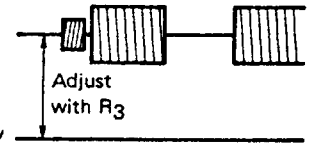
External mode

① For composite



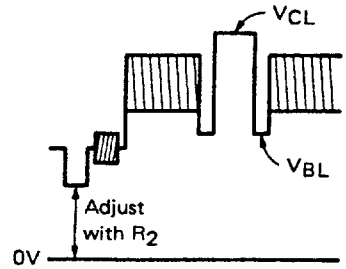
② For component



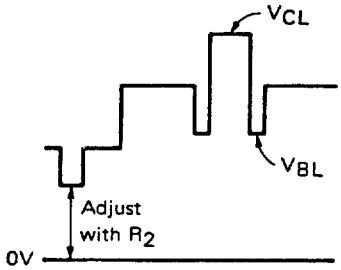


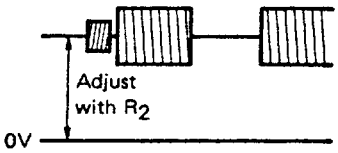
Internal mode

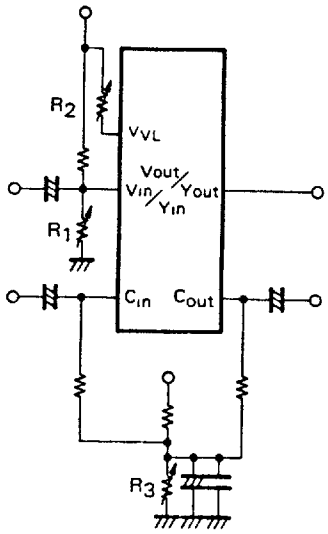
① For composite



② For component







Note: Since there is no built-in pedestal clamp circuit for external video signal, connect direct current clamp circuit in front of "video in/Y in".

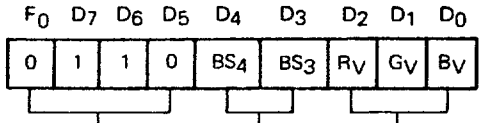
Background Assignment and Color Changing of Internal Video Signal

The background can be selected for each screen image from no-background, black-fringe, black square background, and black-solid background by the background internal video signal color assignment command. The background color is black.

When an internal video signal is used because of NTSC/PAL switching, external/internal video switching, and X'tal oscillation control command, raster color is switched by this background internal video signal color assignment command as well. In this case, white, black, red, green, or blue can be selected.

- No background ..... Character is totally surrounded by image or internal video signal.
- Black fringe ..... Characters are trimmed with 1 dot-minimum character (1H/1 dot).
- Black square background ..... The 12 line x 24 column block displaying characters has a black background.
- Black solid background ..... Image signal or internal video signal is totally omitted and whole screen has a black background.

Background Internal Video Signal Color Assignment Command



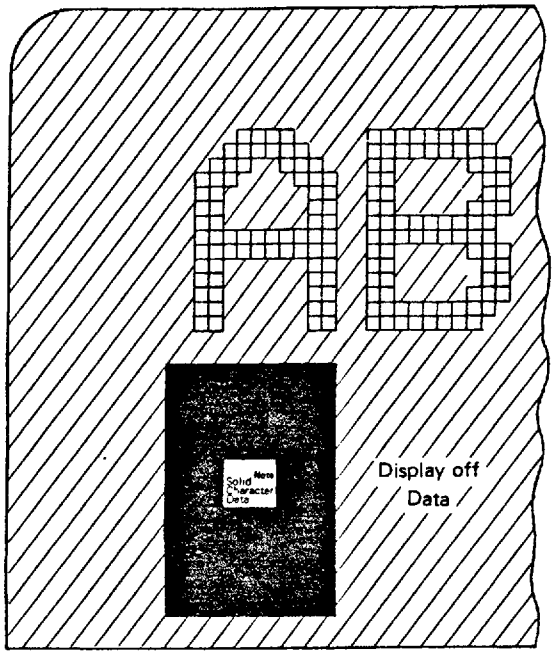
Internal simplified video signal color assignment bit			
R_V	G_V	B_V	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Setting impossible
1	0	0	Red
1	0	1	Setting impossible
1	1	0	Setting impossible
1	1	1	White

Background assignment bit		
BS_4	BS_3	Function
0	0	No background
0	1	Black fringe
1	0	Black square background
1	1	Black solid background

These show that this command is the background/internal video signal color assignment command.

Display in Various Background Modes

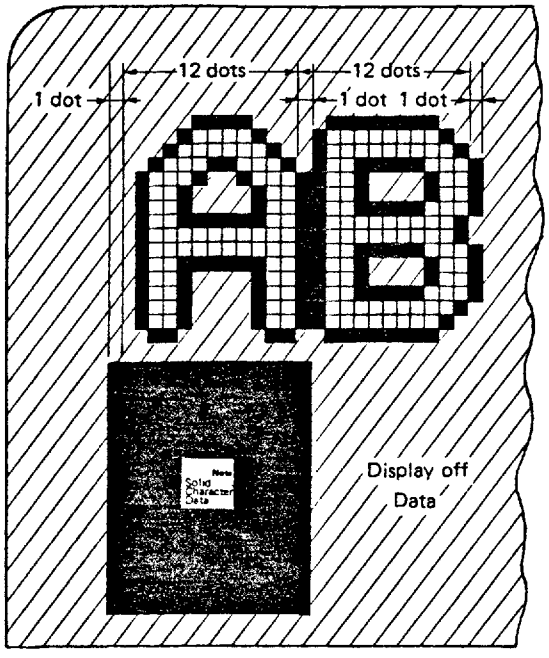
No background



White (character)

Color of image or internal video signal

Black fringe

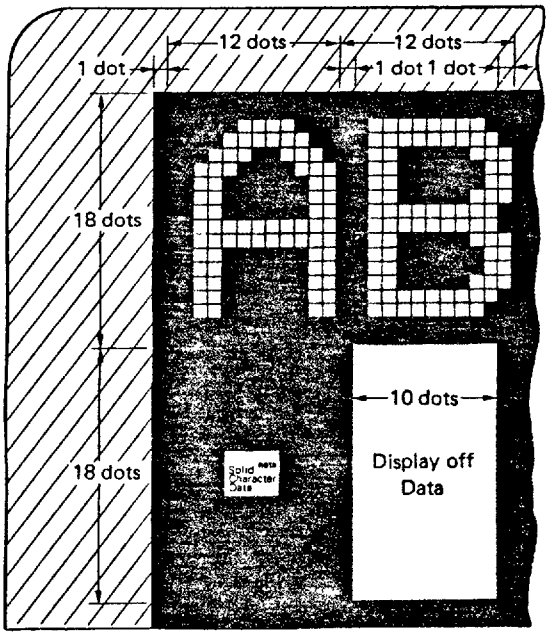


White (character)

Black (background)

Color of image or internal video signal

Black Square background

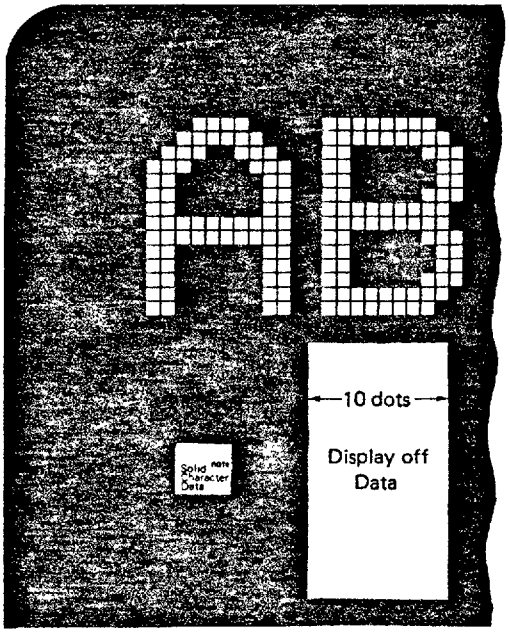


White (character)

Black (background)

Color of image or internal video signal

Black Solid background



White (character)

Black (background)

Color of image or internal video signal.

Note: The solid character data means the data of character code 1FH(standard type of NEC).

1. No background
   Only characters are displayed.

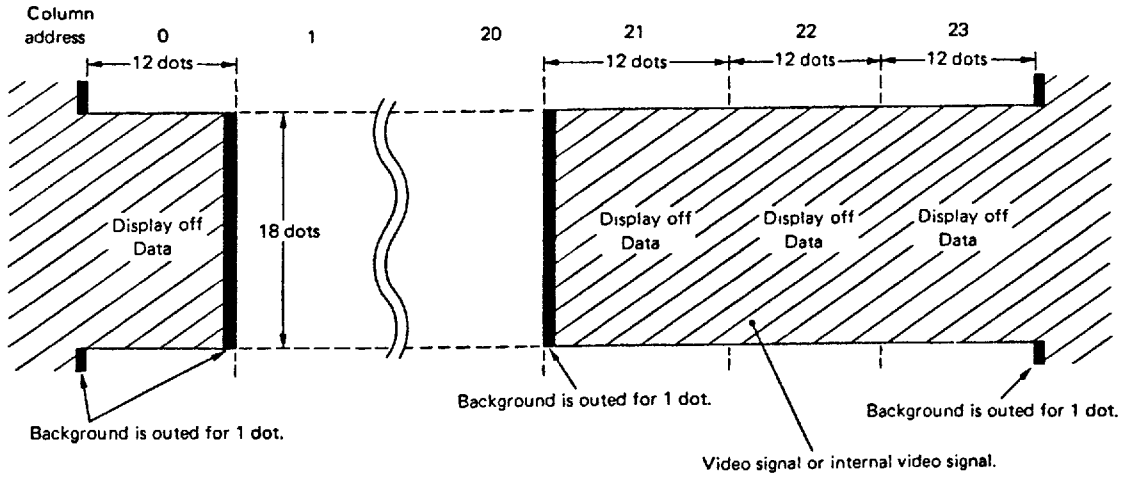
2. Black fringe
   Characters with black fringe are displayed. Black fringe of a character which is used the edge of dot-matrix (right and left) is displayed in neighbor character area for 1 dot.
   The fringe is the dot of the smallest character size and irrespective of character size.

3. Black square background
   The black square background is displayed in character display area.
   In this case, the background is displayed in outside of character display area (right and left) for 1 dot.
   In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

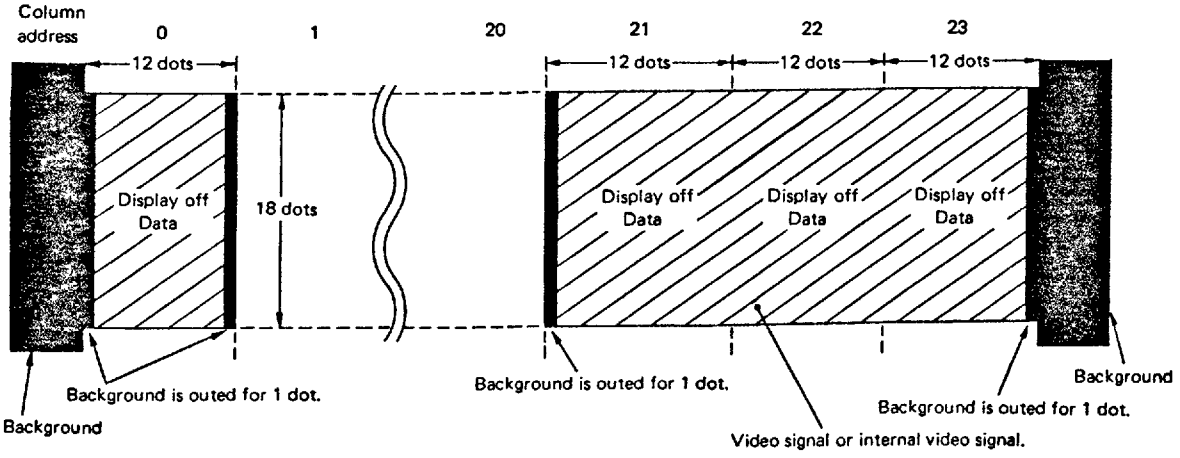
4. Black solid background
   The black solid background is displayed in the all area of screen.
   In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

In case of using "Display OFF data".

- Black square background



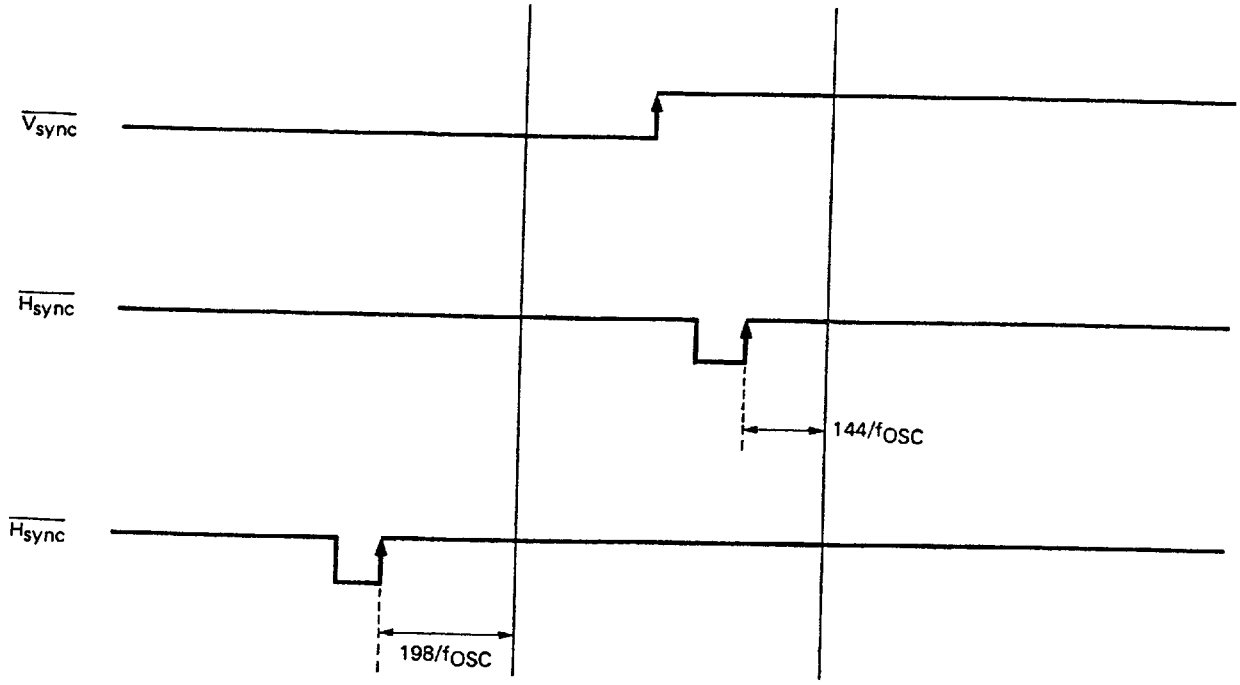
- Black solid background



Note: The "1 dot" is the dot of the smallest character size and irrespective of character size.

Synchronous protection operation

Synchronous protection operation is performed depending on the area **** where the $\overline{V_{sync}}$ rises, and the displayed character does'nt shake vertically.



Synchronous protection operation can be assigned the format "for frame" or "for field".

for frame: Same as synchronous protection operation of the preceding frame (two field before).

for field: Same as synchronous protection operation of the preceding field.

The mode "for frame" or "for field" may be selected with the "format and synchronous protection assignment" command "FF".

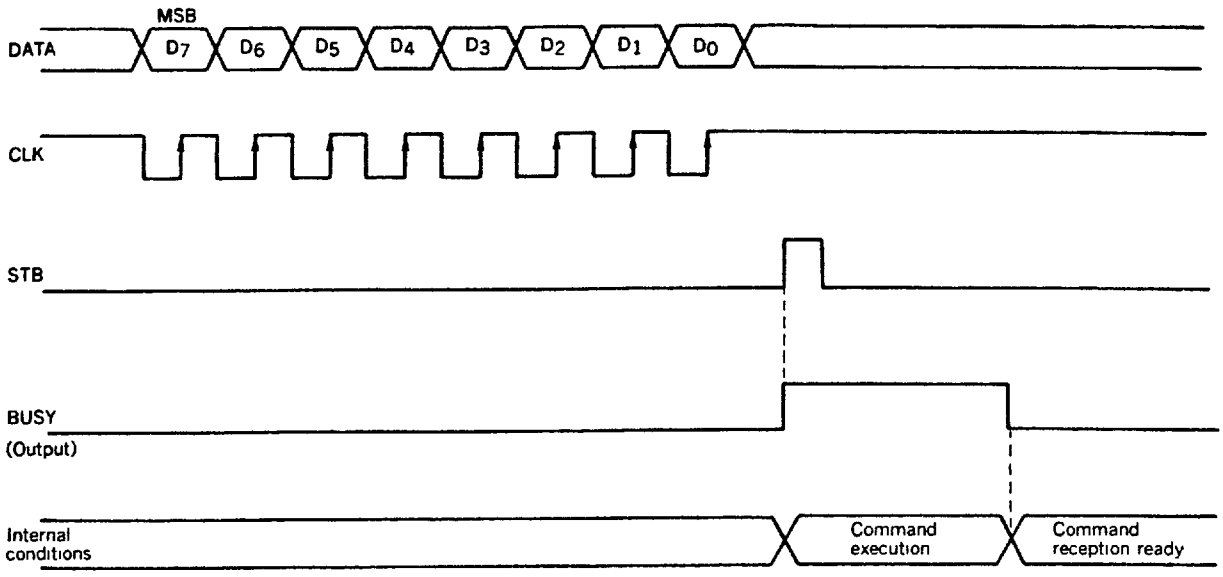
"0" : for frame

"1" : for field

Synchronous protection monitor output is enabled by changing the BUSY signal output to the synchronous protection monitor output (V_{MON}) with the mask code option. The output is as follows:

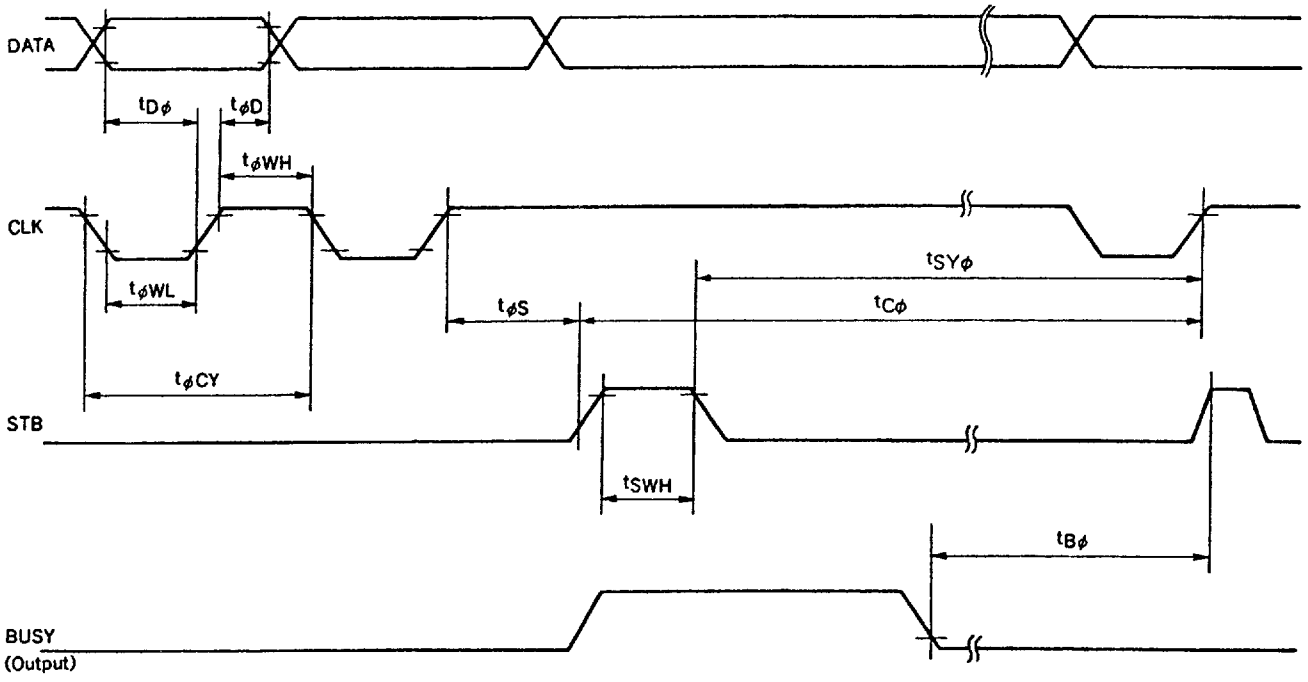
"Low": Synchronous protection operation

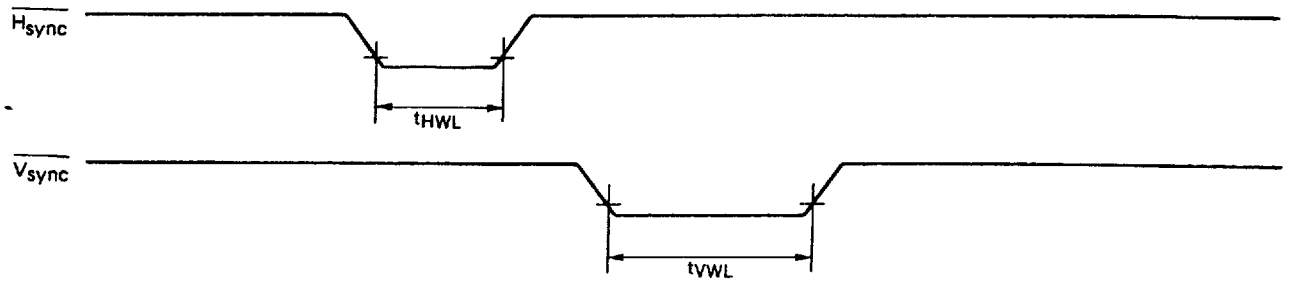
"High": No synchronous protection .



For format data, a busy signal is generated after the internal conditions are completely determined. When writing data in VRAM, a busy signal is generated after the completion of writing in VRAM. When the VRAM write period extends into the horizontal retrace line period, the busy signal becomes longer than usual, so be careful. (This is because oscillation is suspended during the horizontal retrace line period, so writing in VRAM becomes impossible.)

Note: As the synchronous protection monitor output function is selected in mask code option, the 1st-terminal cant output the BUSY signal.
Please take care of the data transmitting and keep the recommended operation timing.





RECOMMENDED OPERATION TIMING (T_a = 25 °C, $V_{DD} - V_{SS}$ = 5.0 V)

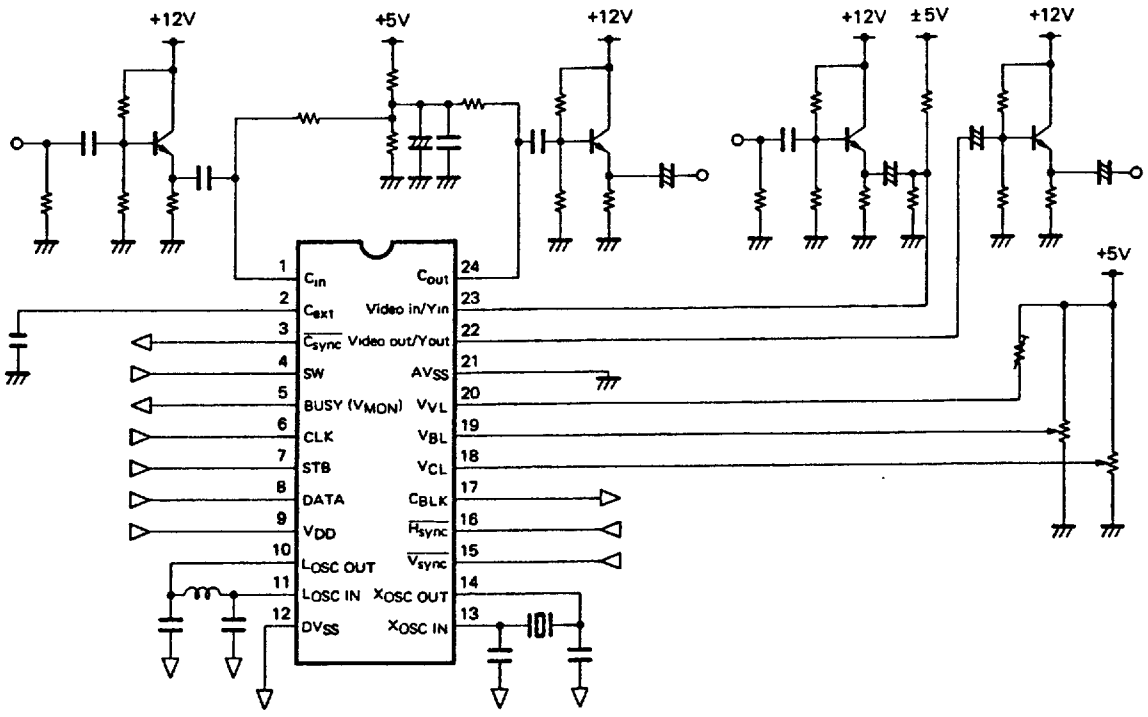
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Min. Setup Time	$t_{D\phi}$	200			ns	
Min. Hold Time	$t_{\phi D}$	200			ns	
Min. Clock Low-level Width	$t_{\phi WL}$	700			ns	
Min. Clock High-level Width	$t_{\phi WH}$	700			ns	
Min. Clock → Strobe Time	$t_{\phi S}$	400			ns	
Min. Strobe High-level Width	t_{SWH}	1			μs	
Clock Cycle	$t_{\phi CY}$	1.6			μs	
Min. Busy → Strobe Time	$t_{B\phi}$	100			ns	
Min. $\overline{V_{sync}}$ Low-level Width	t_{VWL}	4			μs	
Min. $\overline{H_{sync}}$ Low-level Width	t_{HWL}	4			μs	
Max. Strobe → Strobe Time	$t_{C\phi}$	14.4			μs	Displayed Character Data Command transmits at display ON with following conditions. Strobe high-level Width: 1 μs; $\overline{H_{sync}}$ low-level Width: 5 μs; f_{osc}: 6 MHz; Character size: 2H/dot
		11.1			μs	Displayed Character Data Command transmits at display OFF with following conditions. Strobe high-level Width: 1 μs; $\overline{H_{sync}}$ low-level Width: 5 μs; f_{osc}: 6 MHz; Character size: 2H/dot
Min. Strobe → Clock Time	$t_{SY\phi}$	4			μs	Commands except Displayed Character Data Command transmit.

The calculate expression of Max. Strobe → Strobe Time

$t_{C\phi}$ = STB High + $\overline{H_{sync}}$ Low + (25/f_{osc}) x (character size) + 100 ns

- (25/f_{osc}): When the display is off: 15
- 100 ns: When the display is off: 0

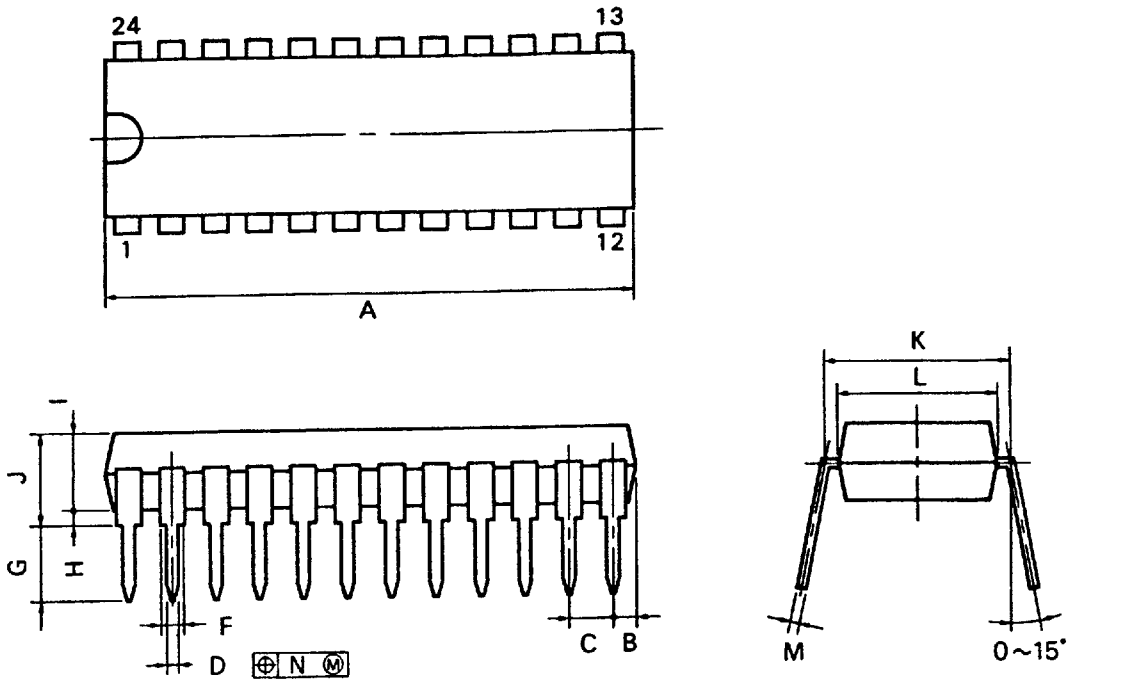
ADOPTED CIRCUIT



Note: The peripheral amplifier uses +12 V. To use +5 V, give attention to the amplifier configuration. Use analog ground ⏚ and digital ground ▽ separate.

Note: This bracket shows terminal arrangement for the mask code option when terminal 5 of μPD6452 is used for the synchronization protection monitor output (V_{MON}).

24PIN PLASTIC SHRINK DIP (300 mil)



S24C-70-300B

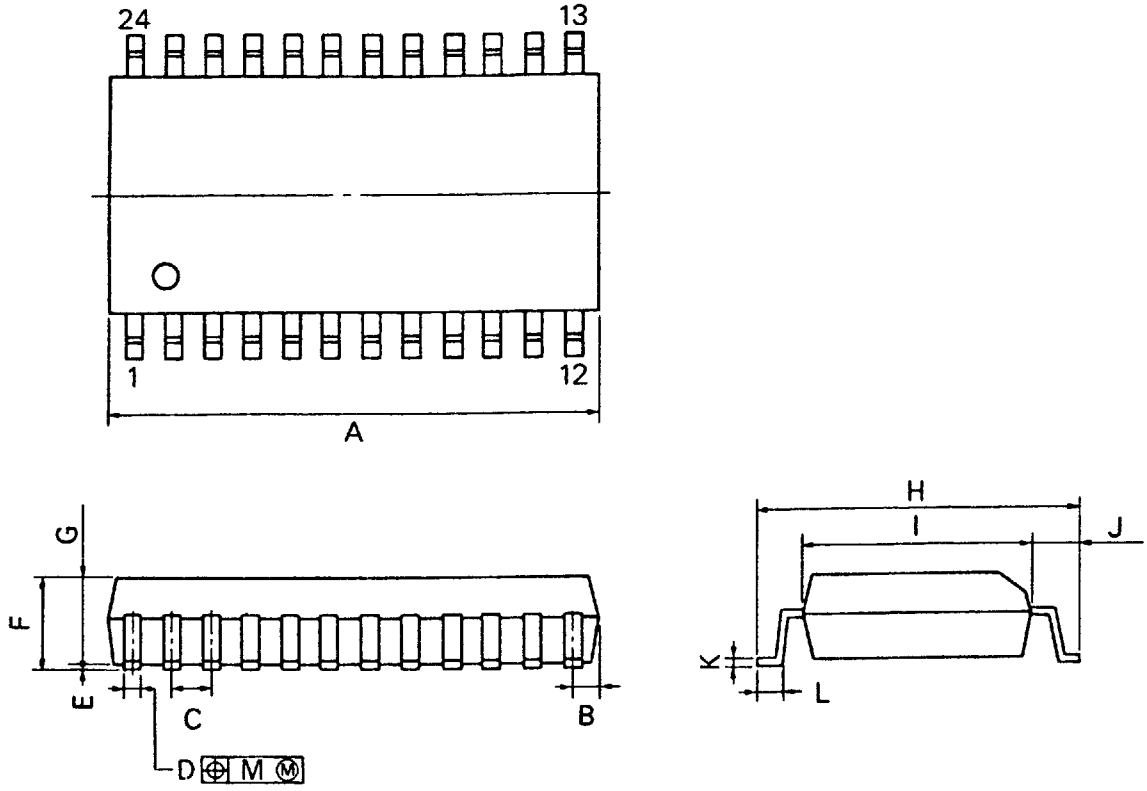
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24PIN PLASTIC SOP (375 mil)



P24GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005