Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS SEMICONDUCTOR

ICL7109

12-Bit, Microprocessor-Compatible A/D Converter

August 1997

Features

- 12-Bit Binary (Plus Polarity and Over-Range) Dual Slope Integrating Analog-to-Digital Converter
- Byte-Organized, TTL Compatible Three-State Outputs and UART Handshake Mode for Simple Parallel or Serial Interfacing to Microprocessor Systems
- RUN/$\overline{\text{HOLD}}$ Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing
- True Differential Input and Differential Reference
- Low Noise (Typ) . . . . . $15\mu V_{P-P}$
- Input Current (Typ). 1pA
- Operates At Up to 30 Conversions/s
- On-Chip Oscillator Operates with Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions/s for 60Hz Rejection. May Also Be Used with An RC Network Oscillator for Other Clock Frequencies

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICL7109MDL	-55 to 125	40 Ld SBDIP	D40.6
ICL7109IDL	-25 to 85	40 Ld SBDIP	D40.6
ICL7109IJL	-25 to 85	40 Ld CERDIP	F40.6
ICL7109CPL	0 to 70	40 Ld PDIP	E40.6
ICL7109MDL/883B	-55 to 125	40 Ld SBDIP	D40.6
ICL7109IPL	-25 to 85	40 Ld PDIP	E40.6

Description

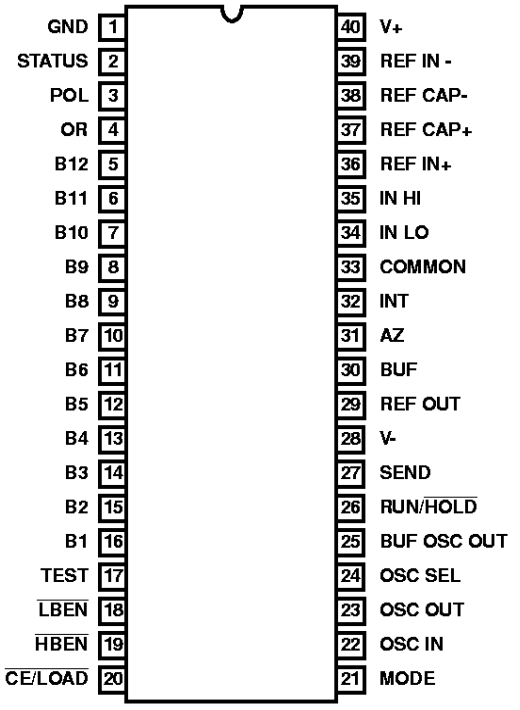
The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and over-range) may be directly accessed under control of two byte enable inputs and a chip select input for a single parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission. The RUN/$\overline{\text{HOLD}}$ input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than $1\mu V/^{o}C$, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

Pinout

ICL7109
(CERDIP, PDIP, SBDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3092.1**

Absolute Maximum Ratings

Positive Supply Voltage (GND to V+) . . . . . +6.0V
Negative Supply Voltage (GND to V-) . . . . . -9V
Analog Input Voltage (Either Input) (Note 1) . . . . . V+ to V-
Reference Input Voltage (Either Input) (Note 1) . . . . . V+ to V-
Digital Input Voltage . . . . . (V+) +0.3V
Pins 2-27 (Note 2) . . . . . GND -0.3V

Operating Conditions

Temperature Range
M Suffix . . . . . -55°C to 125°C
I Suffix . . . . . -25°C to 85°C
C Suffix . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	60	20
CERDIP Package	55	18
PDIP Package	50	N/A

Maximum Junction Temperature (PDIP Package) . . . . . 150°C
Maximum Junction Temperature (CERDIP Package) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s Max) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Analog Electrical Specifications

$V+ = +5V$, $V- = -5V$, GND = 0V, $T_A = 25°C$, $f_{CLK} = 3.58MHz$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Oscillator Output Current					
High, O_{OH}	$V_{OUT} = 2.5V$	-	1	-	mA
Low, O_{OL}	$V_{OUT} = 2.5V$	-	1.5	-	mA
Buffered Oscillator Output Current					
High, BO_{OH}	$V_{OUT} = 2.5V$	-	2	-	mA
Low, BO_{OL}	$V_{OUT} = 2.5V$	-	5	-	mA
Zero Input Reading	$V_{IN} = 0.0000V$, $V_{REF} = 204.8mV$	-0000	±0000	+0000	Counts
Ratiometric Error	$V_{IN} = V_{REF}$, $V_{REF} = 204.8mV$ (Note 7)	-3	-	0	Counts
Non-Linearity	Full Scale = 409.6mV to 2.048mV Maximum Deviation from Best Straight Line Fit, Over Full Operating Temperature Range (Notes 4 and 6)	-1	±0.2	+1	Counts
Rollover Error	Full Scale = 409.6mV to 2.048V Difference in Reading for Equal Positive and Negative Inputs Near Full Scale (Notes 5 and 6), $R_1 = 0\Omega$	-1	±0.2	+1	Counts
Linearity	Full-Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 4)	-	±0.2	±1	Counts
Common Mode Rejection Ratio, CMRR	$V_{CM} = ±1V$, $V_{IN} = 0V$, Full Scale = 409.6mV	-	50	-	µV/V
Input Common Mode Range, VCMR	Input HI, Input LO, Common (Note 4)	(V-) +2.0	-	(V+) -2.0	V
Noise, eN	$V_{IN} = 0V$, Full-Scale = 409.6mV (Peak-to-Peak Value Not Exceeded 95% of Time)	-	15	-	µV
Leakage Current Input, I_{ILK}	$V_{IN} = 0V$, All Devices at 25°C (Note 4)	-	1	10	pA
ICL7109CPL	0°C to 70°C (Note 4)	-	20	100	pA
ICL7109IDL	-25°C to 85°C (Note 4)	-	100	250	pA
ICL7109MDL	-55°C to 125°C	-	2	100	nA
Zero Reading Drift	$V_{IN} = 0V$, R_1 - 0Ω (Note 4)	-	0.2	1	µV/°C

Analog Electrical Specifications $V+ = +5V, V- = -5V, GND = 0V, T_A = 25^oC, f_{CLK} = 3.58MHz,$ Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Scale Factor Temperature Coefficient	$V_{IN} = 408.9mV = > 7770_8$ Reading Ext. Ref. 0ppm/^{o}C (Note 4)	-	1	5	ppm/^{o}C
REFERENCE VOLTAGE					
Ref Out Voltage, V_{REF}	Referred to V+, 25kΩ Between V+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temperature Coefficient	25kΩ Between V+ and REF OUT (Note 4)	-	80	-	ppm/^{o}C
POWER SUPPLY CHARACTERISTICS					
Supply Current V+ to GND, I+	V_{IN} = 0V, Crystal Osc 3.58MHz Test Circuit	-	700	1500	µA
Supply Current V+ to V-, I_{SUPP}	Pins 2 - 21, 25, 26, 27, 29; Open	-	700	1500	µA

Digital Electrical Specifications $V+ = +5V, V- = -5V, GND = 0V, T_A = 25^oC,$ Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{OUT} = 100µA Pins 2 - 16, 18, 19, 20	3.5	4.3	-	V
Output Low Voltage, V_{OL}	I_{OUT} = 1.6mA Pins 2 - 16, 18, 19, 20	-	±0.20	±0.40	V
Output Leakage Current	Pins 3 - 16 High Impedance	-	±0.01	±1	µA
Control I/O Pullup Current	Pins 18, 19, 20 V_{OUT} = V+ -3V MODE Input at GND (Note 4)	-	5	-	µA
Control I/O Loading	$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18 (Note 4)	-	–	50	pF
DIGITAL INPUTS					
Input High Voltage, V_{IH}	Pins 18 - 21, 26, 27 Referred to GND	3.0	-	-	V
Input Low Voltage, V_{IL}	Pins 18 - 21, 26, 27 Referred to GND	-	-	1	V
Input Pull-Up Current	Pins 26, 27 V_{OUT} = (V+) -3V	-	5	-	µA
Input Pull-Up Current	Pins 17, 24 V_{OUT} = (V+) -3V	-	25	-	µA
Input Pull-Down Current	Pin 21 V_{OUT} = GND +3V	-	5	-	µA
TIMING CHARACTERISTICS					
MODE Input Pulse Width, t_W	(Note 4)	50	-	-	ns

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.
3. This limit refers to that of the package and will not be obtained during normal operation.
4. This parameter is not production tested, but is guaranteed by design.
5. Roll-over error for $T_A = -55^oC$ to 125^oC is ±10 counts (Max).
6. A full scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.
7. For CERDIP package the Ratiometric error can be -4 (Min).

Pin Descriptions

PIN	SYMBOL	DESCRIPTION		
1	GND	Digital Ground, 0V. Ground return for all digital logic.		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity - HI for positive input.		Three-State Output Data Bits
4	OR	Overrange - HI if overranged.		Three-State Output Data Bits
5	B12	Bit 12	(Most Significant Bit)	Three-State Output Data Bits
6	B11	Bit 11	High = True	Three-State Output Data Bits
7	B10	Bit 10	High = True	Three-State Output Data Bits
8	B9	Bit 9	High = True	Three-State Output Data Bits
9	B8	Bit 8	High = True	Three-State Output Data Bits
10	B7	Bit 7	High = True	Three-State Output Data Bits
11	B6	Bit 6	High = True	Three-State Output Data Bits
12	B5	Bit 5	High = True	Three-State Output Data Bits
13	B4	Bit 4	High = True	Three-State Output Data Bits
14	B3	Bit 3	High = True	Three-State Output Data Bits
15	B2	Bit 2	High = True	Three-State Output Data Bits
16	B1	Bit 1	(Least Significant Bit)	Three-State Output Data Bits
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{\text{LBEN}}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1 through B8. With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.		
19	$\overline{\text{HBEN}}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9 through B12, POL, OR. With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.		
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load - With Mode (Pin 21) low. $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1 through B12, POL, OR outputs are disabled. With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.		
21	MODE	Input Low - Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.		
22	OSC IN	Oscillator Input		
23	OSC OUT	Oscillator Output		

Pin Descriptions (Continued)

PIN	SYMBOL	DESCRIPTION
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V-	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V+ (Pin 40).
30	BUFFER	Buffer Amplifier Output.
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}.
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}.
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON.
34	INPUT LO	Differential Input Low Side.
35	INPUT HI	Differential Input High Side.
36	REF IN +	Differential Reference Input Positive.
37	REF CAP +	Reference Capacitor Positive.
38	REF CAP-	Reference Capacitor Negative.
39	REF IN-	Differential Reference Input Negative.
40	V+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$
  f_{OSC} (Typ) = 60kHz
  or
  f_{OSC} (Typ) = 3.58MHz Crystal

- **OSCILLATOR PERIOD**

  $t_{OSC} = RC/0.45$
  $t_{OSC} = 1/3.58MHz$ (Crystal)

- **INTEGRATION CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}$ (RC Mode)
  $f_{CLOCK} = f_{OSC}/58$ (Crystal)
  $t_{CLOCK} = 1/f_{CLOCK}$

- **INTEGRATION PERIOD**

  $t_{INT} = 2048 \times t_{CLOCK}$

- **60/50Hz REJECTION CRITERION**

  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

- **OPTIMUM INTEGRATION CURRENT**

  $I_{INT} = 20\mu A$

- **FULL-SCALE ANALOG INPUT VOLTAGE**

  V_{INFS} Typically = 200mV or 2V

- **INTEGRATE RESISTOR**

  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

  $$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

  $$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **V_{INT} MAXIMUM SWING**

  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$
  V_{INT} (Typ) = 2V

- **DISPLAY COUNT**

  $$COUNT = 2048 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

  $t_{CYC} = t_{CLOCK} \times 8192$
  (In Free Run Mode, Run/$\overline{HOLD}$ = 1)
  when f_{CLOCK} = 60kHz, t_{CYC} = 133ms

- **COMMON MODE INPUT VOLTAGE**

  $(V- + 2.0V) < V_{IN} < (V+ - 2V)$

- **AUTO-ZERO CAPACITOR**

  $0.01\mu F < C_{AZ} < 1\mu F$

- **REFERENCE CAPACITOR**

  $0.1\mu F < C_{REF} < 1\mu F$

- **V_{REF}**

  Biased between V+ and V-
  $V_{REF} \cong V+ - 2.8V$
  Regulation lost when V+ to V- $\leq$ 6.4V.
  If V_{REF} is not used, float output pin.

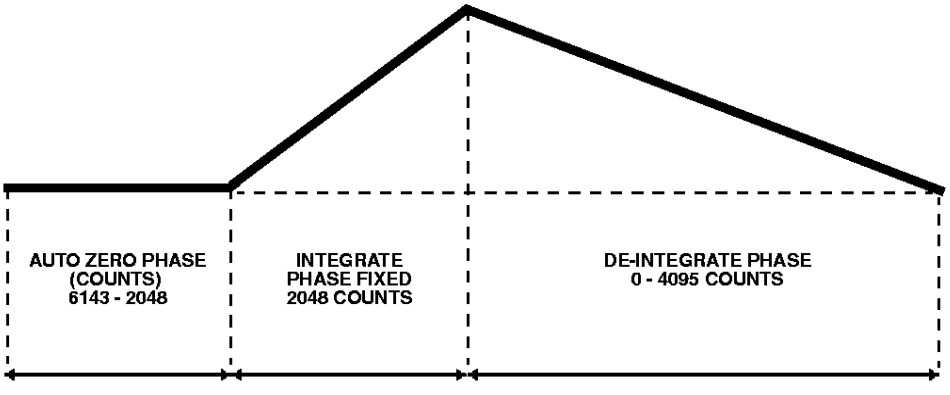
- **POWER SUPPLY: DUAL $\pm$5.0V**

  V+ = +5V to GND
  V- = -5V to GND

- **OUTPUT TYPE**

  Binary Amplitude with Polarity and Overrange Bits
  Tips: Always tie TEST pin HIGH.
  Don't leave any inputs floating.

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 8192 x t_{CLOCK} (IN FREE-RUN MODE)

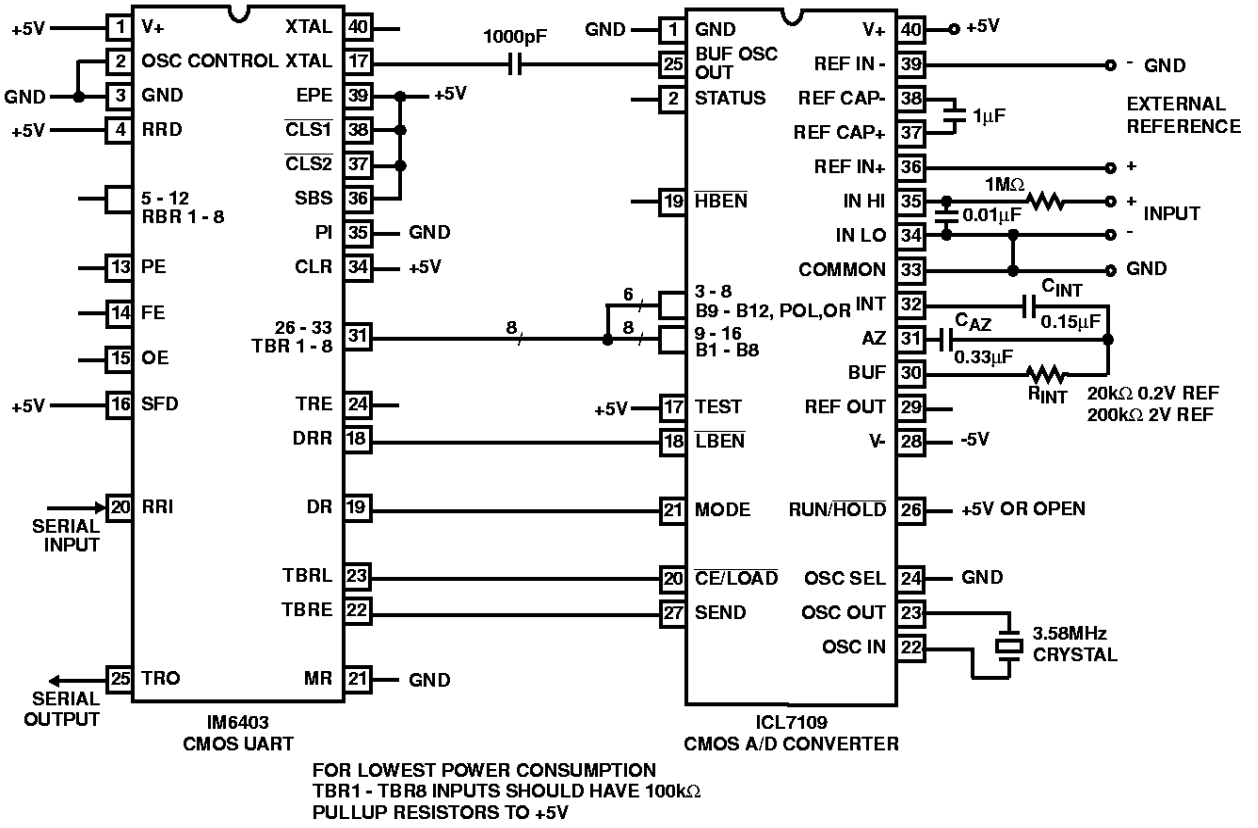


FIGURE 1A. TYPICAL CONNECTION DIAGRAM UART INTERFACE-TO TRANSMIT LATEST RESULT, SEND ANY WORD TO UART

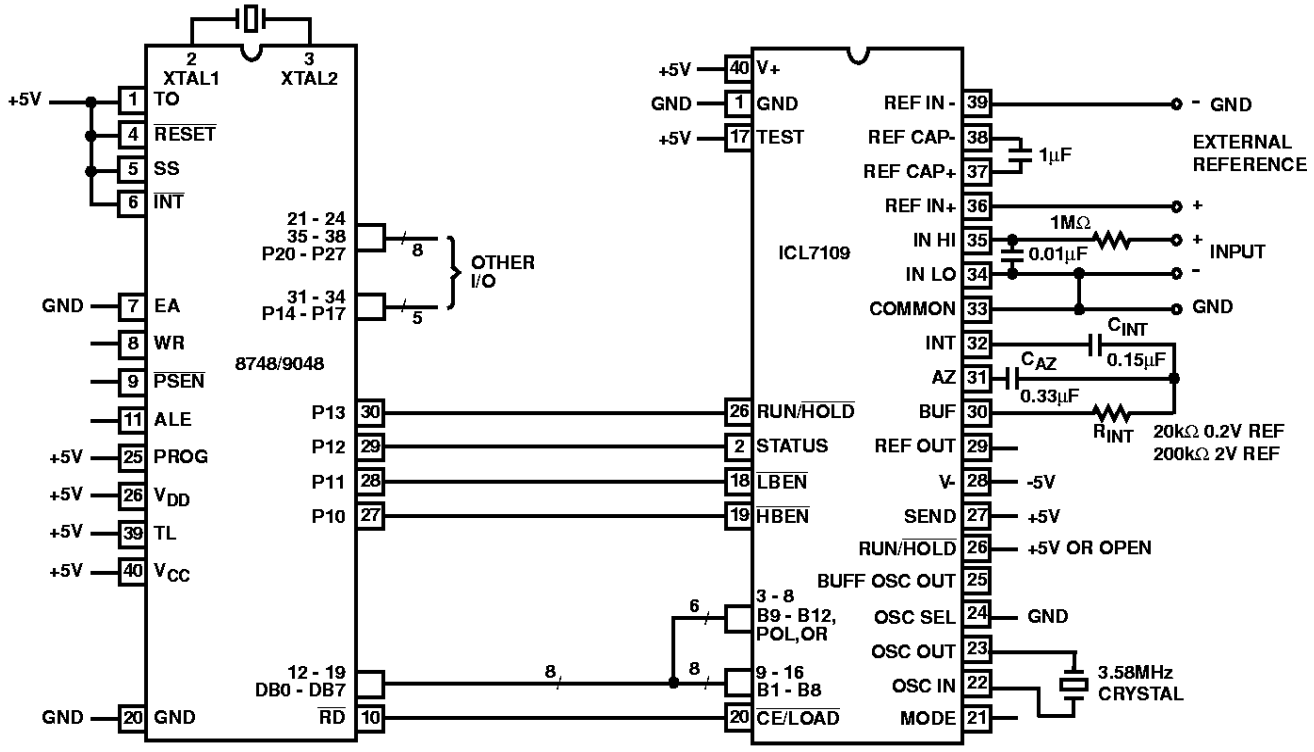


FIGURE 1B. TYPICAL CONNECTION DIAGRAM PARALLEL INTERFACE WITH 8048 MICROCOMPUTER

FIGURE 1.

Detailed Description

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section for the ICL7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto-Zero) with a fixed slope. The time required for the output to return to zero is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 1V below the positive supply to 1.5V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 4V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

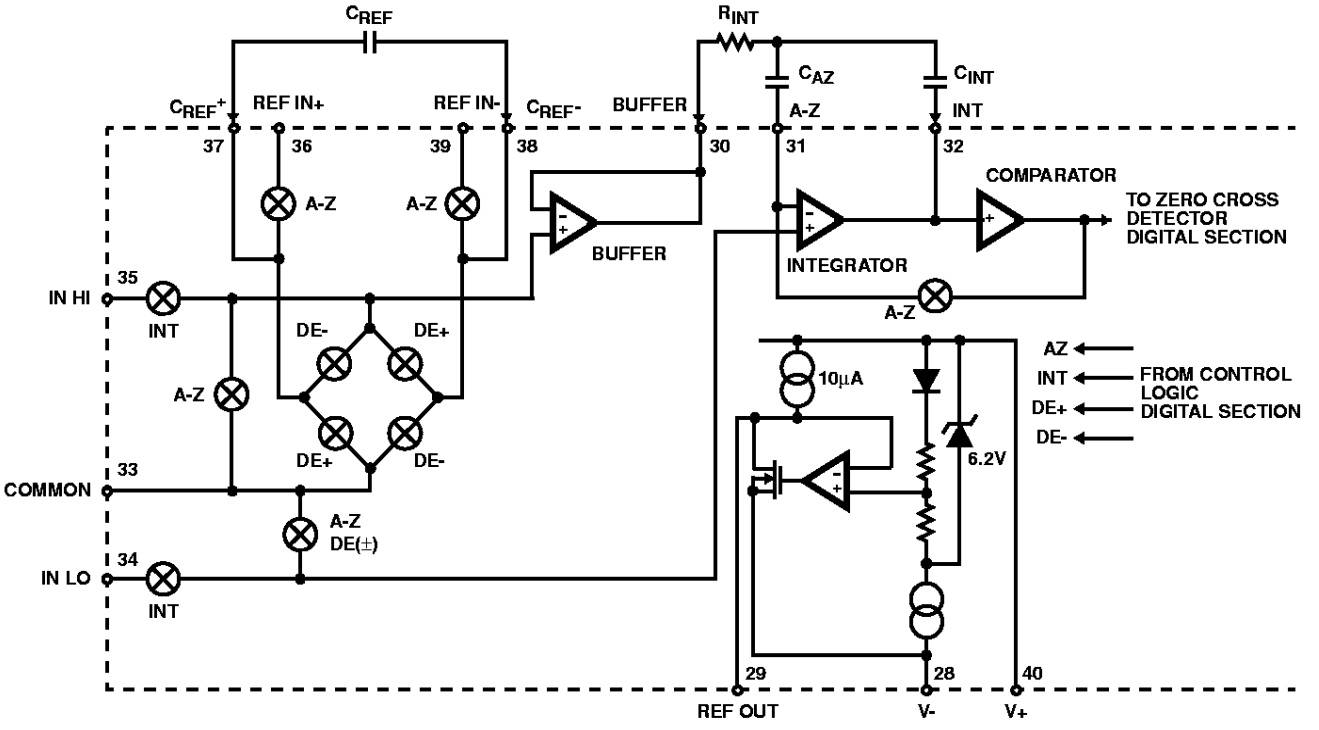


FIGURE 2. ANALOG SECTION OF ICL7109

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and -5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the normal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and roll-over will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve the performance, supplies of ±6V may be used.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They supply 20µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 409.6mV full-scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation :

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}.$$

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approximately. 0.3V from either supply). For the ICL7109 with ±5V supplies and analog common connected to GND, a ±3.5V to ±4V integrator output swing is nominal. For $7^1/_2$ conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15µF and 0.33µF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output swing. In general, the value C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{clock period})(20\mu A)}{\text{integrator output voltage swing}}.$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at The integrating capacitor should have a low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon™ capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system: a smaller physical size and a larger capacitance value lower the overall system noise. However, C_{AZ} cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

Reference Capacitor

A 1µF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e., the reference low is not at analog common) and a 409.6mV scale is used, a large value is required to prevent roll-over error. Generally 10µF will hold the roll-over error to 0.5 count in this instance. Again, Teflon, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

Teflon™ is a trademark of DuPont Corporation

Reference Voltage

The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. For normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of driving the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 33kΩ and 0.15µF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/^{o}C (onboard reference) a temperature difference of 3^{o}C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (Pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10µA. The output voltage is nominally 2.8V below V+, and has a temperature coefficient of ±80ppm/^{o}C (Typ). When using the onboard reference, REF OUT (Pin 29) should be connected to REF- (Pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V+ should be used.

Note that if Pins 29 and 39 are tied together and Pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with Pin 39.

Detailed Description

Digital Section

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Specifications Table. For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

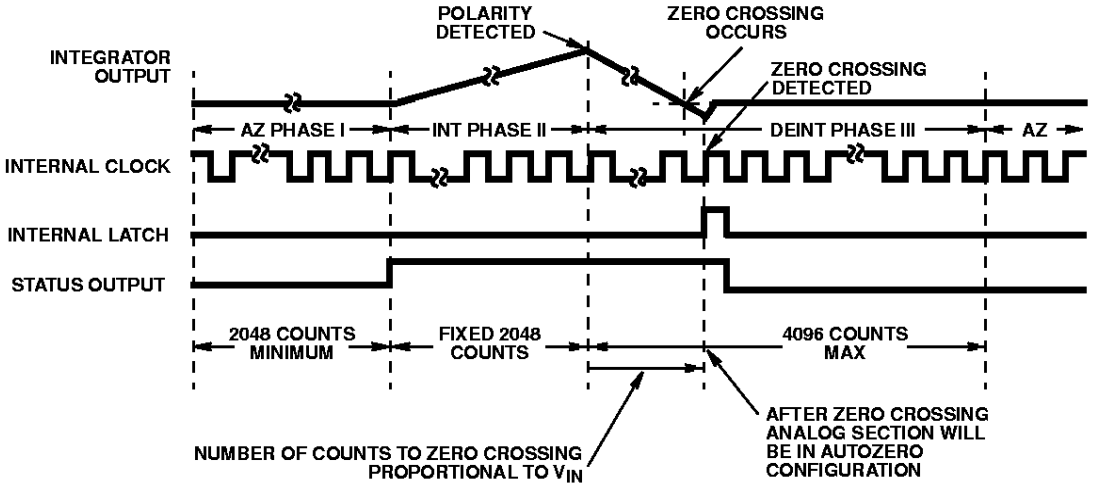


FIGURE 3. CONVERSION TIMING (RUN/$\overline{\text{HOLD}}$ PIN HIGH)

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

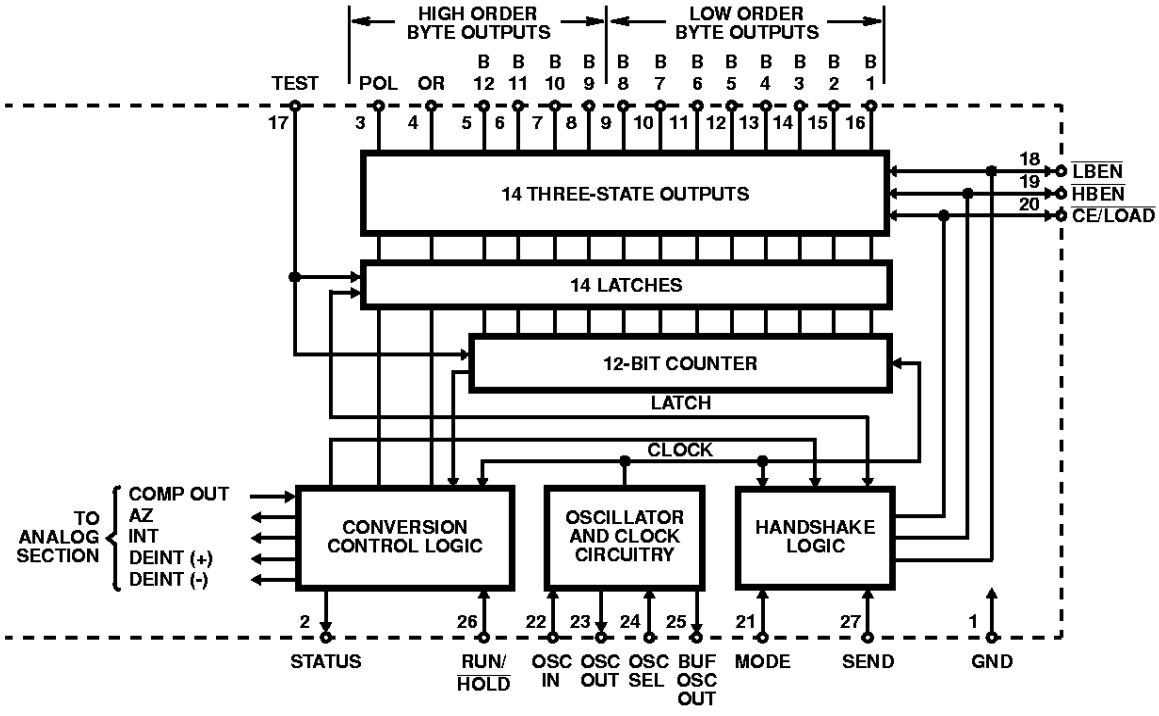


FIGURE 4. DIGITAL SECTION

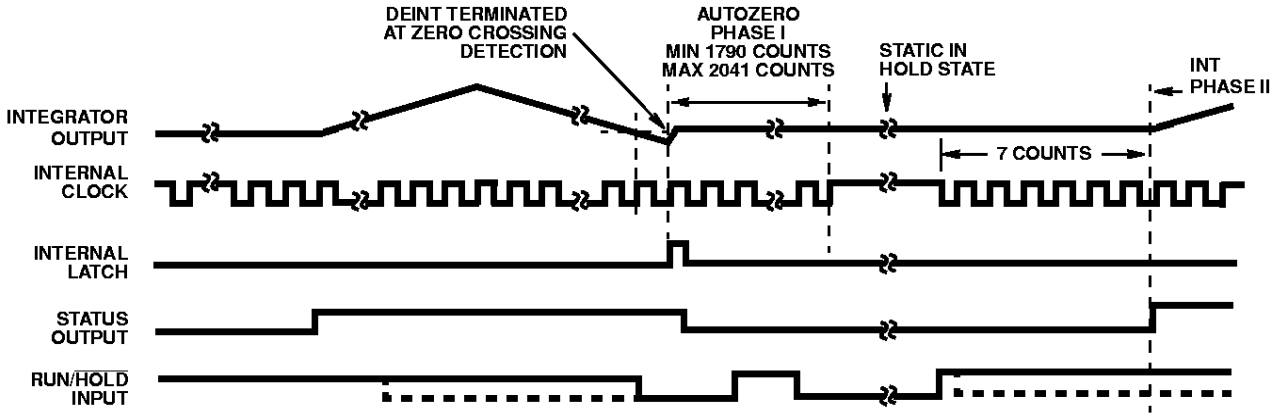


FIGURE 5. RUN/$\overline{\text{HOLD}}$ OPERATION