INTERFACE SPECIFICATION

ADPCM LINE FORMATTER

Bt8200

.c.1.0 INTRODUCTION

This specification describes an ADPCM Line Formatter circuit that implements signaling and line formatting for 32 kbit/s ADPCM voiceband signals according to ANSI standard T1.302-1989, "Digital Processing of Voiceband Signals - 32 kbit/s ADPCM Line Format Standard" (T1.302). The ADPCM Line Formatter also implements all features of Bell Communications Research technical reference TR-TSY-000210, "Low Bit Rate Voice (LBRV) Terminals," and AT&T Communications PUB 54070, "M44 Multiplexing." The signaling methods for ADPCM DS1s specified in ANSI T1.302, Bundle Format, Transition Signaling, and Robbed-bit Signaling, are all provided. In addition, all "bundle format channel-control templates" described in Committee T1 document T1Y1/90-076 (draft supplement to ANSI T1.302) are supported.

The ADPCM Line Formatter supports the line format and the pass-through 60-channel format given in CCITT recommendation G.761. Signaling according to G.761 is not supported in the ADPCM Line Formatter but can be provided either with external hardware or a microcontroller.

In applications that require no signaling the ADPCM Line Formatter can be used to provide format control for the ADPCM Processor. Code rate selection and transparent channel selection can be provided as well as the diagnostic test of the ADPCM Processor.

Control of formatting features is provided via an integral interface to a controller consisting of a microprocessor, program and data memory, and desired status indicators. The ADPCM Line Formatter connects directly to the Brooktree ADPCM Processor; these products in combination provide the complete transcoding function. In this configuration the controller can control both T-1 framing and ADPCM Line Formatter functions.

The ADPCM Line Formatter performs an integral diagnostic test of the ADPCM processor to ensure detection of any faults. The diagnostic, which tests all channels of the ADPCM processor, can be run on any idle channel, unused channel, or any Delta Channel when Bundle Format is used.

Applications for this device include digital cross-connect systems, digital loop concentrators, customer premise multiplexers, network managers, voice-messaging systems, PBXs, and transcoders.

The ADPCM Line Formatter connects directly to either Brooktree's ADPCM Processor: the gate-array set that is described in interface specification IS-101 or the Bt8110 ADPCM Processor. The recommended configuration uses the Bt8110 and is described in application note AN-112. The Bt8200 formatter provides all control signals required to obtain ANSI T1.303-1989 standard ADPCM coding at both 32 kbit/s and at 24 kbit/s as required for Robbed-bit Signaling format. In addition control of optional codes that can be used in place of the standard codes can be provided.

The Bundle Format carries 44 channels on a T-1 line, along with signaling bits and cyclic-redundancy check bits in a "Delta Channel." The channels are organized as four 11-channel "bundles" of 384 kbit/s. These bundles can be carried as H_0 data streams in ISDN systems, as described in AT&T PUB 41459. The Bundle Format is compatible with the AT&T Communications M44 Multiplexing service described in PUB 54070. This signaling format can be connected in 384-kbit/s bundles in fractional T-1 applications.

Transition Signaling will allow 48 channels in a T-1 line with full 32-kbit/s coding. Signaling information is transmitted over the ADPCM information; signaling messages are transmitted only when signaling transitions occur using the all-zeros code word not generated by the ADPCM algorithm for framing and error control. This technique allows the full capacity of the T-1 line to be used with 32 kbit/s encoding. The Transition Signaling format can be switched at DCS terminals or drop/insert terminals on 64 kbit/s (two-channel) boundaries in fractional T-1 applications.

Robbed-bit Signaling carries 48 channels in a T-1 stream. The signaling bits are carried in-band by changing the coding rate of each channel from 32 kbit/s to 24 kbit/s during each T-1 signaling frame and substituting a signaling bit for the unused ADPCM code bit. This slightly reduces the voice quality of the speech signal. This format cannot be switched at DCS systems and is not compatible with fractional T-1; it is provided primarily for compatibility with existing equipment.

The three signaling formats can be assigned on a bundle-by-bundle basis, although Robbed-bit Signaling has no application other than a full T-1 using all four bundles.

The bundle channel-control templates, which allow the transmission of 64 kbit/s "transparent" channels without ADPCM coding, 64 kbit/s channels with signaling, and 32 kbit/s channels with and without signaling are supported in all three signaling formats. In addition, 32 kbit/s transparent channels can be created. These bundle templates are implemented using channel control words.

.c.1.1 Operation Modes and Capacity

The ADPCM Line Formatter operates on either 24, 32, 48, or 60/64 channels. A system clock of 6.144 MHz, 8.192 MHz, 12.288 MHz, or 16.384 MHz is required for the respective rates. In addition, a "gapped clock" mode is available for 24 and 48-channel operation with system clock rates of 6.176 MHz and 12.352 MHz respectively; this mode allows direct connection to serial PCM and ADPCM signals at the T-1 line rate of 1.544 MHz. With any signaling format or channel rate, either an eight-bit parallel or a serial interface can be provided for the ADPCM line signals.

Both serial and parallel PCM interfaces are provided. The parallel PCM interface is unbuffered and has a four-channel delay between the input channel and the corresponding output channel in either the encoding or the decoding direction. The parallel interface is bidirectional and is used for both the ADPCM and PCM input and output signals.

The serial PCM interface for 24 and 48 channel operation uses a one-frame buffer of both the PCM input and PCM output to allow the formation of bundles and the implementation of "templates" described in ANSI document T1Y1/90-076. The one-frame buffers are required to reorder the PCM from each of two input T-1 sources to the encoded ADPCM output and from the ADPCM input to the decoded PCM outputs.

The templates allow the transmission of a mix of channels with signaling, with no signaling, and channels transmitted "transparently" at 64 kbit/s with or without signaling. Although the templates are specified only for the bundle format, they are also supported in the other two signaling modes.

Any channel can also be set for 32-kbit/s clear-channel operation. When this mode is selected, the four most significant bits of the PCM input are placed directly in the corresponding ADPCM time slot at the encoder. At the decoder, the four bits from the ADPCM time slot replace the four most significant bits of the PCM output. The other four bits are set to 0.

In the parallel PCM interface mode the input channel order to the ADPCM Line Formatter must correspond to the output channel order; however, signaling and transparent functions are still controllable. This mode is suitable for terminal applications that have a switching fabric to control the placement of the PCM signals in the desired order. The one-frame PCM input and output buffers are not used in this mode.

The serial PCM interface provided for 60/64-channel operation allows the implementation of the channel formats specified in CCITT recommendation G.761. This operation is provided with minimum delay. Signaling according to G.761 is not supported by the ADPCM Line Formatter.

The following table is a summary of the interface modes for the ADPCM Line Formatter:

Parameter	Number of channels 24	32	48	60/64
Clock Rate	6.144 MHz	8.192 MHz	12.288 MHz	16.384 MHz
Clock Gapping	yes, 6.176 MHz	no	yes, 12.352 MHz	no
Number of bundles	2	2	4	5
Serial PCM inputs	yes	no	yes	yes
Serial ADPCM inputs	no	no	yes	yes
Parallel PCM inputs	yes	yes	yes	yes
Parallel ADPCM inputs	yes	yes	yes	yes
ANSI Formats	yes	yes	yes	yes (parallel PCM)
G.761 Format	no	no	no	yes (serial PCM)

.c.1.2 Signaling Modes

Bundle Format signaling is available in all modes except 32-channel and 60/64-channel serial. When the serial interface is used in 24 or 48-channel operation, the templates described in T1Y1/90-076 can be implemented as well. When the parallel interface is used, the input channel order must correspond to the template format output, but all other Bundle Format features are implemented. (Typically the parallel interface is used in a digital terminal that has internal switching capability that can be used to obtain the channel ordering required). In 60/64-channel mode, the first 60 channels in the frame are organized into five bundles. The last four channels are unused.

Transition Signaling is available in all modes except 60/64-channel serial. In 60/64 channel mode signaling can be provided for all 64 channels.

Robbed-bit Signaling is available in all modes except 60/64-channel serial. However, since Robbed-bit Signaling is specified for 48-channel operation on T-1 lines and requires synchronization to the superframe alignment of those lines, it is applicable only to 24-channel and 48-channel operation. An external signaling superframe synchronization input, ZINSY, specifies the location of the signaling bits on the ADPCM input signal.

Transparent 64 kbit/s signals can be carried with or without signaling. In Bundle Format, PCM signaling is carried in the Delta Channel. In Robbed-bit Signaling and in Transition Signaling, transparent channels carry signaling only in the PCM robbed-bit signaling bit positions.

In the modes in which ANSI formats are available, Transition Signaling Format and Bundle Format can be selected on a bundle-by-bundle basis. This feature is useful in networks with fractional T-1 capability or where both types of signaling are needed.

Configuration, control and monitoring of the formatter is provided by a microcontroller, which monitors all status conditions and provides configuration control. The microcontroller can respond to commands through its internal UART or can be commanded remotely over a data link in applications in which one is available.

.c.1.3 Diagnostic Test of the ADPCM Processor

Brooktree has two ADPCM Processor products that interface to the ADPCM Line Formatter. Both are multichannel designs whose processing logic is shared among all channels. For that reason, a diagnostic test of any single channel in either product tests the processor for all channels, even those in service.

The ADPCM Line Formatter includes the capability of a diagnostic test of both the ADPCM encoder and decoder functions. The diagnostic test consists of independent sequences of 2048 test vectors for both the encoder and the decoder and is programmable from the microcontroller; the microcontroller loads the sequence from program memory to RAM through the integrated circuit. The test takes 250 ms to run, and can be run repeatedly on any idle channel, on any channel that is unused because the adjacent channel is run at 64 kbit/s (transparent, without ADPCM encoding), or on any channel that is used for the Delta Channel in Bundle Format.

The results of the diagnostic (pass or fail) is available at an external pin and in a status register that can be read by the microcontroller.

.c.1.4 Applications

An application of the ADPCM Line Formatter using the parallel PCM interface in 48-channel operation is illustrated in Figure 1. In this application the ADPCM Line Formatter provides a T-1 line signal carrying up to 48 channels of ADPCM-coded signals and providing Bundle Format signaling, Transition signaling, or Robbed-bit Signaling.

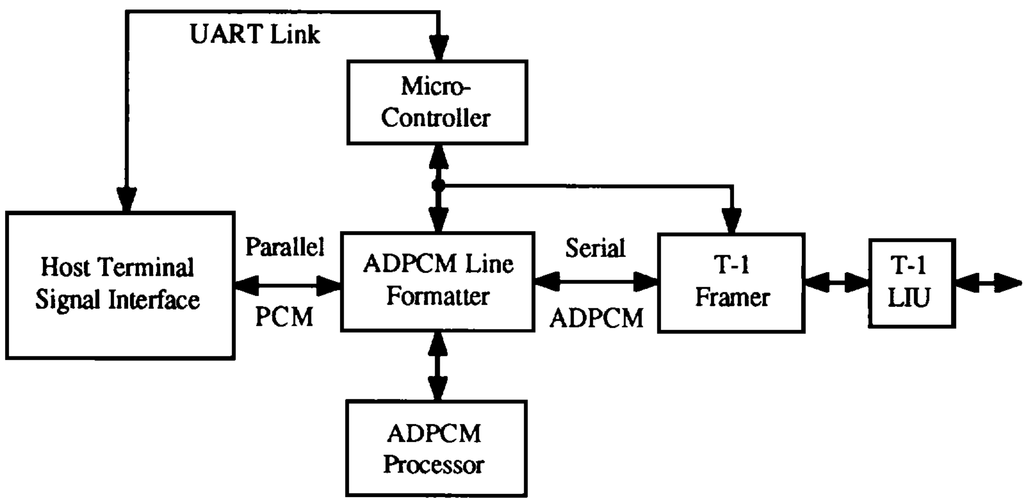

Figure 1. ADPCM Line Card Application

The formatter circuitry consists of a integrated circuit packaged in an 84-pin PLCC, an 8Kx8 static RAM, and a microcontroller with program memory. The microcontroller can also set latches to indicate alarm and status conditions via LED indicators, and can communicate through a serial data port in order to provide remote monitoring and control.

A transcoder application of the ADPCM Line Formatter is shown in Figure 2. In this application a Dual T-1 Framer, the ADPCM Line Formatter, the ADPCM Processor, and a Single T-1 Framer are used to provide the entire transcoding function. The ADPCM Line Formatter operates in 48-channel mode with serial PCM and ADPCM signal interfaces. The transcoder can operate using Bundle Format signaling, Transition Signaling, or ADPCM Robbed-bit Signaling. These signaling modes can be selected on a bundle-by-bundle basis.

.c.1.5 Block Diagrams

A functional block diagram of the ADPCM Line Formatter is shown in Figure 3. The top of the diagram shows the encoder processing of PCM and Signaling Inputs into the ADPCM Line Output. The PCM and the signaling information can be provided separately for encoder processing, with the signaling presented either at separate out-of-band signaling inputs or as idle signaling bits when the channel is set for idle signaling. The Encoder Processing block represents the circuitry that provides the ADPCM Line Output from the PCM signals, the signaling bits, and the formatter control signals. The ADPCM Line Output includes the coded PCM information and the signaling bits formatted as determined by the control options.

The path at the bottom of the figure is the signal path for the decoder direction. The Decoder Processing block consists of receiving the ADPCM Line Input signal, decoding the ADPCM to PCM, and removing the signaling information and formatting it for PCM transmission.

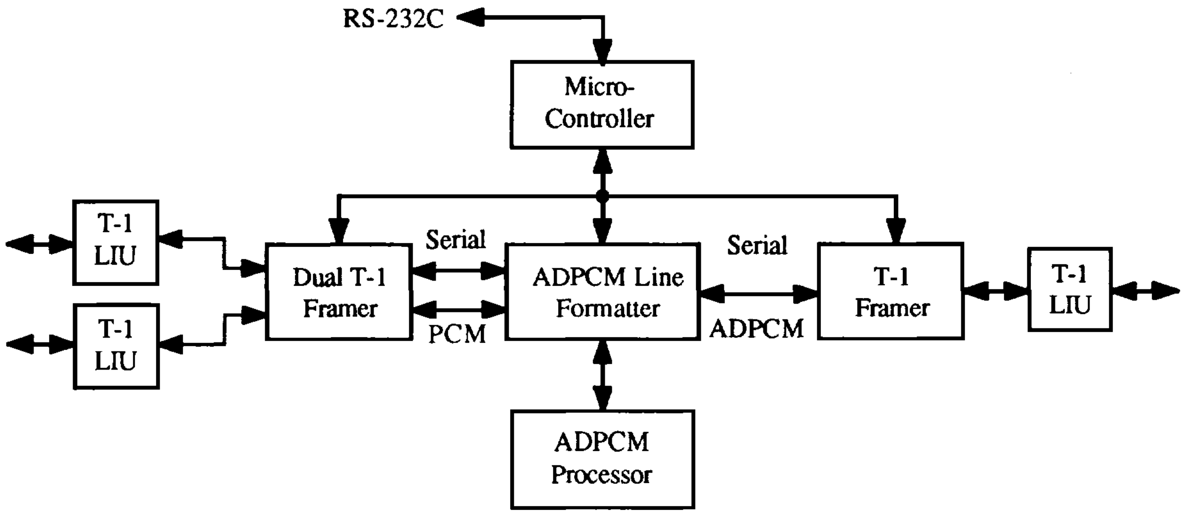

Figure 2. ADPCM Transcoder Application

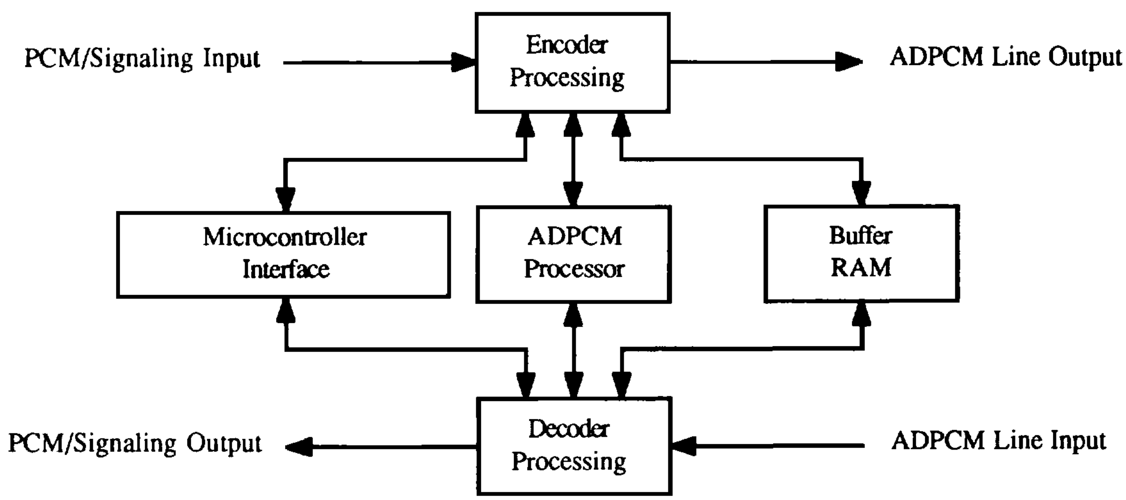

Figure 3. Functional Block Diagram

The microcontroller interface, the ADPCM Processor, and the Buffer RAM are each resources shared between the encoder processing and the decoder processing. The Buffer RAM locations include PCM signal buffers, signaling-bit buffers, control register locations, and other control and data buffers required by the individual signaling formats.

A more detailed block diagram of the formatter is shown in Figure 4. The two PCM serial input streams are designated "X " and "Y" and the ADPCM signals are designated "Z" per T1.302. All of the inputs are applied to a signal mux at the top of the figure. The two PCM serial input signals are stored in PCM Input Buffers to allow for bundle formatting. Parallel PCM signal inputs are applied directly to the multiplex. These two PCM streams are then multiplexed together with the incoming ADPCM stream and sent to the ADPCM processor. The compressed PCM and expanded ADPCM channels returning from the ADPCM processor are then demultiplexed to form the X, Y, and Z-port output signals.

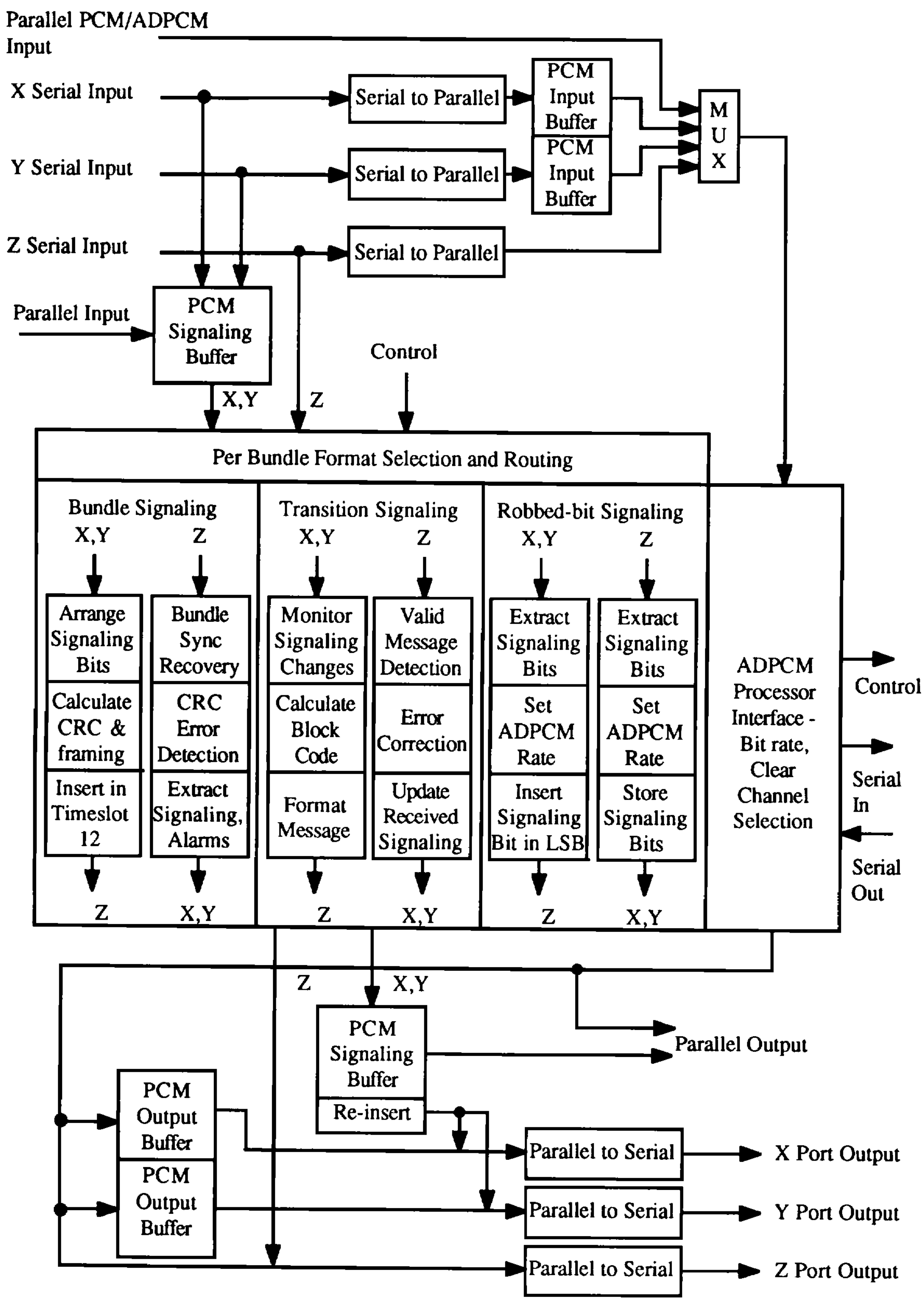

Figure 4. ADPCM Line Formatter Block Diagram

Signaling bit processing is performed concurrently with the ADPCM encoding and decoding. Three separate sets of processing logic are provided for the three signaling modes. Also included on the block diagram is the control circuitry for processing the delta channels if bundled mode is selected, or decoding signaling messages if transition signaling mode is selected.

The PCM Output Signals are then buffered for the inverse bundle "unformatting" operation required at the encoder. Signaling bits are inserted in the output PCM channels as required.

.c.1.6 Logic Diagram

A logic diagram is shown in Figure 5. Input pins are marked "I," output pins are marked "O," and bidirectional pins are marked "B."

The clock and mode controls set the input signal format and provide clock signal inputs and outputs. The input system clock is used to generate an output bit clock that defines the timing required for the serial inputs. A parallel-input enable control is provided for controlling the drivers to the parallel input/output signal bus.

The interface to the ADPCM Processor is defined in IS-110. AN-112 describes the configuration and timing used for 48-channel and 64-channel transcoder operation. The ADPCM Processor is driven by clock, synchronization, serial input, code-select, and control signals. The control signal provides control of transparent operation and of the algorithm reset function that is used in conjunction with the diagnostic testing. The ADPCM Processor has a single serial output.

The input and output section consists of serial input pins for the PCM and the signaling for the X and Y stream, serial inputs and outputs for the Z stream, and a parallel input/output bus for both the ADPCM and PCM inputs and outputs. When the serial PCM interface is used, the upper four bits of the parallel input/output bus are used for X and Y PCM and signaling stream outputs. An additional input is used to freeze the state of signaling at the Z port if there is an out-of-frame condition on that stream.

The microprocessor interface consists of five control signals, an eight-bit address/data bus, and one status output. The status signal, which indicates a failure of the ADPCM diagnostic when it is high, can be used to interrupt the microprocessor.

The ADPCM Line Formatter requires an 8Kx8 RAM for buffer storage and for storage of the diagnostic tables for the ADPCM Processor. The interface to this RAM consists of thirteen address signals, the read and write control signals, and an eight-bit bidirectional data bus.

.c.2.0 MICROCONTROLLER INTERFACE

The formatter is managed by a microcontroller. An integral interface to an Intel 8051-family processor or equivalent, or Motorola 68HC11-family or equivalent is provided (the 68HC11 requires an external quad-NAND part, 74HCT00, to decode read and write enable signals).

The integrated circuit is connected to the microcontroller exactly like static RAM. The microcontroller can read or write to two different kinds of registers within the framer circuit. "Direct" write operations are to latches in the circuit which contain mode control indicators. "Indirect" read and write operations are to memory locations in the RAM that is connected to the circuit. These locations contain information associated with particular channels of the two T-1 facilities being processed by the ADPCM Line Formatter.

.c.2.1 Signal Interface

The controller interface to the integrated circuit consists of thirteen pins: Address Latch Enable (ALE), Read Enable (~RD), Write Enable (~WR), Chip Select (CS), RAM Enable (RAMEN), and eight multiplexed address/data bits (AD7-AD0).

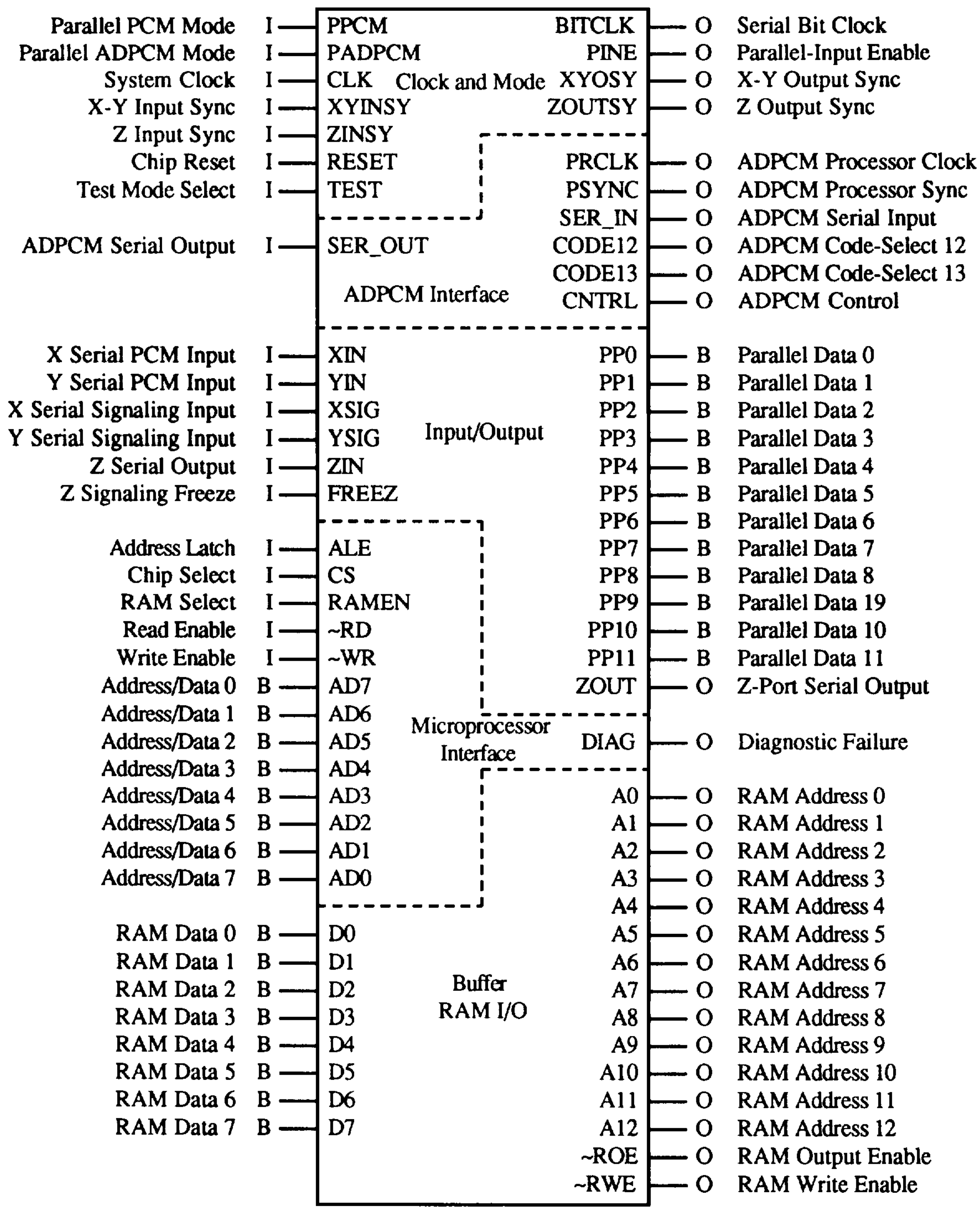

Figure 5
ADPCM Line Formatter Logic Diagram

The controller interface is designed to allow the direct connection of an Intel 8051-family or equivalent microprocessor. The Chip Select and RAM Enable inputs can be taken from two of the address inputs or from an address decoding circuit to establish any desired memory address range. The Chip Select input allows the control of multiple parts from a single microprocessor.

.c.2.2 8051 Controller Interface Timing

The interface for the 8051 Controller consists of the latch enable signal, the read enable signal, the write enable signal, the address bus (two pins from port P2) and the eight-bit address/data bus (port P0). The setup and hold times required for the latch enable and write enable signals are 10 ns. The ~RD low to valid-data-in time is less than 25 ns. Typically these times are less than required by any 8051-family microprocessor. Other processors can be used as well, as long as the multiplexed address/data bus feature of the 8051 is supported. More detailed timing information is given in section 9.4.

.c.2.3 Address Map

The address map for the controller is given in Table 1. There are three types of address space: Internal Control Registers, which can only be written; Internal Status Registers, which can only be read; and "indirect" RAM locations, which can be read or written. The Internal Control and Status Registers are in addresses 000-003 and 000-001 respectively. The are selected by setting the input RAMEN low.

The RAM space includes all addresses from 0000-1FFF (hex). The Chip Select (CS) input must be high to address the gate array or RAM and the RAM enable input (RAMEN) must be high to access the indirect RAM locations. The RAM is divided into pages of 256 bytes, and a page register is used to generate the upper five bits of the RAM address. This register is described in section 2.3.1.4.

2.3.1 Internal Control Registers

There are four internal control registers and two internal status registers, as shown in Table 2. The internal registers are latches within the gate array and are set by a write operation of the controller when the gate array chip select pin is high. The RAMEN pin must be low to access these latches instead of writing indirectly into RAM.

2.3.1.1 Mode Register

Figure 6 shows the individual bit functions of the Mode Register, which is located at address 00. Bits 0, 1, and 3 of this register are reserved for possible future functions and must be set to 0.

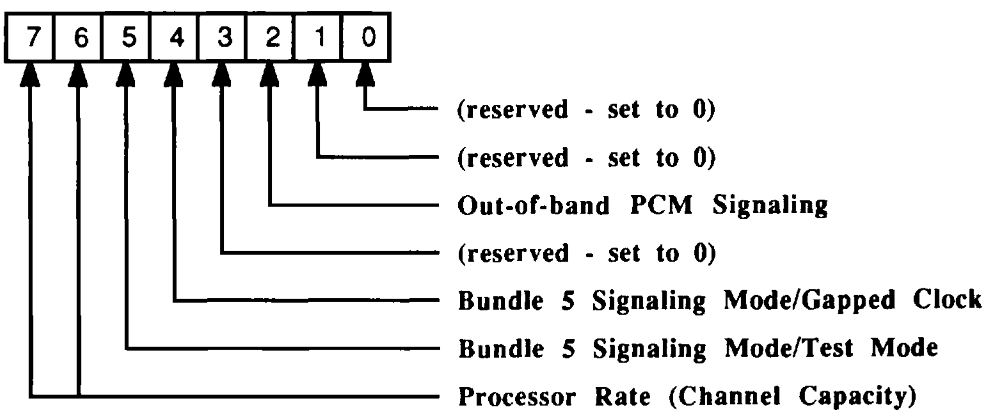

Figure 6. Mode Register Bit Functions

<u>Out-of-band PCM Signaling Input</u> is set if the incoming PCM channels do not contain signaling information in the robbed-bit positions. This implies that the incoming signaling is out-of-band and is being supplied on separate input pins (XSIG and YSIG in serial mode, PP11-PP8 in parallel mode). This bit is reset if the incoming channels have Robbed-bit Signaling.

Processor Rate selects the number of channels that will be processed. The number of channels selected can be 24, 32, 48, or 64 by setting bits 7 and 6 to 00, 01, 10, or 11 respectively.

Bundle 5 Signaling Mode specifies the type of signaling to be applied to the fifth bundle in 60/64 channel mode. The signaling types are discussed in Section 2.3.1.2. The Processor Rate must be set to 64 channels for this function to be active.

Gapped Clock selects gapped clock timing when in 24 or 48 channel mode. This allows a 6.176 MHz or 12.352 MHz clock to be used as the input clock. Frame bit gapping will automatically be inserted in the clock supplied to the ADPCM processor. This mode allows serial line rates of 1.544 MHz to be used at the serial PCM and ADPCM inputs and outputs. When this bit is not set, ungapped clock rates appropriate to the rate selected in bits 6 and 7 must be used. The Processor rate must be set to other than 64 channels for this function to be active.

Test Mode is used in manufacturing testing and must be set to 0. The processor rate must be set to other than 64 channels for this function to be active.

2.3.1.2 Bundle Register

Figure 7 shows the Bundle Register, which is located at address 01 and provides a bit pair to control the signaling format for each of the four primary bundles. When the bit pair is set to 00, no signaling is enabled; this mode is used for Bundle Format templates that have no delta channel provided. Bundle Format with delta channel is enabled for a bit pair of 01, Transition Signaling is enabled for a bit pair of 10, and Robbed-bit Signaling Format is enabled for a bit pair of 11. This allows each bundle to have a unique signaling format, if desired.

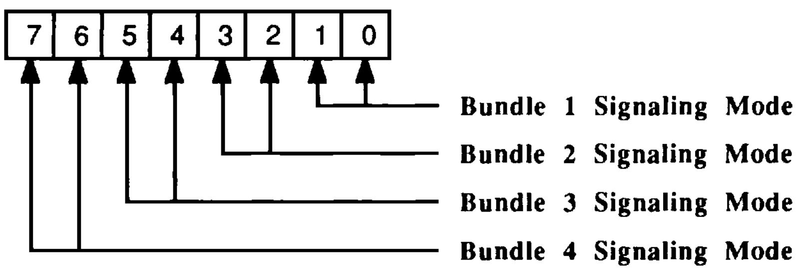

Figure 7. Bundle Signaling Mode Register

When 60/64 Channel Mode is used, the signaling format for the fifth bundle is specified by bits 4 and 5 of the Mode Register.

2.3.1.3 Template Register

Figure 8 shows the individual bit functions of the Template Register, which is located at address 02. A bit pair is used to specify which of the four groups of 12 incoming channels is to be the source for that particular bundle. Channels X1-X12 are selected by 00, channels X13-X24 are selected by 01, channels Y1-Y12 are selected by 10, and channels Y13-Y24 are selected by 11.

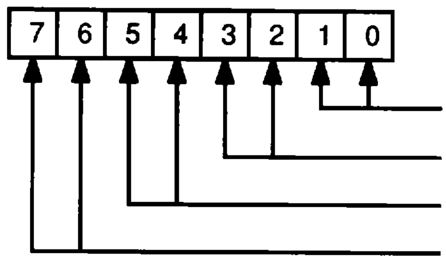

Figure 8. Template Register Bit Functions

The following table shows the contents of the Template Register used to implement specific templates given in T1Y1/90-076:

Template number per bundle 1	2	3	4	Template Register Contents (hex)
0-61	0-61	0-61	0-61	E4
63	62	0-61	0-61	E0
62	63	0-61	0-61	E5
0-61	0-61	63	62	A4
0-61	0-61	62	63	F4
0-61	63	62	0-61	D4
0-61	62	63	0-61	E8
63	62	63	62	A0
63	62	62	63	F0
62	63	63	62	A5
62	63	62	63	F5
63	63	62	62	50
62	62	63	63	FA

Note that the templates can be implemented only in 24-Channel and 48-Channel modes using the serial PCM interface. In 24-Channel Mode, only bundles 1 and 2 are implemented and only channels X1-X12 and X13-X24 are available as sources.

2.3.1.4 Page Register

The page register, shown in Figure 9, is located at address 03 and is provided to allow access to all of the 8K available RAM space. This register provides the upper 5 bits of address for accessing pages of 256 bytes each within the RAM. The address byte latched with ALE from the controller is appended to bits 4-0 of the Page register to derive the full 13 bit address to the RAM.

Bit 5 of the page register controls an "update function" of the MSB of the addressed data. If this bit is set, a read operation will replace the MSB of the location that is read with the MSB of the data word last written to the RAM. This function can be used in the implementation of Transition Signaling (See Sections 5.1.6.2, 5.1.6.4 and 5.1.6.6). It can be used for any address in RAM, however.

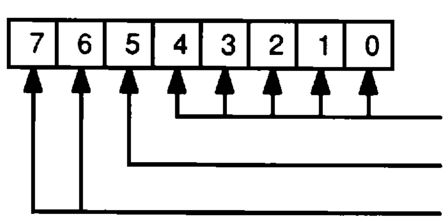

Figure 9. Page Register Bit Functions

2.3.2 Internal Status Registers

There are two internal status registers as shown in Table 2. The internal status registers are latches within the gate array and are read by the microcontroller when the gate array chip select pin is high. The RAMEN pin must be low to access these latches instead of reading from RAM.

2.3.2.1 CRC/OOF Register

Figure 10 shows the individual bit functions of the CRC/OOF Register, which is located at address 00. This provides status for bundles operating in Bundle Format with the Delta Channel provided. Each pair of bits provides status information for one bundle. The CRC/OOF Register should be read every 3 ms if an accurate count of CRC failure events is required.

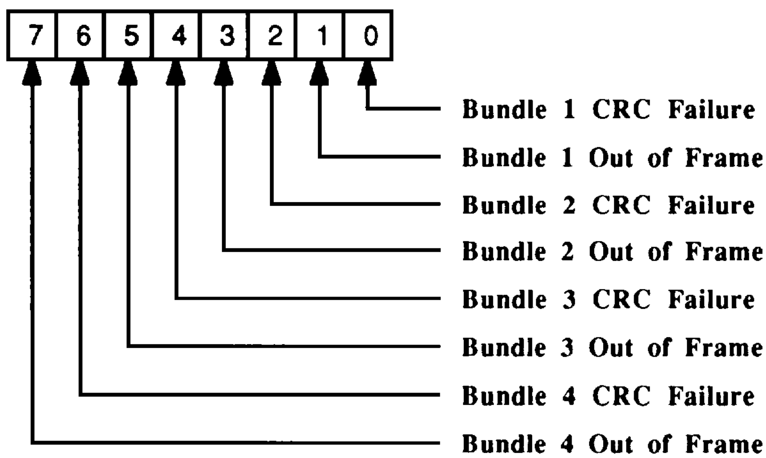

Figure 10. CRC/OOF Register Bit Functions

2.3.2.2 Bundle 5/ADPCM Status Register

Figure 11 shows the status register located at address 01. It contains status information for Bundle 5 and the result of the ADPCM Diagnostic test. The ADPCM Diagnostic Error bit is low if all encoder and decoder channels pass the diagnostic test and high if any one channel fails. The bit is updated every 250 ms.

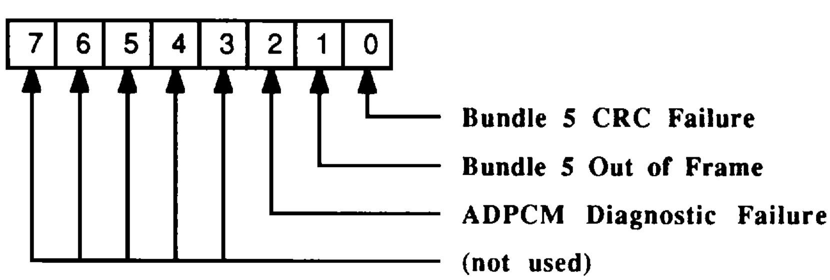

Figure 11. Bundle 5/ADPCM Signaling Mode Register

2.3.3 RAM Locations

The controller interface allows the writing and "indirect" reading of all locations in the static RAM associated with the part set. When a write operation is performed, the circuit latches the address and data and executes the write operation within the next 3.0 microseconds (with a 12.288 MHz input clock). When a read operation is performed, the address is latched, and the read operation takes place within the next 3.0 microseconds. A second read operation must then be performed to obtain the desired data at the controller. The five least significant bits of the page register select one of 32 possible 256-byte pages. Addresses are generated by loading the page register first with a value of 00H to 1FH, and then accessing the desired location with an address in the range 00H-FFH.

The minimum period between RAM operations is proportional to the input system clock. If a 6.144 MHz clock is used, the period is 6.0 µs. If a 16.384-MHz clock is used the period is 2.2 µs. This limitation applies only to read and write operations to the RAM locations; access to the internal control and status latches is limited only by the microcontroller speed.

The read operations can be "pipelined." If twenty-four locations are to be read, the first operation should have the address of the first location. On the second read operation, the second address is presented and the data corresponding to the first location is returned to the controller. In this way "N+1" operations are required to read "N" buffer locations.

Write operations may be interleaved with pipelined read operations.

If bit 5 of the page register (address 03) is set, the MSB of each byte read is replaced by the MSB last written to the RAM. The operation is exactly like a read operation except that the most-significant bit of the data last presented to the interface will replace the data in the buffer address after reading. (This operation is useful in the implementation of transition signaling).

The memory map of the buffer RAM is:

000-3FF	Per-channel Control/Signaling Registers
400-417	PCM Buffer - X Serial Input, Frame N
420-437	PCM Buffer - Y Serial Input, Frame N
440-47F	Encoder Signaling Buffer
480-497	PCM Buffer - X Serial Output, Frame N
4A0-4B7	PCM Buffer - Y Serial Output, Frame N
4C0-4FF	Decoder Signaling Buffer
500-517	PCM Buffer - X Serial Input, Frame N-1
520-537	PCM Buffer - Y Serial Input, Frame N-1
580-597	PCM Buffer - X Serial Output, Frame N-1
5A0-5B7	PCM Buffer - Y Serial Output, Frame N-1
5C0-5FF	Decoder Idle Signaling Buffer
700-7FF	STPQ Error Correction Lookup Table
800-1FFF	Diagnostic Test Input and Output Data

Since the PCM input and output buffers are used only in 24- and 48-channel operation, they only have 48 assigned addresses.

There are four types of per-channel buffer registers located in RAM. Each set of registers contains a buffer register for each channel. The functions of each type are:

- Channel Control and Working Registers
- PCM Input and Output Buffers
- PCM Signaling Buffers
- ADPCM Signaling Buffers

In addition to the per-channel registers above, there is an error-correction table for use with Transition Signaling and diagnostic test input and output data located in the remainder of the RAM. The error correction and diagnostic tables are available in the program ROM of the T-1 Transcoder Evaluation Board described in application note AN-201.

Within the Channel Control and Working Register range there are 16 registers for each channel. The offset (00-1F) within a group of 16 registers locates specific working registers for the channels. Details of the channel offset and the use of the control registers to establish templates are given in section 2.4.

2.3.3.1 Channel Control Registers

For each channel processed, there are two channel control registers, a low register and a high register. For all control bits except the signaling controls, the low control register controls encoder functions and the high control register controls decoder functions. The hex addresses of the low and high registers are nE and nF respectively, where n is the channel number (00H-3FH).

Figure 12 shows the bit functions of each channel control register. Some of the bits in the control register are for channels with an offset from the addressed channel, depending on whether the PCM interface is in serial or parallel mode.

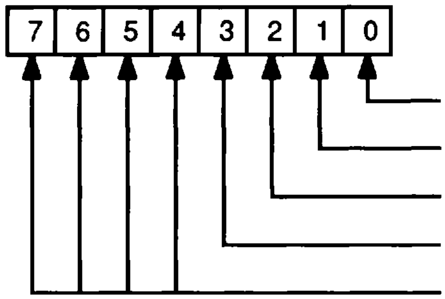

Figure 12. Channel Control Registers

Alternate Coding Table/64 kbit/s Transparent selects an alternate set of ADPCM coding tables for this channel. This may be used in data circuit applications where an optimized algorithm is available for voiceband data circuits. This bit controls the CODE13 signal of the ADPCM processor control interface. For channels that are set to be "transparent," this bit is set to provide 64 kbit/s transparent operation; this bit is set for the second channel of the ADPCM channel pair that makes up the 64 kbit/s transparent channel. If the Transparent Channel bit only is set, a 32 kbit/s transparent channel will be provided. (32-kbit/s transparent channels transfer the four most-significant bits of the 64 kbit/s input channel to the output). This control bit is normally set the same in both the low and high control register, to provide symmetrical operation between the encoder function and the decoder function.

Transparent Channel specifies that this channel is a transparent (32-kbit/s or 64-kbit/s) channel and therefore has no ADPCM compression or expansion. These channels are sent directly through the ADPCM processor without change (except for delay equal to the compressed channels). If 32-kbit/s transparent operation is set for the encoder, the four leading bits for the PCM word are transmitted (the sign and chord bits for PCM coding). If 32-kbit/s transparent is selected for the decoder, the bits in the ADPCM channel position are placed in the same bit locations and the four following bits are set to 0. This control bit is normally set the same in both the low and high control register.

Enable Signaling is set in the high control register to enable signaling on the ADPCM output for Transition Signaling format and for Robbed-bit Signaling format. It has no effect in Bundle Format (signaling is always provided in this format). In the low control register, this bit enables robbed-bit signaling-bit insertion to the PCM output streams in all signaling formats. The correspondence of this bit address to the affected channel is different in the various interface modes, so this bit will be set differently in the low and high control registers.

Signaling Idle is set to enable the insertion of an idle signaling code into the signaling bits of this channel. The low channel control word controls the decoder function, and the high channel word controls the encoder function. The correspondence of this bit address to the affected channel is different in the various interface modes, so this bit will be set differently in the low and high control registers.

Setting this bit of the high channel control word inhibits signaling updates to the PCM input signaling buffer. The desired idle code to be inserted in the ADPCM output is loaded into the PCM signaling buffers by the microcontroller.

Setting this bit of the low channel control word causes the output PCM signaling to be obtained from the PCM Output Idle Signaling buffers instead of the PCM Signaling buffers. See Table 5 for the buffer addresses.

PCM Channel Select is part of the timeslot interchange function for the template formats. These four bits are set to a value from 0-11 to select one of 12 channels (a 12 channel group is selected in the Template register) as a source for transmission to the ADPCM processor. These four bits are set to a value of 15 to denote that this channel is not used (idle) and to enable the diagnostic test on this channel.

In the 24-channel and 48-channel serial PCM modes, the value present in these bits determines the order that the PCM input channels are read out of the PCM input buffer in the encode direction or written into the PCM output buffer in the decode direction. These control bits are normally set the same in both the low and high control register. In all modes, setting the hex value of this field to F enables the diagnostic test of the ADPCM encoder or decoder on this channel.

2.3.3.2 PCM Input Buffer

The PCM input and output buffers are used with the PCM serial interface only. In 24 or 48-channel modes, the buffers are required to form the bundles from the serial inputs to meet the ANSI standard T1.302-1989. This will be referred to as ANSI mode. In 60/64 channel mode, the buffer delay is approximately six channel periods (23 µs) and the buffers are used to obtain the line format given in CCITT Recommendation G.761.

There are two frames of PCM Input buffering used for Bundle Format, starting at addresses 400 and 500 respectively. The one-frame buffers are alternately filled and emptied. For 48-channel ANSI format, the inputs are derived from an X T-1 port and a Y T-1 port. The X port signals fill the locations starting at 400/500 and the Y port fills the locations starting at 420/520. In 24-channel ANSI mode, only the X port signals are used. In 24-channel ANSI format, only the X port locations are used.

In each of these modes, to select a PCM channel for one of the ADPCM time slots available at the encoder output, the PCM Channel Select field is set to a value of 0-11 to select channels 1-12 of the corresponding input bundle. If two ADPCM time slots are to be set for 64 kbit/s transparent operation, the PCM Channel Select of the first location is set to F and the channel select for the second location is set to the desired PCM channel address. The Transparent Channel and the Alternate Coding/64-kbit/s Transparent control bits must be set for the second location as well. To comply with T1.302, only ADPCM channel pairs that correspond to a normal PCM channel time slot at the ADPCM encoder output can be selected for 64 kbit/s transparent operation.

In G.761 mode, the PCM input buffer is used to format the output for either compressed or transparent operation. The correspondence between the buffer locations and the channels processed is given in Table 3 and is discussed in section 2.4.1.3.

2.3.3.3 PCM Output Buffers

In ANSI modes, the PCM outputs are loaded in a buffer arrangement similar to the PCM inputs. The decoder PCM output buffers for the X PCM stream start at locations 480 and 580, and for the Y stream start at locations 4A0 and 5A0. Only the X PCM stream buffers are used in 24-channel mode.

If a decoder channel is in diagnostic mode, the PCM output is not written to a buffer (the write operation is replaced by a read operation to fetch the expected diagnostic result). Therefore PCM Output Idle codes can be provided on a per-channel basis by setting the decoder channel for diagnostics and then writing the desired idle code to the corresponding channel buffer addresses. For instance, if channels X5 and X6 are replaced by a 64 kbit/s transparent channel that appears in the Channel X5 time slot in the output, the desired idle code for channel X6 should be written to addresses 485 and 585 (hex).

The use of the buffers to obtain 60-channel operation according to G.761 is similar to the use of the encoder buffers. Only the buffer locations 480-487 are used. PCM idle codes for unused channels cannot be implemented in this case and must be provided by the accompanying primary-rate framer circuit.

2.3.3.4 Encoder Signaling Buffer

Encoder signaling refers to the signaling bits that arrive on the PCM input signals and are transmitted with the ADPCM signaling outputs. The encoder signaling buffers are used to accumulate signaling bits from the PCM inputs. Both in-band or out-of-band signaling modes are provided for serial and parallel PCM interfaces.

Idle signaling can be inserted in place of the input signaling for any channel by setting the Idle Signaling control bit in the high channel control word for that channel. This control bit will inhibit the update of the Encoder Signaling Buffer address for that channel. The desired idle signaling code can then be written to the buffer location from the controller. Note that the idle signaling function can be used in applications where signaling is locally generated and inserted in the ADPCM output via the controller.

Figure 13 shows the configuration of the Encoder Signaling Buffer registers. Each register contains a "current" and a "previous" location for each signaling bit. Every time a new signaling bit is loaded, it becomes the current signaling bit and the preceding current bit is moved to the previous signaling position. The current signaling bit is the only one used in Bundle Signaling and Robbed-bit Signaling. In Transition Signaling, both the "previous" and "current" bits are both used as described in section 6.1.5.1.

When signaling is set idle, both the current and the previous bit positions should be set to the desired signaling bits. In transition signaling, this will cause the immediate transmission of a signaling message if the idle signaling state is different than the "stable" state contained by the transition signaling message buffer. Also, this function is used to inhibit signaling in the Transition Signaling format but still allow the sending of alarm messages.

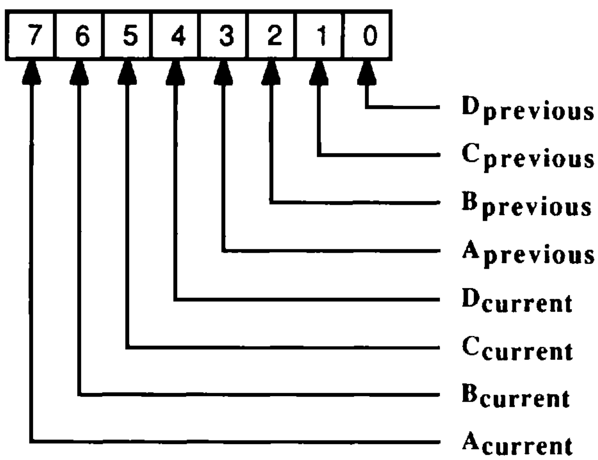

Figure 13. Encoder Signaling Buffer Configuration

The Encoder Signaling Buffer addresses start at 440 and are consecutive according to channel number. When parallel PCM inputs are used, the encoder signaling buffers are in consecutive locations according to the input order. When serial PCM inputs in ANSI modes are used, the Encoder Signaling Buffers are located as follows:

Channel Range	Address Range
X1-X12	0440-044B
X13-X24	044C-0457
Y1-Y12	0458-0463
Y13-Y24	0464-046F.

2.3.3.5 Encoder Signaling Buffer Updates

The Encoder Signaling Buffer can be updated with either in-band or out-of-band signaling with either the serial or the parallel PCM interface.

In-band signaling is obtained from the least-significant bit of the PCM word every sixth frame as described in T1.302 for the X and Y port signals. Each signaling bit position will be updated every 3 ms.

Out-of-band signaling in serial mode is accomplished by taking the bits for the XIN and the YIN PCM signals from the XSIG and YSIG inputs respectively. The A, B, C, and D signaling bits must be inserted in the same time slots as the four least-significant PCM bits (bits 5, 6, 7, and 8). Out-of-band serial signaling bits are updated every frame if the corresponding bundle is in Bundle Format or Robbed-bit Signaling Format. Each bit is updated every 3 ms at robbed-bit signaling times if the corresponding bundle is in Transition Signaling format to allow the proper functioning of the "current" and "previous" signaling information.

Out-of-band encoder signaling updates with parallel PCM inputs are under external control. A control bit corresponding to each signaling bit causes that signaling bit to be updated in that frame. The following format is used:

Signaling Bit	Bit Position	Bit Update Control
A	PP11	XIN
B	PP10	XSIG
C	PP9	YIN
D	PP8	YSIG.

If the signaling bits are present every frame with the PCM sample, the update controls can be set high constantly for Bundle Format and Robbed-bit Signaling. If this is done in Transition Signaling mode, one or two additional signaling messages may be sent at signaling bit transitions. It is not expected that this will be a problem, but the additional signaling messages can be avoided by only updating the signaling bits once every 1.5 ms or 3 ms.

2.3.3.6 Decoder Signaling Buffers

Decoder Signaling refers to the signaling information that arrives with the ADPCM input signal and is provided with the PCM output signals. The Decoder Signaling Buffer accumulates signaling bits from the ADPCM input signal. These bits are output as out-of-band signaling bits with the PCM outputs and will be inserted in the robbed-bit signaling positions in any channel for which the Signaling Enable bit of the low channel control word is set. The decoder signaling buffer updates are inhibited in any signaling mode when the "FREEZ" input is set high indicating an out-of-frame or other maintenance problem on the ADPCM input T-1.

In ANSI modes, the decoder signaling buffers are filled for any channel that is in a bundle which is set to a signaling format. The signaling information is inserted in the output PCM signal only if the Signaling Enable bit of the low channel control word for that channel is set but is always available at the out-of-band signaling output.

Figure 14 shows the format for the Decoder Signaling Buffer registers. In Bundle and Robbed-bit Signaling formats, the upper four bits are the most recently received signaling bits and the lower four bits are the corresponding bits from the previous ESF superframe. If the signaling freeze input FREEZ is high or there is a bundle out-of-frame condition in bundle format, the "old" bits automatically replace the "new" bits and are held until the alarm condition clears. In Transition Signaling Format, the upper four bits consist of a status bit that is set when a new message is been received and the three alarm bits M1, M2, and M3. The lower four bits are the signaling bits most recently received.

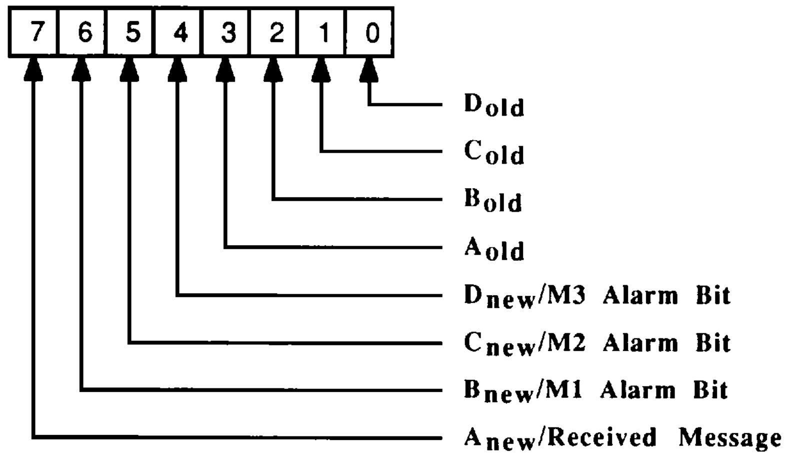

Figure 14. Decoder Signaling Buffer Configuration

There is also a separate Decoder Idle Signaling Buffer. If the Signaling Idle control bit of the low channel control word is set for a channel, its decoder output signaling is read from a different buffer. The lower four bits of that buffer should be loaded with the required idle signaling bits.

The decoder signaling buffers are located in consecutive addresses starting at 4C0. For ANSI 24-channel and 48-channel modes, the signaling buffers for the four bundles are located as follows:

Channel Range	Active Buffer Address Range	Idle Buffer Address Range
X1-X12	04C0-04CB	05C0-05CB
X13-X24	04CC-04D7	05CC-05D7
Y1-Y12	04D8-04E3	05D8-05E3
Y13-Y24	04E4-04EF	05E4-05EF.

.c.2.4 Channel Control Word Settings

The channel control words are used to establish the templates, signaling activity, and idle channel and diagnostic activity for the ADPCM Line Formatter. Templates control the formatting of the output signals, including whether channels are transmitted as 64 kbit/s clear channels. Their application is different for the serial and the parallel PCM interface and for ANSI T1.302 and CCITT G.761 line formats.

There are two channel control words for each PCM time slot processed. For each time slot, these are separated into a low channel control word and a high channel control word. The correspondence between the address of the control word and the channel controlled by that word depends on both the mode that the formatter is in and the particular bit of the word.

The upper four bits of the channel control word are the PCM Channel Select word. When the Serial PCM interface mode is used, these four bits are used as an address to map a PCM input buffer location to the ADPCM encoder input and the ADPCM decoder output to a PCM output buffer location. Thus the address corresponds to an ADPCM stream time slot and the four-bit contents to a PCM encoder input or decoder output time slot. When the parallel PCM input is used, the PCM time slots appear in the ADPCM output in the same order as they are applied to the input. In ANSI mode, this control word is used to set up the "templates" that are provided; in G.761 mode, these bits control the timing of the output and are altered to implement transparent channels. These bits also control the implementation of the diagnostics; when the bits are set to F (hex), the corresponding channel is set to diagnostic mode. The ADPCM Processor runs a diagnostic input sequence stored in RAM on either the encoder or the decoder and checks the output.

The transparent channel and alternate coding/64-kbit/s transparent bits control the ADPCM processor on a per-channel basis. These two control bits are located in the order of the channels as they appear on the ADPCM encoder output and decoder input with no channel offset.

The high control signaling enable and signaling idle is in the order of the channels as they appear at the encoder ADPCM output for Robbed-bit signaling and Transition signaling and is in the order of the channels as they appear at the encoder PCM input for bundle signaling. The low channel control decoder signaling enable is in the order of the PCM output channels and are interleaved between the X and Y port signals (X1, Y1, X2, Y2, etc.). Further details are given below and in each signaling section.

Each section below describes the use of the channel control word for each operating mode.

2.4.1 Buffered Serial PCM Interface

When the serial PCM interface is used, the PCM inputs and outputs are buffered to allow the formation of bundles and specified templates from different serial streams. In 24-channel and 48-channel mode, ANSI T1.302 line and signaling formats are supported. In 60/64-channel mode, the CCITT G.761 line format is supported.

The low channel control word upper 4 bits contain an address from 0-11 to specify a channel from the PCM Input Buffer to be sent to the ADPCM processor. The transparent channel bit and the alternate coding/64-kbit/s transparent bit control the ADPCM processor for this channel. The signaling enable bit (bit 2) in this control word is used for the PCM output channels, is interleaved, and starts with channel 0 (Xout 1). The signaling idle bit (bit 3) is also used for the PCM output channels, is interleaved, but must anticipate the output channel by one timeslot and therefore starts with channel Xout 2.

The high channel control word upper 4 bits contain an address from 0-11 to specify where in the PCM Output Buffer to store the reconstructed PCM data coming from the ADPCM processor. The coding and transparency bits control the processor for this channel. Since the ADPCM channels are normally 4 bits each, two of these channels will occupy the 8 bit timeslot in the incoming Z-port stream. Therefore, these channels are designated as high (H) and low (L) channels for the corresponding timeslot. The signaling enable bit in this control word is used for the PCM input channels and is in the same order that the channels are presented to the ADPCM processor. The signaling idle bit is also used for the PCM input channels but are interleaved.

When a 64 kbit/s transparent channel is specified, it must be present in an odd channel slot when delivered to the ADPCM processor. The previous even channel slot will then be unused and can be designated as a diagnostic channel. Unused channels are designated by setting the template bits (upper four bits) in a channel's control word to a value of 15 (hex value F).

2.4.1.1 48-Channel Serial PCM Control for ANSI T1.302

The low channel control words for 48-channel serial mode are as follows, where the XOUT and YOUT refer to the channels position in the X and Y output PCM streams and the PCM "n" channel is the channel position in the serial input to the ADPCM processor. This ordering also corresponds to the channel output ordering on the Z ADPCM stream output ZOUT, except that channels set for 64 kbit/s transmission can take two consecutive ADPCM time slots. These time slot assignments can be seen in the function timing diagrams that are described in section 3.

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00E	PCM 0	XOUT 2	XOUT 1	PCM 0
01E	PCM 1	YOUT 2	YOUT 1	PCM 1
02E	PCM 2	XOUT 3	XOUT 2	PCM 2
03E	PCM 3	YOUT 3	YOUT 2	PCM 3
:	:	:	:	:
2EE	PCM 46	XOUT 1	XOUT 24	PCM 46
2FE	PCM 47	YOUT 1	YOUT 24	PCM 47

The low channel control word signaling bits affect decoder signaling functions. All other bits control encoder functions. The template control words provide the template control for the PCM input channels applied to the ADPCM encoder. Each control address determines the function for a particular channel slot at the ADPCM Processor output, and the template field will select a particular PCM channel from the bundle input.

When bundle signaling is implemented, the template contents of the delta channels (normally 0BE and 0BF for channel X12, 17E and 17F for channel X24, 23E and 23F for channel Y12, 2FE and 2FF for channel Y24) must be set to an F. The ADPCM output corresponding to this location is overwritten with the "delta channel" that contains the bundle signaling.

The alternate coding and the transparent channel control bits have the same correspondence to formatted channels as the template control.

The signaling control bits act on the X and Y output channels directly as shown. The Signaling Enable control bits enables robbed-bit signaling to be inserted in the proper positions in the PCM outputs; the Idle Signaling control bits cause that signaling to be selected from the idle-signaling buffer instead of the active-signaling buffer. The desired idle signaling pattern can be written to the proper location of the decoder idle signaling buffer; these addresses are given in Table 5.

The high channel control words for 48-channel serial mode control the following functions:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00F	ADPCM 0H	XIN 1	XIN 1/PCM 0	ADPCM 0H
01F	ADPCM 0L	YIN 1	XIN 2/PCM 1	ADPCM 0L
02F	ADPCM 1H	XIN 2	XIN 3/PCM 2	ADPCM 1H
03F	ADPCM 1L	YIN 2	XIN 4/PCM 3	ADPCM 1L
:	:	:	:	:
2EF	ADPCM 23H	XIN 24	YIN 23/PCM 46	ADPCM 23H
2FF	ADPCM 23L	YIN 24	YIN 24/PCM 47	ADPCM 23L

The template and alternate coding/transparency control bits act on the ADPCM input channels as they are applied to the decoder. They have the same functions in the decoder section that the contents of the low control words have on the encoder. These control bits are set the same in the two control words in normal operation.

The Enable Signaling bit has two different operating modes. In Bundle Signaling format, it operates on the twelve channels of the bundle being processed in that order. This allows the signaling for all channels to be passed. The ordering shown is for the nominal bundle assignment, where X1-X12 is assigned to the first six channels of the Z PCM stream, and Y13-Y24 is assigned to the last six channels.

In Robbed-bit Signaling and Transition Signaling mode, the control bit operates on the PCM channels in the order that they are presented to the ADPCM Processor. This allows the correct signaling function to be associated with the ADPCM output from the encoder.

The Signaling Idle bit operates directly on the encoder PCM inputs as shown. This bit inhibits the updating of the input signaling buffer as the PCM input is applied to the encoder buffer circuitry. In bundle mode, the channels corresponding to the delta channels (X12, X24, Y12, and Y24) must all be set idle. The corresponding signaling buffer locations are used for insert alarm bits on the delta channels. This function is discussed further in section 4.

2.4.1.2 24-Channel Serial PCM Control for ANSI T1.302

Channel control word addresses above 17F are not used in the 24 channel mode. Only the X port is used as a PCM input and outputs in this mode. The functions of the bits are the same as for 48-channel mode, described above. A functional timing diagram for this mode is given in Figure 19.

The low channel control words for 24-channel serial mode are as follows:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00E	PCM 0	XOUT 3	XOUT 1	PCM 0
01E	PCM 1	XOUT 4	XOUT 2	PCM 1
02E	PCM 2	XOUT 5	XOUT 3	PCM 2
03E	PCM 3	XOUT 6	XOUT 4	PCM 3
:	:	:	:	:
2EE	PCM 22	XOUT 1	XOUT 23	PCM 22
2FE	PCM 23	XOUT 2	XOUT 24	PCM 23

The high channel control words for 24-channel serial mode are as follows:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00F	ADPCM 0H	XIN 1	XIN 1/PCM 0	ADPCM 0H
01F	ADPCM 0L	XIN 2	XIN 2/PCM 1	ADPCM 0L
02F	ADPCM 1H	XIN 3	XIN 3/PCM 2	ADPCM 1H
03F	ADPCM 1L	XIN 4	XIN 4/PCM 3	ADPCM 1L
:	:	:	:	:
16F	ADPCM 11H	XIN 23	XIN 23/PCM 22	ADPCM 11H
17F	ADPCM 11L	XIN 24	XIN 24/PCM 23	ADPCM 11L

2.4.1.3 60/64-Channel Serial PCM Control for CCITT G.761

In 60/64-channel serial mode, 8 buffer locations are sufficient to enable the timeslot arrangement called for in the G.761 standard. The write addresses for both the PCM Input Buffer and the PCM Output Buffer are fixed. The upper four bits of the control words will therefore contain a read address from 0-7 to properly order the channels for ADPCM processing in the encode direction (and to descramble them in the decode direction). The coding and transparency bits are associated with the channel where they are located. The signaling idle and enable bits are not used in 60/64-channel mode. Table 3 shows the addresses that enable the G.761 format. The least significant 4 bits of the 40X and 48X addresses come from the corresponding channel control word.

The channels specified in G.761 that are transparent channel candidates (6A, 6B, 22A, 22B, etc.) fall on odd channel slots in the table and can therefore be set as transparent with the bottom two bits in the control word. These transparent channels will fall in the proper stream C timeslot as specified in G.761.

2.4.2 Unbuffered Parallel PCM Interface

The unbuffered parallel PCM interface is for application in digital terminals that have an internal capability for switching and ordering PCM input channels. In this application, the ADPCM output channel ordering does not change from the PCM input, and the PCM output ordering from the decoder does not change from the ADPCM input. The PCM Input/Output Channel Select bits are used only to define diagnostic channels.

This interface can be used for either ANSI T1.302 or CCITT G.761 ADPCM signal formats. However, the input ordering that is required on the output must be provided by the host interface. The ADPCM Line Formatter can then provide ADPCM coding and transparent channels as required.

Only ANSI signaling formats are supported. Two bundles can be provided for 24-channel and 32-channel operation; in 32-channel operation the two bundles consist of the first 24 channels processed. Four bundles are provided in 48-channel operation and five bundles are provided in 60/64-channel operation. The five bundles consist of the first 60 channels processed. Robbed-bit Signaling is not supported in 32-channel and 60/64-channel mode.

The functions of the control words are listed in the tables below. The only function of the template word is to set the corresponding channel to diagnostic mode. On the encoder side, this function will force the ADPCM output to be all 1s. On the decoder side, the output will be a PCM idle code of 7F (hex).

2.4.2.1 48-Channel Parallel PCM Control for ANSI T1.302

The 48 PCM channels are numbered 0-47 and are applied at the PCM input to the encoder sequentially. Only the channels PCM 1, PCM 3, etc., can be transmitted as 64-kbit/s transparent channels.

The low channel control words control the following channels:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00E	PCM 0	ADPCM 22H	ADPCM 22H	PCM 0
01E	PCM 1	ADPCM 22L	ADPCM 22L	PCM 1
02E	PCM 2	ADPCM 23H	ADPCM 23H	PCM 2
03E	PCM 3	ADPCM 23L	ADPCM 23L	PCM 3
:	:	:	:	:
2EE	PCM 46	ADPCM 21H	ADPCM 21H	PCM 46
2FE	PCM 47	ADPCM 21L	ADPCM 21L	PCM 47

The template is used only to enable diagnostics. The signaling control functions have the same functions as for the serial interface.

The high channel control words are:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00F	ADPCM 0H	PCM 0	PCM 0	ADPCM 0H
01F	ADPCM 0L	PCM 1	PCM 1	ADPCM 0L
02F	ADPCM 1H	PCM 2	PCM 3	ADPCM 1H
03F	ADPCM 1L	PCM 3	PCM 4	ADPCM 1L
:	:	:	:	:
2EF	ADPCM 23H	PCM 46	PCM 46	ADPCM 23H
2FF	ADPCM 23L	PCM 47	PCM 47	ADPCM 23L

2.4.2.2 24-Channel Parallel PCM Control for ANSI T1.302

Channel control word addresses above 17F are not used in 24-channel mode. The 24 PCM channels are numbered 0-23 and are applied at the PCM input to the decoder sequentially. Only the channels PCM 1, PCM 3, etc., can be transmitted as 64-kbit/s transparent channels.

The low channel control words control the following channels:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00E	PCM 0	ADPCM 10H	ADPCM 10H	PCM 0
01E	PCM 1	ADPCM 10L	ADPCM 10L	PCM 1
02E	PCM 2	ADPCM 11H	ADPCM 11H	PCM 2
03E	PCM 3	ADPCM 11L	ADPCM 11L	PCM 3
:	:	:	:	:
16E	PCM 22	ADPCM 9H	ADPCM 9H	PCM 22
17E	PCM 23	ADPCM 9L	ADPCM 9L	PCM 23

The high channel control words are:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00F	ADPCM 0H	PCM 0	PCM 0	ADPCM 0H
01F	ADPCM 0L	PCM 1	PCM 1	ADPCM 0L
02F	ADPCM 1H	PCM 2	PCM 3	ADPCM 1H
03F	ADPCM 1L	PCM 3	PCM 4	ADPCM 1L
:	:	:	:	:
16F	ADPCM 11H	PCM 22	PCM 22	ADPCM 11H
17F	ADPCM 11L	PCM 23	PCM 23	ADPCM 11L

2.4.2.3 60-Channel Parallel PCM Control for ANSI T1.302

In bundle mode, the first 60 channels are used to form five 12-channel bundles. In transition signaling mode, all 64 channels may be used. Robbed-bit signaling is not supported in 60/64-channel mode, as there is no way to guarantee a common signaling multiframe reference in this application.

The low control word controls the template (which is used only to set channels to diagnostic mode) and coding/transparency for the encoder and signaling functions for the decoder.

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00E	PCM 0	ADPCM 30H	ADPCM 30H	PCM 0
01E	PCM 1	ADPCM 30L	ADPCM 30L	PCM 1
02E	PCM 2	ADPCM 31H	ADPCM 31H	PCM 2
03E	PCM 3	ADPCM 31L	ADPCM 31L	PCM 3
:	:	:	:	:
3EE	PCM 62	ADPCM 29H	ADPCM 29H	PCM 62
3FE	PCM 63	ADPCM 29L	ADPCM 29L	PCM 63

The high channel control words are:

Control Address	Template	Signaling Idle	Enable Signaling	Coding/Transparency
00F	ADPCM 0H	PCM 0	PCM 0	ADPCM 0H
01F	ADPCM 0L	PCM 1	PCM 1	ADPCM 0L
02F	ADPCM 1H	PCM 2	PCM 3	ADPCM 1H
03F	ADPCM 1L	PCM 3	PCM 4	ADPCM 1L
:	:	:	:	:
3EF	ADPCM 31H	PCM 62	PCM 62	ADPCM 31H
3FF	ADPCM 31L	PCM 63	PCM 63	ADPCM 31L

Note that for bundle mode, the last four channels are not used. Each of their template controls should be set to F, which will put them in diagnostic mode.

.c.3.0 DATA INTERFACES

In addition to the required clock and initialization inputs, the formatter has three primary data interfaces: the PCM Signal Interface, the ADPCM Signal Interface, and the ADPCM Processor Interface. The ADPCM Interface is largely transparent in any application, as the controls from the ADPCM Line Formatter automatically set the ADPCM Processor for the appropriate operation.

The description of the PCM and ADPCM signal inputs is given in terms of the ANSI T1.302 notation where the full-rate PCM ports are designated X and Y and the ADPCM port is designated Z. In CCITT G.761, these notations are A, B, and C respectively.

.c.3.1 Clocks and Synchronization

The circuit has a clock input which must be supplied with a 6.144 MHz, 12.288 MHz, or 16.384 MHz square wave, depending on the channel capacity selected in the mode register. If gapped clock mode is selected for 24 or 48 channel operation, then the input frequency is 6.176 MHz or 12.352 MHz. The clock must have a duty cycle between 45% and 55%.

The clock input is divided by 8 to obtain a bit clock for the incoming serial PCM or ADPCM signals. This clock signal is provided at an output pin and will be 768 kHz, 1.536 MHz (1.544 MHz if gapped mode is selected), or 2.048 MHz depending on the input clock frequency.

A timing diagram for the clock signals for 48-channel operation is shown in Figure 15. The reset signal is active low. After the reset signal transitions to a high state, the PCM bit clock output (divide-by-8 for 48 or 60/64 channel modes) will become active on the fourth rising edge of the input clock.

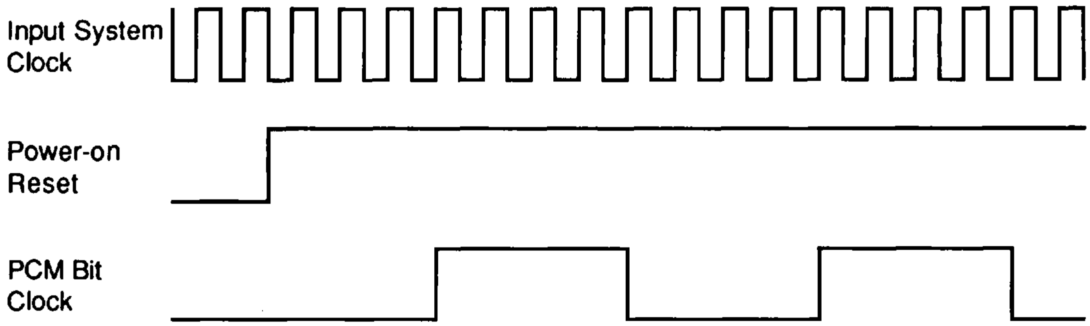

Figure 15. Clock Signals

.c.3.2 PCM Port Interfaces

The interfaces for the full-rate PCM data streams can be either parallel or serial. A low level on the PCM Parallel Select input PPCM enables the frame-buffered serial inputs while a high level on the select input enables the unbuffered, parallel inputs. Pin functions for the parallel and serial modes are given in Table 4. Timing diagrams for these interfaces for 48-channel capacity are shown in Figure 16 using an ungapped clock and in Figure 17 using a gapped clock. Figures 18 and 19 are the timing diagrams for 24-channel operation.

Timing for 60/64-channel operation with serial PCM inputs (to obtain the G.761 format) is given in Figure 20. Timing for 60/64 channel operation with parallel PCM inputs is given in Figure 21. Timing for 32-channel operation is given in Figure 22.

Each timing diagram shows the system clock CLK and the serial bit clock BITCLK. XYINSY is the input synchronization signal; it is an ESF superframe synchronization signal with a rising edge at the first bit of the first frame of the superframe. The timing diagram shows the beginning of a new superframe, so that the XYINSY transition is shown.

The strobe signal is an internal signal that samples the parallel inputs. PINE is the Parallel Input Enable signal; its rising edge should be used to latch the parallel outputs from the formatter and the parallel inputs to the formatter should be enabled when PINE is high. PP is the parallel signaling bus; the timing diagram shows the approximate period when the outputs are valid.

PRCLK, SER_IN, and SER_OUT are interface signals to and from the ADPCM Processor. The timing diagram shows the gapped clock to the processor as required.

The last lines show the serial PCM inputs and outputs. In 24-channel and 48-channel operation, the XIN, YIN, XOUT, YOUT, and ZIN signals are all synchronized. The ZOUT signal has a delay of about two PCM channel periods.

One PCM ESF superframe sync input, XYINSY, is provided for frame synchronization of all three PCM inputs. XYINSY should have a rising edge at the beginning of the first bit of each superframe (24 frames). The serial PCM inputs and XYINSY are sampled by the falling edge of the bit clock. The first bit of a frame is defined as the most-significant bit of the first PCM channel in ungapped mode and as the frame bit in gapped mode. Regardless of which input mode is selected, the X and Y port PCM outputs are always available on the parallel bus.

A multiframe synchronization signal ZINSY is provided to indicate signaling-bit alignment for robbed-bit ADPCM inputs. This signal occurs at the end of the "D" bit signaling frame. If Robbed-bit ADPCM signaling is not used, the ZINSY signal must be connected to ground.

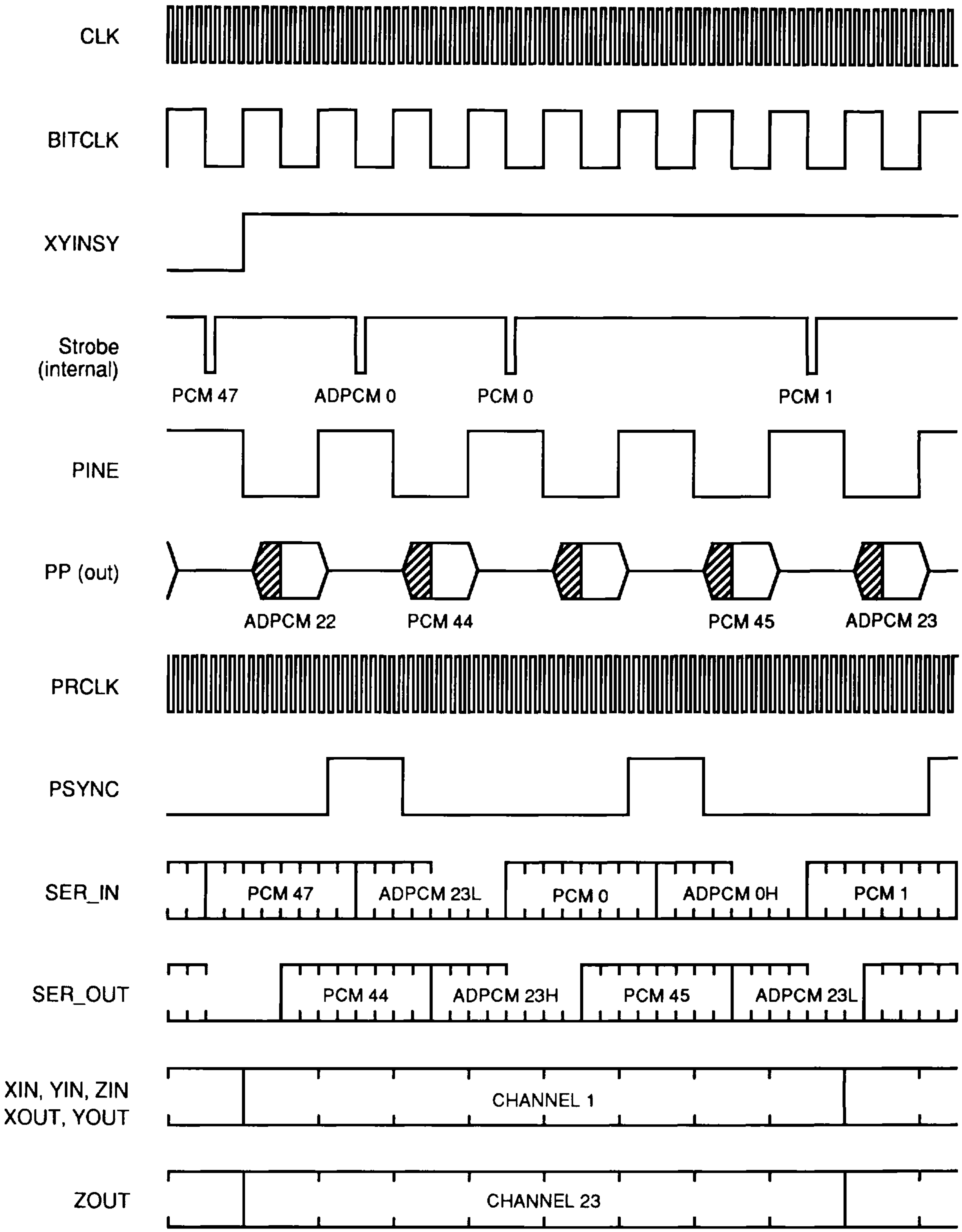

Figure 16. Timing Diagram for 48-Channel Ungapped Mode

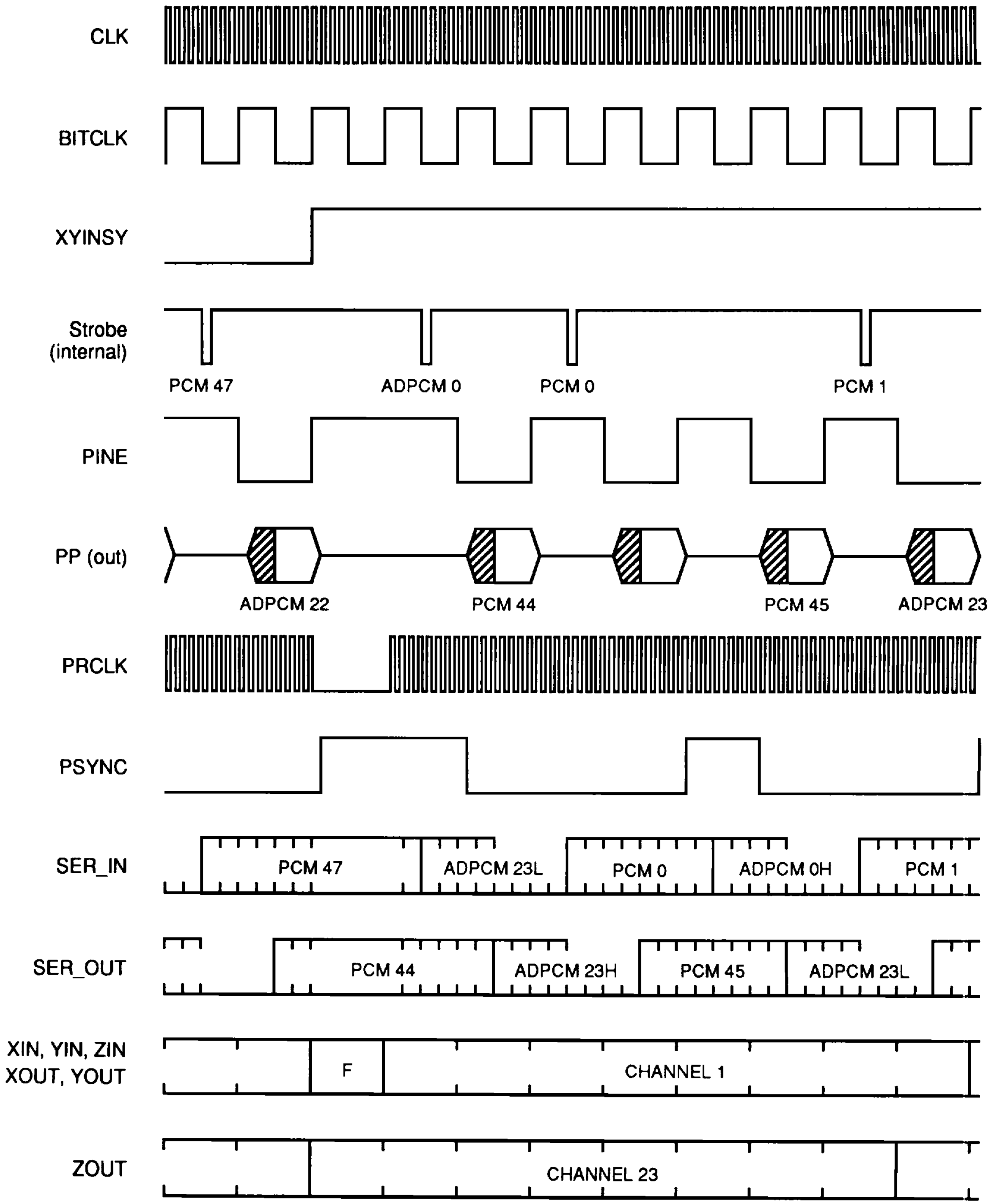

Figure 17. Timing Diagram for 48-Channel Gapped Mode

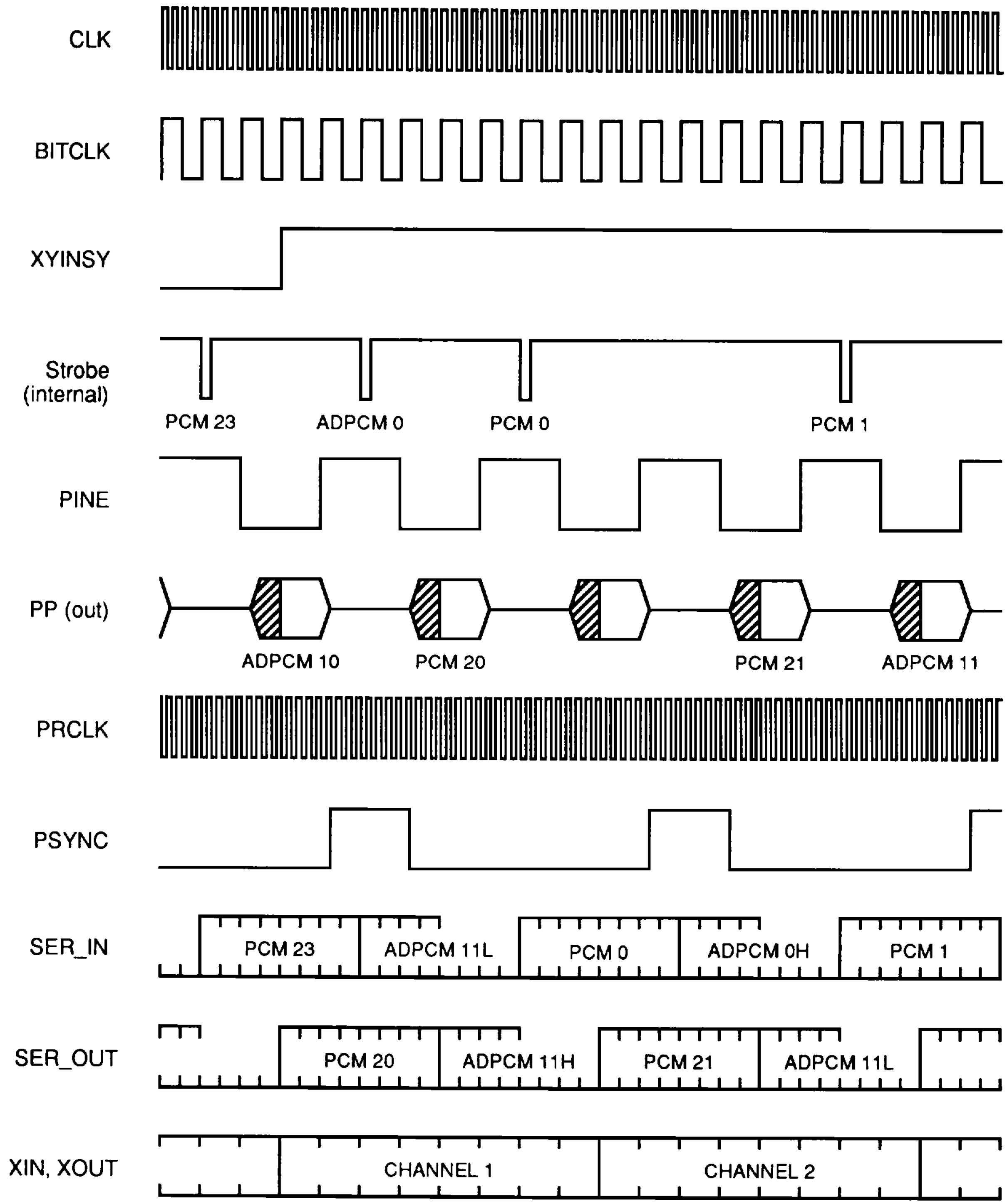

Figure 18. Timing Diagram for 24-Channel Ungapped Mode

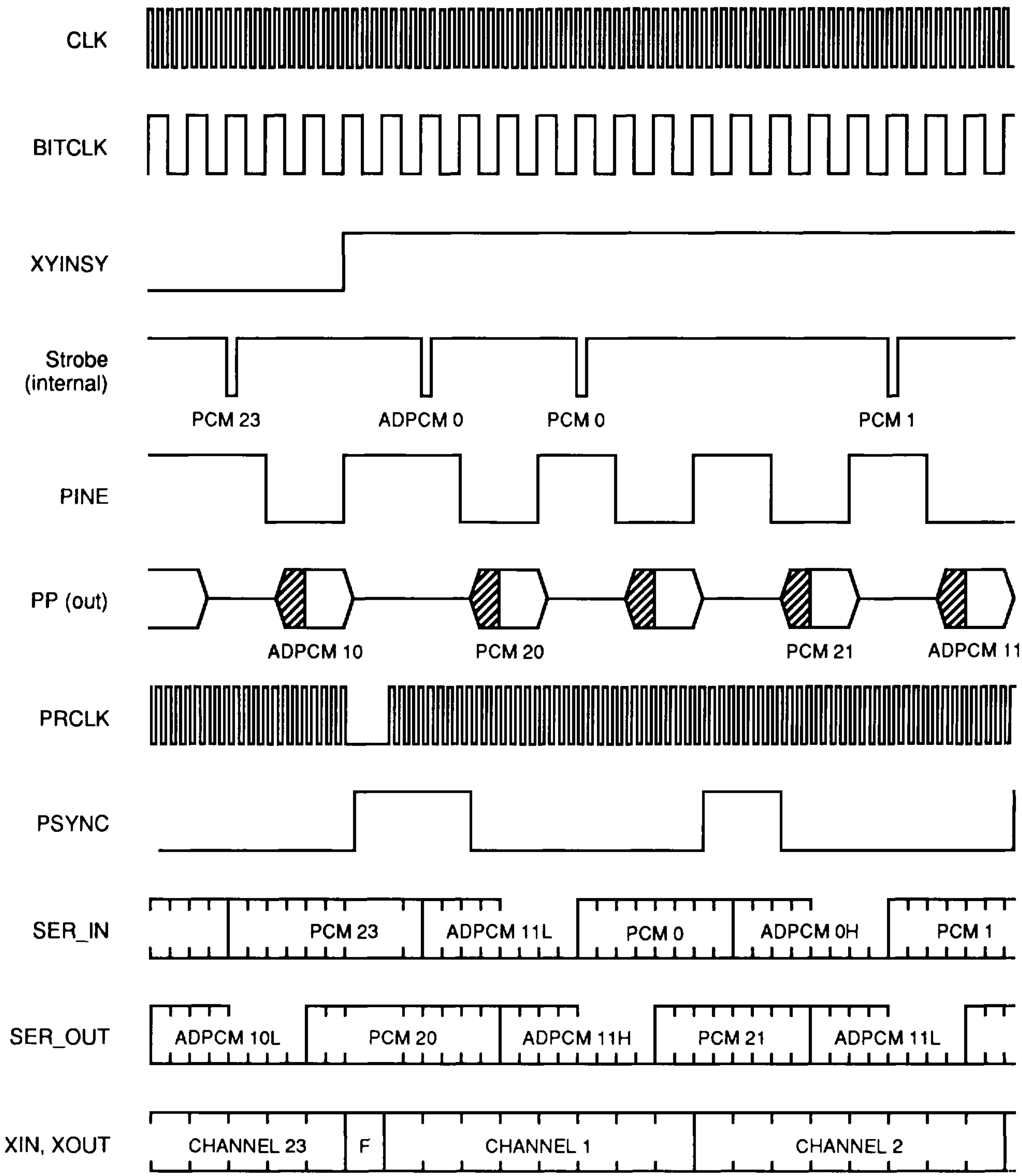

Figure 19. Timing Diagram for 24-Channel Gapped Mode

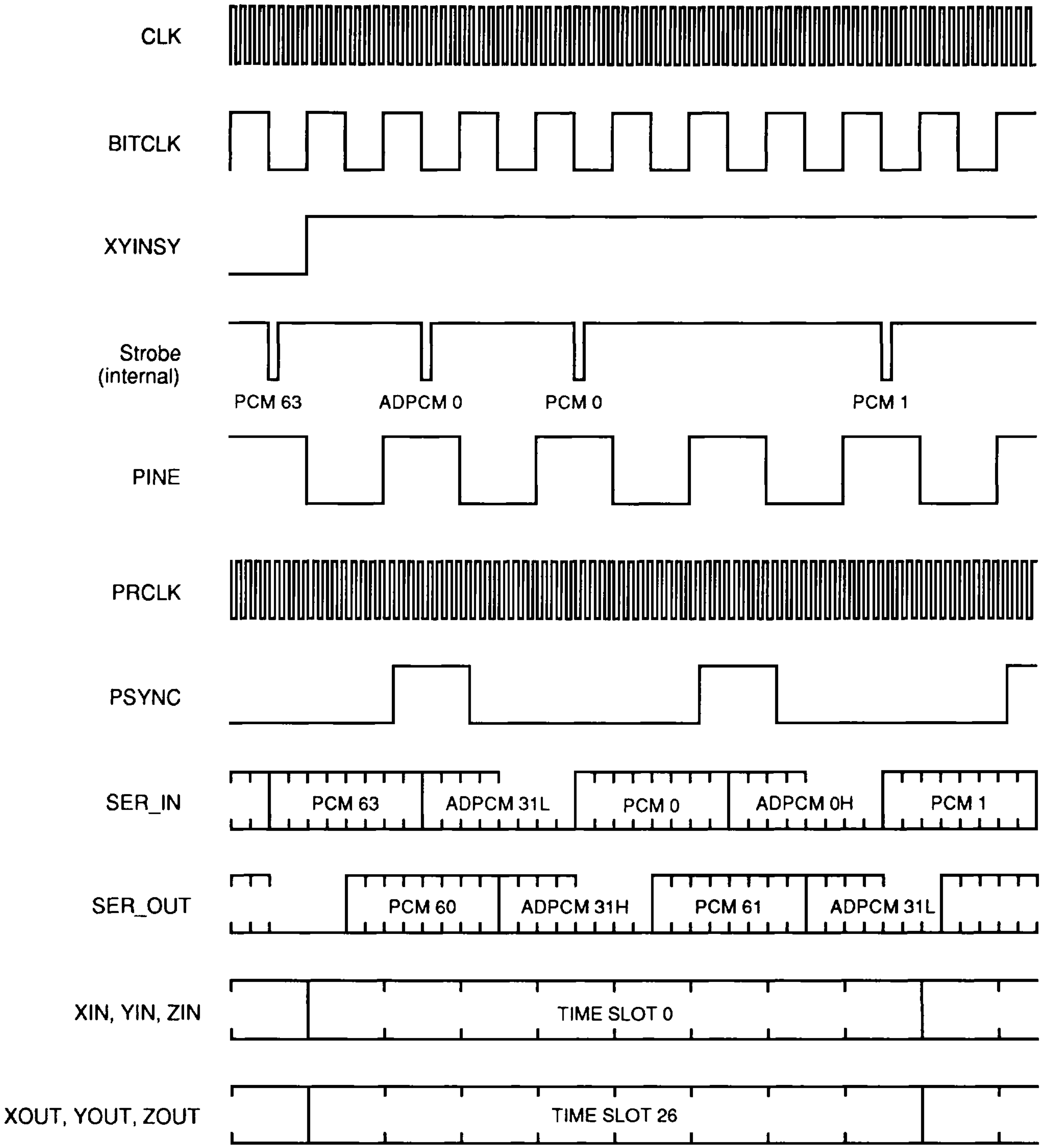

Figure 20. Timing Diagram for 60/64-Channel Mode, Serial PCM Input (G.761)

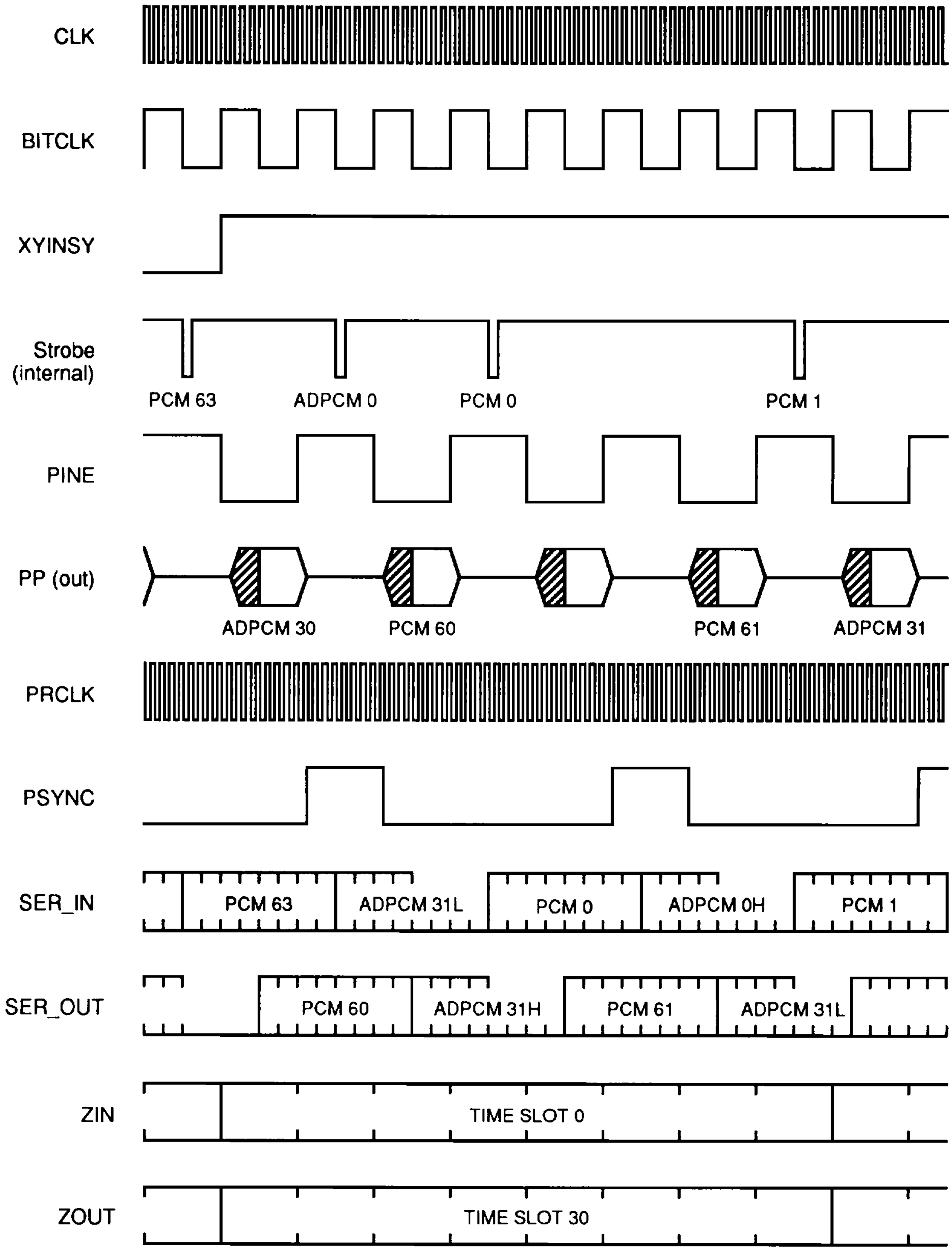

Figure 21. Timing Diagram for 60/64-Channel Mode, Parallel PCM Input

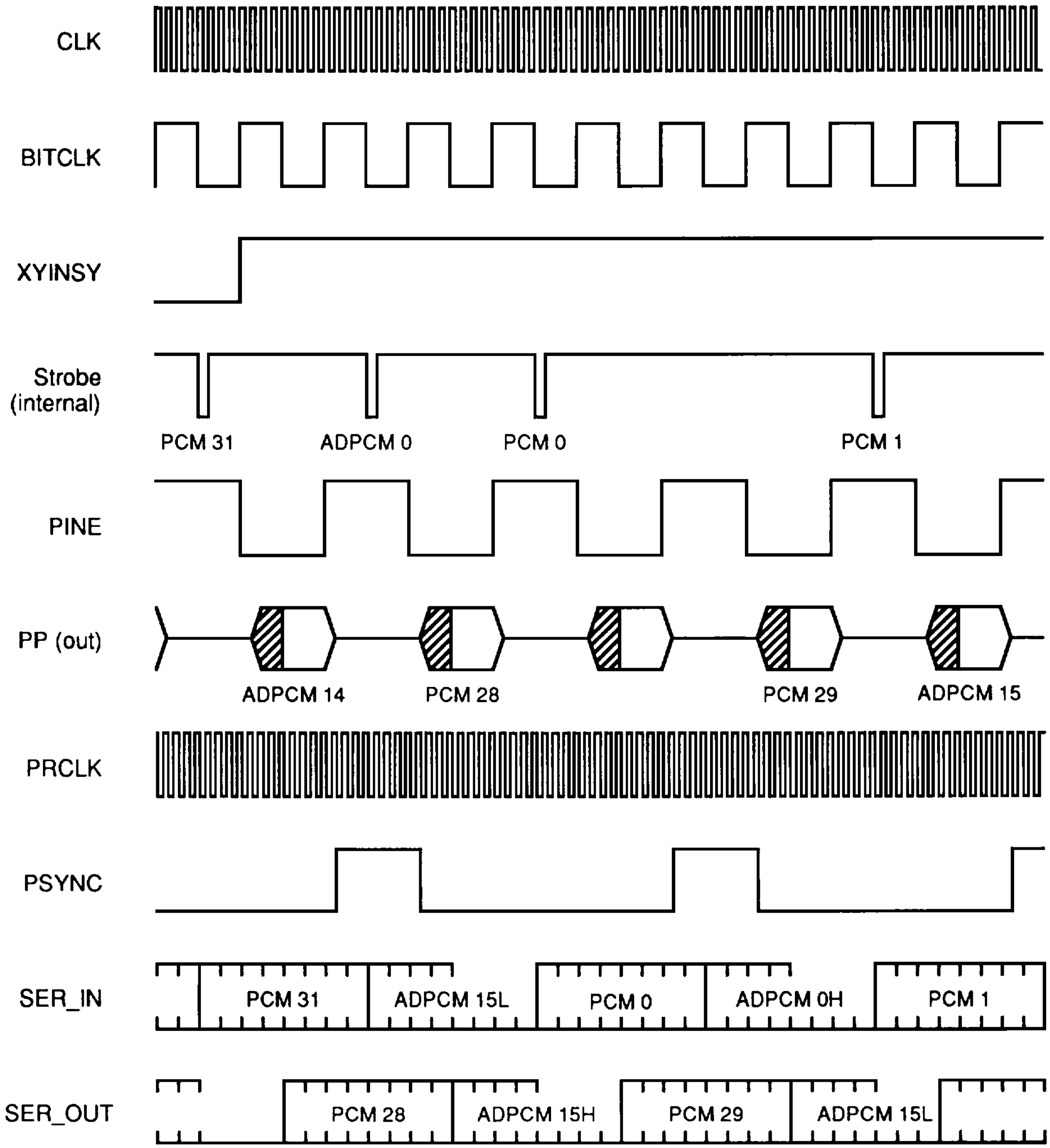

Figure 22. Timing Diagram for 32-Channel Mode

3.2.1 Serial Interface for 24 or 48 Channels

When the serial mode is enabled, the X and Y port data streams are input on the XIN and YIN pins, respectively. As shown in the timing diagram in Figure 16, the PCM channels (starting at channel 0 on the X port and channel 24 on the Y port) are supplied to the input pin one bit at a time on each rising edge of the PCM bit clock output. The first bit of channel 0 on the X port (or channel 24 on the Y port) is supplied after the rising edge of the PCM superframe sync input. A frame is complete on the X and Y ports after 192 bits have been supplied (24 channels X 8 bits/channel). The PCM channel slots should be provided most-significant bit first. No frame bit should be in the serial stream in ungapped mode.

If gapped mode is selected (valid only for the 24 and 48 channel rates), a frame bit position is present in the X, Y, and Z input streams (for 24-channel operation, only the X input stream is used and the parallel ADPCM interface is used). This frame bit position need not contain a valid framing pattern. The frame bit position begins immediately after the rising edge of the PCM superframe sync input, followed by the PCM channel data provided most-significant bit first. Thus, in gapped mode, a frame consists of 193 bits.

The X and Y port data streams are "buffered" when serial input mode is selected. This means that the PCM channels are written to a frame buffer to permit implementation of the timeslot rearrangement required by the various templates in T1Y1/90-076. As the inputs are written into one frame buffer, the contents of the previous frame buffer are read and sent to the ADPCM processor to form the Z transmit stream. This creates a one frame delay on the encode side of the formatter.

Likewise, on the decode side, the PCM channels coming back from the ADPCM decoder are written into a frame buffer before being output on the XOUT and YOUT pins. This permits the inverse timeslot rearrangement on the decode side and also results in a one frame delay. XOUT and YOUT are available on PP11 and PP9, respectively.

The buffer locations for the PCM input and the PCM output are given in Table 5. Signaling buffer addresses are given as well. The PCM buffers are two-frame buffers; thus two locations are required for each PCM channel. In the case of unused channels at the decoder, the desired idle code should be written into both locations. For the decoder signaling buffer, a separate idle signaling buffer is provided as indicated.

As shown in Figures 16 and 17, the XOUT and YOUT serial data streams are of the same format as the XIN and YIN data streams. The first bit of the superframe is synchronized to the rising edge of the superframe sync input and the data bits are supplied on the rising edge of the PCM bit clock. A frame bit position is contained in the data stream only in gapped clock mode and does not contain a valid framing pattern.

3.2.2 Serial Interface for 60/64-Channel Operation

The operation of 60/64-channel mode with serial PCM is shown in Figure 20. This mode is for implementing the G.761 line format.

The CLK input in this mode is 16.384 MHz and the BITCLK output is 2.048 MHz. The superframe synchronization pulse input must be present at any frame multiple; it can be synchronized every frame if desired as the frame counter is not used in this application.

The ADPCM and PCM output streams are delayed six channel periods (approximately 24 µs) from the PCM and ADPCM input streams. ZOUTSY is a superframe synchronization signal that is synchronized to the PCM and ADPCM outputs (XYINSY delayed by six channel intervals).

3.2.3 Parallel PCM Interface

The parallel interface timing is shown in Figures 16 and 17 for the ungapped and gapped modes at 48 channels respectively. Figures 21 and 22 show the parallel interface timing for 64 channels and 32 channels; the important features of these diagrams are the same as for 48-channel Ungapped Mode. The lower 8 bits of the 12 bit Parallel bus (PP) are the inputs and outputs for the PCM bytes. The most-significant bit of the PCM channels is input on PP7 and the LSB on PP0. The PP bus is a bidirectional bus that serves to collect both the PCM and ADPCM inputs as well as providing the PCM and ADPCM outputs. The Parallel Input Enable

(PINE) signal is an output that is used in conjunction with the PP bus for arbitration. PINE is active high, meaning that the PP bus is an input when PINE is high and the PP bus is an output when PINE is low.

As shown on both Figures 16 and 17, the PCM channels are supplied in order from channel 0 to channel 47 during every fourth clock cycle of the PCM bit clock starting on the fourth cycle after the rising edge of the PCM superframe sync input. PINE will be high during this interval and may be used to enable the user's external bus drivers. An internal strobe will sample the PP bus in the middle of the clock cycle as shown in the figures. Notice that in gapped clock mode, there is an extra clock cycle after PCM channel 47 is input. This is the 193rd bit position necessary at the 48 channel gapped clock rate. In both modes, the PCM channels are input on every fourth clock cycle for clock cycles numbered 4 to 192.

The parallel interface is an "unbuffered" interface. This means that the PCM channels supplied at this interface are sent directly to the ADPCM processor for encoding. No timeslot rearrangement is performed on this channel stream. It is assumed that the user is supplying the channels in the desired ordering via an external switching arrangement.

On the decode side, the PCM channels coming back from the ADPCM processor are also unbuffered, and are output on the PP bus in the same order that they were supplied to the ADPCM processor. In the decode direction, the ADPCM processor has a delay of 88 processor clock (PRCLK) cycles from the first bit of ADPCM input to the first bit of PCM output. The PCM channels are output directly to the PP bus (shown as PP(out)) when PINE is low.

.c.3.3 ADPCM Port Interface

The interface for the ADPCM DS1 stream can also be either parallel or serial, independent of the PCM interface mode (24-channel gapped operation requires the use of the ADPCM parallel interface, however). A low level on the ADPCM Parallel Select input enables the serial input while a high level on the select input enables the parallel input. The timing for these modes is also shown in Figures 16-18 and Figure 20.

Except in 24-channel gapped mode, the ADPCM port data stream is always available on both the parallel (PP bus) and serial output (ZOUT).

3.3.1 Serial Interface

When the serial mode is enabled, the ADPCM port data stream is input on the ZIN pin. The ADPCM input is not buffered; therefore, the ADPCM channels are sent directly to the ADPCM processor from the ZIN pin for decoding. After a decoder processing delay of 88 clock cycles, the expanded (PCM) channels are returned from the ADPCM processor. At this point, the channels are written into the RAM buffer as discussed above in section 3.2.1. When serial mode is used, there is a one frame delay from ZIN to XOUT and YOUT. This is due to the RAM frame buffer used to implement the timeslot rearrangement required for the bundle format.

3.3.2 Parallel Interface

In parallel mode, the Z port data is input on the PP bus in the same manner as the X and Y port data, eight bits at a time. As shown in the timing diagrams, the parallel input enable is active on the second PCM bit clock after the rising edge of the superframe sync input. During this clock cycle, the internal strobe signal will clock in data for the first two ADPCM channels (2 channels x 4 bits/channel) unless the first channel is a clear channel. In this case, the eight bits latched from the parallel bus will represent one channel. On every eighth clock cycle after this first strobe, another 8 bits of Z port data will be latched in on the parallel bus.

The Z port data outputs are also shown in the timing diagrams. These data outputs also use the entire 8-bit data bus. Therefore, every eight clock cycles of the PCM bit clock, the data bus will output Z port data. This data represents either two 4-bit ADPCM channels or one 8-bit channel if that channel was transmitted as a clear channel.

.c.3.4 ADPCM Processor Interface

The interface to the ADPCM processor circuit set consists of 7 signals: a serial data input, a serial data output, 3 control lines, a data clock, and a synchronization signal. The ADPCM processor clock is the same frequency as the system input clock. If gapped mode operation is selected, then the circuit deletes 8 clock cycles during the frame bit period before sending the clock to the ADPCM processor. The serial data in and out signals are named with reference to the ADPCM processor. SER_IN is therefore a serial, multiplexed bit stream consisting of interleaved PCM and ADPCM channels going to the ADPCM processor. SER_OUT is the corresponding bit stream coming back from the ADPCM processor. The synchronization signal identifies channel locations in the serial data bit streams coming from the ADPCM Line Formatter. The processor control signal CNTRL is a multiplexed signal that contains algorithm reset and clear-channel information for each channel. Finally there are two coding table select signals allowing for the selection of 1 out of 4 different ADPCM compression/expansion functions. This feature is used to provide a 24 kbit/s coding table for use with Robbed-bit Signaling. Other optional tables can be included to provide for special applications. The SER_IN, synchronization (PSYNC) and clock signals (PRCLK) provided by the FORMATTER to the ADPCM processor are also shown in Figures 16-21. The ADPCM Line Formatter automatically gaps the clock and inserts the required "dead space" in the SER_IN stream for the ADPCM processor in gapped mode. The SER_OUT stream returning from the ADPCM processor is shown and contains the same "dead space" in gapped mode.

.c.3.5 PCM Signaling Interface

The signaling bits associated with the X and Y port streams can be provided either in-band or out-of-band in parallel or serial mode. The signaling associated with the Z port is always embedded in the data stream.

3.5.1 Serial Interface

When the serial mode is enabled, input signaling for the PCM channels on the X and Y ports is expected from one of two sources. If the Out-of-band PCM Signaling Input bit in the Mode register is clear, then the incoming signaling bits are expected in the robbed-bit signaling position of each PCM channel. The A, B, C, and D signaling bits will be extracted from the LSB position of each channel with signaling enabled in the 6th, 12th, 18th, and 24th frames of the 3 msec superframe, respectively. If the Out-of-band PCM Signaling Input bit in the Mode register is set, then the signaling bits are expected on the XSIG and YSIG pins. The A, B, C, and D bits are expected to be provided every frame.

Output signaling for the PCM channels on the X and Y ports is also available either in-band or out-of-band. If the Signaling Enable bit in the control register for the corresponding output is set, then the signaling bits are carried in the standard robbed-bit positions in the 6th, 12th, 18th, and 24th frames of the superframe. Signaling is only updated for the channels whose Signaling Idle bit in the low channel control register is not set. If the Signaling Idle bit is set for a particular channel, then that channel will have an idle signaling pattern inserted into the signaling bit positions. The idle signaling pattern desired can be loaded into the PCM Signaling Buffer for that channel by the microprocessor. The output signaling is also available on the PP10 pin for the X port and on the PP8 pin for the Y port in serial mode. If the Signaling Enable bit in the low channel control register is not set, then the signaling is available only on these pins and is not reinserted into the robbed-bit signaling positions of the PCM streams. The timing for the signaling data on these pins is the same as in-band signaling bits.

3.5.2 Parallel Interface

When the parallel mode is enabled, either in-band or out-of-band signaling is available. The signaling bits appear in the standard positions in in-band mode. In out-of-band mode, the A, B, C, and D signaling bits are expected on the upper four bits of the PP bus. The XIN, XSIG, YIN, and YSIG pins are inputs that indicate when an update of the A, B, C, and D input signaling bits, respectively, should be made. (See Table 4) Since the PP bus is bidirectional, the Parallel Input Enable (PINE) signal is used to indicate whether the bus is an input or an output. When PINE is high, signaling bits are being input. When PINE is low, PP8 through PP11 provide the signaling bits for the output X and Y PCM ports. The signaling bits are present every frame.

Insertion of signaling bits in the parallel PCM output is controlled by the Signaling Enable bit in the low channel control register. For each channel in which the control bit is set, signaling will be inserted in the robbed-bit signaling position.

.c.4.0 BUNDLE SIGNALING MODE

.c.4.1 Encoder Operation

The output Z stream from the encoder consists of 2, 4, or 5 bundles of 384 kbit/s each, depending on which operation speed is selected. Bundle signaling mode is selected for each bundle independently by programming the bit pair corresponding to that bundle in the Bundle Register to a value of 01 as described in Section 3.3.1.2. When bundle mode signaling is selected for a particular bundle, that bundle will contain a delta channel in timeslot 12 if any of the first 11 channels of the bundle contain signaling for transmission. Whether any channels have signaling for transmission is determined by the channel control template (as specified in T1Y1/90-076) that is selected.

The channel control words for the delta channels of each bundle should be set for diagnostic operation. The encoder signaling should be set idle.

As the incoming signaling bits for channels 1 through 11 of the bundle are received, they are written into RAM. When the Z port data stream is formatted for transmission, the signaling bits are inserted into the delta channel along with a bundle frame alignment pattern and bundle CRC calculation as specified in ANSI T1.302-1989. The delta channel provides bandwidth for 16 state signaling for all 11 channels in the bundle. The delta channel also contains 4 alarm bits that are set by the microprocessor. Alarm bit M1 is used to send a bundle yellow alarm to the remote end when the near end is in bundle red alarm. Bit M2 is used to indicate that the PCM port has received a DS1 red alarm or AIS. Bit M3 is used to indicate that the PCM port has received a DS1 yellow alarm. Bit M4 is a summary alarm bit that is set any time bits M1, M2, or M3 are set. The microprocessor can set these bits by writing to the following locations (in hex) in RAM with M1 as bit 7, M2 as bit 6, M3 as bit 5, and M4 as bit 4:

	Bundle 1	Bundle 2	Bundle 3	Bundle 4	Bundle 5
Address (hex)	44B	457	463	46F	47B

.c.4.2 Decoder Operation

The incoming Z port stream will also contain 2, 4, or 5 bundles depending on the rate of operation selected. For any bundle that has a delta channel present, the bundle frame alignment is recovered, the bundle CRC is checked for errors, and the signaling bits are written into RAM. The signaling bits are then reinserted into the outgoing PCM channel streams of ports X and Y. If a bundle has a delta channel present, the corresponding PCM timeslot for that channel (channel 12, 24, 36, or 48) can be conditioned with an appropriate idle code by loading the idle code value desired into the PCM output buffer. This type of conditioning can also be performed on any other unused channels present because of transparent channels present in the Z stream.

The status that needs to be monitored by the microprocessor for each bundle operating in bundle signaling mode is: bundle superframe alignment signal synchronization (OOF), bundle CRC error checking result, and bundle alarm status received on the M1, M2, M3 and M4 bits. The status register at address 0 contains the OOF and CRC check result for bundles 1-4 as shown in Figure 10. The CRC and OOF status for bundle 5 is in status register 1 in bits 0 and 1, respectively. The CRC and OOF status for all bundles is latched every 3 msec.

The M1, M2, M3, and M4 alarm bits are updated each superframe; therefore, they can be read as often as every 3 msec for direct integration by the microprocessor. The processor can then take the appropriate actions based on the given fault condition as specified in ANSI T1.302-1989. Figure 23 shows the configuration of the RAM location that contains the alarm bits. The locations of the alarm bits in RAM are as follows:

	Bundle 1	Bundle 2	Bundle 3	Bundle 4	Bundle 5
Address (hex)	4CB	4D7	4E3	4EF	4FB

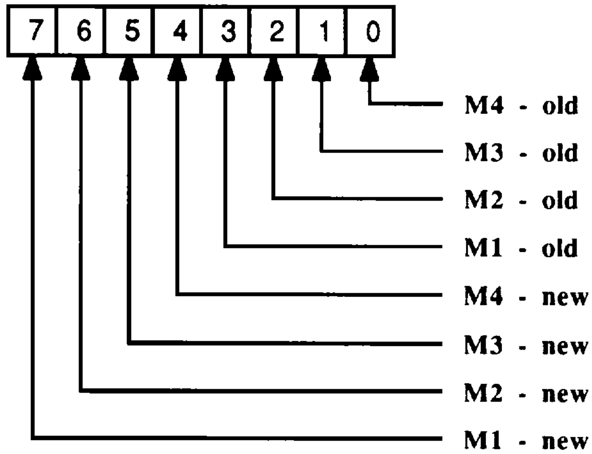

Figure 23: Alarm Bit Storage in RAM

.c.4.3 Signaling Enable Control

The channel alignment of the high control word signaling enable bit is different for bundle mode than for the other signaling modes. The signaling enable bit is associated with the PCM ordering rather than the ADPCM ordering. Therefore, the signaling enable bit located at a given address controls the signaling function for the corresponding PCM channel. This function is shown in the tables in section 2.3.

.c.5.0 TRANSITION SIGNALING MODE

Transition signaling is a signaling method that conserves message bandwidth by sending signaling information only when there is a change in the signaling states. For this reason the line format for transition signaling accommodates 48 channels with full-time 32 kbit/s coding. This gives better transmission performance than the Robbed-bit Signaling mode. The signaling information is contained in a signaling message containing the signaling bits, alarm status information, and error-correction code bits. Each signaling message is recognized by a pattern of all-zero four-bit nibbles. All-zero nibbles are not generated by the ANSI T1.303-1989 32 kbit/s code.

.c.5.1 Transition Signaling Format

In order to clearly present the operation of the ADPCM Line Formatter, this section will generally follow the organization of section 4.1.3 of ANSI standard T1.302-1989, "Transcoders Using Transition Signaling." This is the section that presents the Transition Signaling format.

5.1.1 Transition Signaling Messages

Each transition signaling message is composed of 8 nibbles in the format

0 0 S T 0 0 P Q,

where the S and T nibbles contain signaling and alarm bits and the P and Q bits contain parity bits to allow error-correction at the receiver. "0" represents a nibble consisting of four zero bits.

There is also an acknowledgement sequence of

0 0 F F

that is sent to acknowledge receipt of a message, where "F" represents a nibble containing four bits set to "1."

5.1.2 Encoding of Signaling and Alarm Information

Signaling and alarm information is encoded in the S and T nibbles as follows:

S nibble	A	B	M1	~M1
T nibbles	C	D	~M2	~M3,

where "~" indicates logic inversion. M1, M2, and M3 are alarm bits defined in section 3 of T1.302.

The P and Q nibbles are formed by an encoding process described in section 4.1.3.1.2 of T1.302.

Messages are generated by the Encoder section of the ADPCM Line Formatter by using a transition signaling buffer location in the control space. This address can be generated by setting the upper three characters of the buffer address to the channel number (in hexadecimal) and the lower character to A (hex). This buffer is called the stable-word buffer and the address can be noted for this section as 0ccA. The format for the stable word is

T M1 M2 M3 As Bs Cs Ds,

where T is a control bit that initiates the transmission of a signaling message upon request from the controller and As, Bs, Cs, and Ds are the stable signaling states.

Messages on odd and even channels are always offset by two frames.

5.1.3 Message Rules

Consecutive messages generated by the encoder are separated by four frames. Messages with alarm content or messages transmitted by the controller will be sent at the next "message poll" by the encoder circuit. Acknowledgement messages are not sent unless all signaling messages have been transmitted.

5.1.4 Detection of Signaling Messages

Messages are detected whenever three of the four all-zero nibbles that are transmitted as a part of a signaling message are recognized at the receiver. A table illustrating this is given in section 4.1.3.1.4 of T1.302. Acknowledgement messages are detected when a "00FF" is received.

5.1.5 Decoding of Signaling Messages

A signaling message is decoding by applying the error-correction algorithm described in section of 4.1.3.1.5 of T1.302. The correction table given in Table 9 of this section must be loaded into the RAM in locations 700 to 7FF; only the first two nibbles of each entry in the table are required to correct the S and T nibbles. This table is available in the program ROM for the T-1 Transcoder Evaluation board described in application note AN-201.

5.1.6 Signaling Procedures

This section describes the implementation of the signaling procedures as described in section 4.1.3.1.6 of T1.302.

The Signaling Enable channel control bit must be set for the encoder channel in transition signaling mode. In addition, transition signaling must be set for the corresponding bundle. If the Signaling Enable control is not set for the encoder channel, transition signaling messages will not be sent. The decoder Signaling Enable control bit controls insertion of signaling bits in the robbed-bit signaling positions of the PCM output but does not otherwise affect transition signaling.

5.1.6.1 Signaling Message Generation

The Encoder Signaling Buffer for each channel (this buffer is in consecutive locations from 440 to 47F) contains both the current state and the previous state of the Encoder signaling in the format

Ac Bc Cc Dc Ap Bp Cp Dp.

These locations will be updated by the PCM Input circuitry unless the Idle Signaling bit of the high channel control word is set. If this bit is set the Encoder Signaling Buffer must be loaded by the controller. This feature allows the communication of alarm information in channels in which signaling is set idle or not used.

Whenever there is a difference between the signaling state and both the current signaling state and the previous signaling state, a signaling message will be sent. A signaling message always uses the signaling bits corresponding to the current signaling state. These bits are transferred to the stable signaling state when the message is sent.

The Idle Signaling bit of the low channel control word enables the insertion of idle signaling bits from the Decoder Idle Signaling buffer to the PCM outputs but does not otherwise affect transition signaling operation.

To send a message indicating a change in the alarm bits, the stable word location at location 0ccA, where "cc" is the channel number, is loaded with the new alarm bits and with the "T" bit set high. This action will cause a signaling message to be sent, consisting of the new alarm bits and the current signaling bits from the Encoder Signaling Buffer. If any of the alarm bits are set high, three consecutive signaling messages will be sent.

If the alarm bits are being changed from not all-zero to all-zero, the above procedure should be repeated three times at 3-ms intervals. This will generate the three signaling messages required. An alternative is to monitor the Stable Word location until the "T" bit is set low by hardware, and then reloading the all-zero alarm content and setting the "T" bit high.

5.1.6.2 Signaling Message Reception

Each time a signaling message is received at the decoder, the corresponding Decoder Signaling Buffer location (consecutive locations from 4C0 to 4FF) is loaded with the received message in the format

R M1 M2 M3 A B C D,

where the R bit is set to 1. The signaling bits are used to generate the PCM Output signaling at the decoder output. No message with alarm bits set is regarded as valid and thus written to the signaling buffer unless the message was received with no apparent errors (error syndrome value of zero). For this reason, no message with the M1 and ~M1 bits in agreement is accepted as a valid message.

The Decoder Output Signaling buffer must be monitored by the controller to determine if there has been a change in the alarm state for the channel and to take consequent actions. This can be done directly by checking to see if the R bit is set and clearing it if it is. If the R bit is not set, no new message has been received.

5.1.6.3 Signaling Message Acknowledgement

Each time a valid message is received and accepted by a decoder channel, an acknowledgement message must be sent by the corresponding encoder channel. This procedure is automatically performed by the ADPCM Line Formatter circuitry.

5.1.6.4 Unacknowledged-Message Counter

Each channel of the circuit has an unacknowledged-message counter located at buffer address 0ccB (hex). The unacknowledged-message counter consists of the low seven bits of this buffer word. The most-significant bit of the buffer word is set to zero every time the unacknowledged-message counter reaches zero or a message is sent from the encoder. The format for the word is

$Q\ U_6\ U_5\ U_4\ U_3\ U_2\ U_1\ U_0$,

where "Q" is the status bit and U_6-U_0 are the counter bits. The unacknowledged-message counter is incremented when a message is sent and decremented when an acknowledgement message is received. If this counter is nonzero for longer than 2 seconds after the last message has been sent, the signaling and alarm states should be retransmitted.

To determine if an unacknowledged message has been outstanding for more than 2 seconds plus or minus 50 ms, the unacknowledged-message counter should be polled at intervals of less than 100 ms and the most-significant bit set to 1. If the most-significant bit is read as 1 on consecutive polls for two seconds, then an unacknowledged message has been out for that long. The unacknowledged-message counter should then be written to all-zeros and the current alarm state written to the transmit message buffer with the "T" bit set high. This will retransmit the signaling message on the channel.

If the unacknowledged-message counter for one channel pair is polled every 3 ms, the objective of retransmitting after two seconds without an acknowledgement will be met.

5.1.6.5 Unexpected Acknowledgement Message

If an unexpected acknowledgement is received (unacknowledged-message counter set at zero when acknowledgement message received), the unacknowledged-message counter will remain at zero and a signaling message will be transmitted automatically.

5.1.6.6 Inactive Transition Signaling Channel

If a transition signaling channel has been inactive for six hours, the signaling state is to be retransmitted. This is accomplished by monitoring the state of the message-queue counter that is located at buffer RAM address 0cc9.

This buffer address is used by the transition signaling circuitry to keep track of message transmission. Each time a signaling message is transmitted, the most-significant bit of the message-queue counter is set to 1.

Every few minutes, each message-queue counter should be read and the most-significant bit set to 0. If this bit is read consecutively as 0 for six hours, a message should be generated by setting the "T" bit in the message-generation buffer.

5.1.7 Out-of-Frame and High-Error Conditions

Out-of-Frame is indicated to the ADPCM Line Formatter by setting the FREEZ input high. This immediately forces the acknowledgement register zero and inhibits any received signaling messages.

The rate of all-zero nibbles received is monitored by a zero-nibble counter located at buffer RAM address 0cc8. The buffer register consists of a seven-bit zero-nibble counter and a FREEZ indication bit. If the FREEZ input is high, the low seven bits, the counter, are set to zero and the FREEZ bit is high.

The counter is scaled by a factor of 256 from the values given for the zero-nibble counter in section 4.1.3.1.7 of T1.302.

If the zero-nibble counter is 16 or greater, the signaling message is ignored. The Decoder Signaling Buffer is not updated, and an acknowledgment message is not sent.

The counter should be monitored (read) by the controller to determine the alarm state for the channel. The M1 alarm bit should be set if the counter is 96 or above and cleared if the counter is below 64.

5.1.8 Line Formats

All templates are available as in Bundle Format when no delta channel is present. If signaling is active of a 64 kbit/s transparent channel, PCM Robbed-bit Signaling is used. In this case, a ADPCM Receive signaling input must be applied as in Robbed-bit Signaling format. This is described in section 5.2 below.

Transition Signaling is available for 32 kbit/s transparent channels. However, care must be taken with zero nibbles contained in these channels.

5.1.9 Idle Code for DCS

If the transition signaling circuit is connected to a DCS that has an idle code that is used when the incoming DS1 is in Carrier Group Alarm, the alarms for each odd/even channel pair (e.g. X1 and X2) should be based on the alarm state of the even channel only. In this case, the idle code "11110000" will be sent on the line and the even channel will go into the alarm state.

.c.5.2 Transmission Considerations

Signaling messages overwrite the encoded ADPCM at the encoder and are used as input to the ADPCM decoder when received. Transmission effects of this are discussed in section 4.1.3.2 of T1.302.

.c.5.3 Zero Suppression

Some transmission equipment may overwrite all-zero nibbles in odd channels to suppress strings of zeros. Normally such distortion will be overcome in signaling and acknowledgement messages with the error protection and retransmission features of the Transition Signaling format. This issue is discussed in section 4.1.3.3 of T1.302.

.c.5.4 Channel-Pair Bundle Alarm

A red bundle alarm is declared when the zero-nibble counter equals or exceeds 96 on either channel of an odd/even channel pair. The alarm is released when both channels have zero-nibble counts less than 64. This strategy accommodates the use of the DCS idle code "11110000" for alarm conditions.

.c.5.5 Controller Function Summary

This section summarizes the functions of the controller for transition signaling channels with signaling active.

5.5.1 Polling Considerations

To meet the requirements of transition signaling given in T1.302, it is sufficient to scan one channel pair every 3 ms. This results in an update period of 72 ms in a 48-channel system or 90/96-ms in a 60/64-channel system.

The controller should have a table for each channel of the current encoder (near-end) alarm state and decoder (far-end) alarm state. In addition, 8-bit timers are required for unacknowledged-message time and transmit inactivity time.

5.5.2 Polling Activity

For each channel, perform the following functions:

1. Read the Decoder Signaling register (address 4C0 plus channel count). If the "R" bit is set, clear the bit and check to see if the decoder alarm state has changed. If it has, update the current state in storage and take appropriate action.

2. Read the unacknowledged-message counter (address 0ccB). If the "Q" bit is 0, set it to 1. If the "Q" bit has been read as 1 for two seconds, set the register value to 0 and generate a message by writing the current encoder alarm state with the T bit set to one to the stable-word buffer (address 0ccA). The two-second interval can be determined by incrementing an eight-bit timer. If a 72-ms scan is implemented, a count of 28 should be used to initiate a signaling message.

3. Read the zero-nibble counter for both channels of the even/odd channel pair (address 0cc8) and update the local alarm state. If the state has changed, send alarm messages on both channels.

4. Once every ten minutes, check the MSB of the message-queue register (address 0cc9). If the most-significant bit of this counter is 1, set it to 0. If it has been set to 0 for six hours, initiate a signaling message.

Since these operations need only be performed on one channel pair every 3 ms, the real-time requirements on the controller are quite modest.

.c.6.0 ROBBED-BIT SIGNALING MODE

In Robbed-bit Signaling mode, signaling information overwrites one bit of the ADPCM code once every sixth frame. The format that results is given in section 5 of ANSI Standard T1.302-1989. This signaling method is analogous to that used for PCM, but causes more distortion than PCM since the ADPCM word is already a compressed speech signal. For that reason, this signaling method may be less satisfactory in many applications than the other available signaling formats.

In order for the ADPCM coding operations to work properly, both the encoder and the decoder need to be operated at 24 kbit/s instead of 32 kbit/s during signaling frames. This function is also provided by the ADPCM Line Formatter. The CODE12 output is set high to indicate 24 kbit/s coding to the ADPCM Processor.

.c.6.1 Encoder Operation

In Robbed-bit Signaling mode, the output ADPCM consists of 12 4-bit channel slots in each bundle. In every sixth frame, the ADPCM Processor is set for 24 kbit/s encoding, resulting in a three-bit output. A signaling bit is added to these three bits to form the four-bit transmitted word. The format for the output is given in section 5.1 of ANSI Standard T1.302-1989.

Robbed-bit Signaling mode can be selected independently for each bundle by programming the bit pair for that bundle in the Bundle Register to a value of 11 as described in Section 3.3.1.2. Signaling, transparent operation, and templates are all independently controllable for each channel.

Robbed-bit Signaling is not supported in 32-channel and 60/64-channel operation.

6.1.1 Encoder Templates

Templates are preserved for the serial PCM interface in 24 and 48 channel modes. The templates control the selection of both the signaling and the PCM buffers to realize the same template formats available in bundle mode.

For parallel PCM, the template addresses should all be set to the "template 0" values to properly align the PCM and the signaling control words.

6.1.2 Encoder Signaling Options

Each encoded channel can be selected to have signaling enabled, and to have signaling idle if it is enabled.

If the signaling is not enabled, all frames including signaling frames, are set for 32 kbit/s ADPCM encoding and robbed-bit signaling bits are not inserted. PCM Input signaling is updated in the Encoder Signaling Buffer (and can be read by the microcontroller) but it is not inserted in the ADPCM output stream.

If signaling is enabled and is idle, the Encoder Signaling Buffer contents are used to provide signaling bits to the ADPCM output in robbed-bit signaling positions. The Encoder Signaling Buffer for the appropriate channel should be loaded with the desired idle signaling code and the appropriate control word set for idle signaling.

6.1.3 Encoder Transparent Channels

Transparent channels can be sent at either 32 kbit/s or 64 kbit/s with signaling enabled or idle. If signaling is enabled on 32 kbit/s transparent channels, signaling bits will be inserted every sixth frame.

Only odd channels can be set to 64 kbit/s transparent operation. If Robbed-bit Signaling is present on the PCM Input, then the signaling bits will be in the proper frames on the output as well. Thus signaling does not have to be inserted in robbed-bit PCM channels explicitly.

If signaling is enabled on transparent channels, signaling bits will be overwritten on the least-significant bits of the transparent word on signaling frames.

Setting the signaling enabled and idle on 64 kbit/s or 32 kbit/s transparent channels will cause insertion of the idle signaling code on the output signaling frames.

.c.6.2 Decoder Operation

Superframe synchronization for the ADPCM input is used to determine the location of robbed-bit signaling frames for the decoder. This signal should be connected to ZINSY and should be low for the last eight bits of each superframe. An internal counter then determines the locations of signaling bits in the ADPCM signal.

6.2.1 Decoder Templates

Templates are preserved for the decoder with the serial PCM interface at 24 and 48 channels as well as the encoder. The templates control PCM signal selection just as they do for Bundle Format.

6.2.2 Decoder Signaling Options

In the decoder, the least significant bit of each channel is used to update the Decoder Signaling Buffer in signaling frames.

If signaling is enabled for the decoder, the appropriate signaling bits are used to insert Robbed-bit Signaling in the serial PCM outputs if the serial PCM output is selected and in the parallel PCM output if the parallel PCM interface is selected.

Idle signaling can be selected for any output PCM channel by setting the Idle Signaling bit in the appropriate control word and loading the desired idle signaling code in the Decoder Idle Signaling Buffer.

6.2.3 Decoder Signaling Freeze

If the Signaling Freeze input is high, the "old" signaling bits in the Decoder Signaling Buffer are loaded in the "new" signaling bit positions. This operation will be done on all frames (not just signaling frames) and so will freeze all signaling bits within 125 μs.

6.2.4 Decoder Transparent Options

Either 32 kbit/s or 64 kbit/s transparent operation is possible for channels in the decoder. Only odd channels can be selected to be 64 kbit/s transparent. Signaling operation can be controlled for transparent channels just as for coded channels.

.c.7.0 DIAGNOSTIC TESTING

The ADPCM Line Formatter contains circuitry for automatic testing of both the ADPCM Processor and major portions of the formatter itself. This testing is done with encoder and decoder test sequences loaded into the 800 to 1FFF address region of the RAM by the microprocessor during initialization. Addresses 800 to FFF contain the PCM input test sequence for the encoder. Addresses 1000 to 17FF contain the output test sequence for the encoder and the input test sequence for the decoder. Addresses 1800 to 1FFF contain the output test sequence for the decoder. Testing is automatically conducted on all unused channels on both the encoder and decoder without affecting normal operation of the other channels. These unused channels can arise from the presence of either 64 kbit/s transparent channels, delta channels in bundle signaling mode, or idle PCM or ADPCM channels.

The diagnostic tests are run continuously as long as there are idle channels available. After each run of the entire test vector (vector length is 2048 samples), the test results are available on the DIAG pin and in Status Register 1. A failure on any channel at any point during the test of either the encoder or the decoder will be latched and held on this pin until the completion of the next test interval. A high level output on this pin indicates an ADPCM Processor failure.

The DIAG signal can be used to interrupt the microcontroller if desired.

An appropriate diagnostic table for this function is contained in the program ROM provided with the T-1 Transcoder Evaluation Board described in application note AN-201.

.c.8.0 RAM INTERFACE

The circuit is connected to an 8Kx8 static RAM (Cypress CY7C185 or equivalent), which is used for control and buffer operations, including the PCM input and output buffers. Timing diagrams for read and write operations are given in Figures 24 and 25 respectively.

The thirteen address, eight data, output-enable, and write-enable pins of the RAM are connected to the circuit. All enable outputs are active-low.

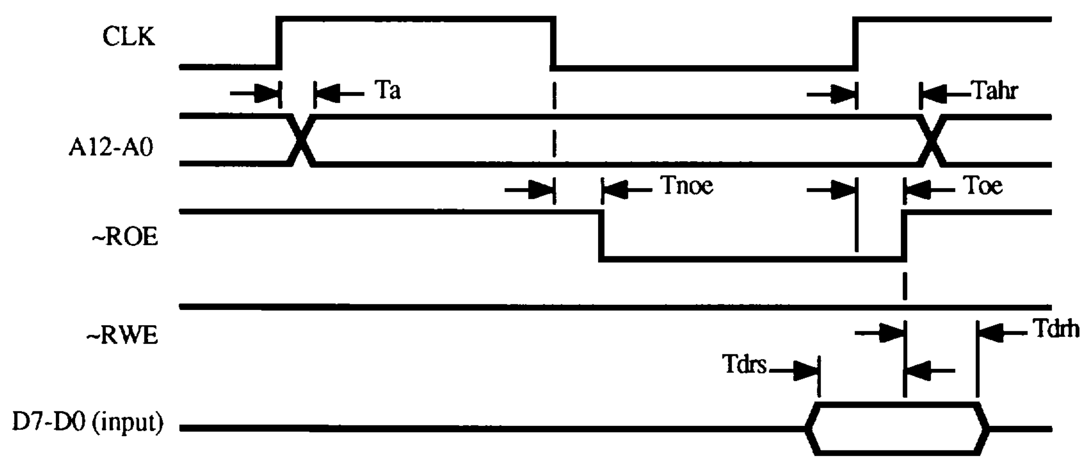

Figure 24. RAM Read Timing

The following are the guaranteed maximum delays and minimum hold times for the memory interface circuit:

CLK to Address Valid	Ta	15 ns max
Address hold from ~ROE	Tahr	0 ns min
CLK low to ~ROE low	Tnoe	10 ns max
CLK high to ~ROE high	Toe	10 ns max
Read data setup to ~ROE high	Tdrs	10 ns max
Read data hold from ~ROE high	Tdrh	0 ns max
Address hold from ~RWE high	Tahw	4 ns min
CLK low to ~RWE low	Tnwre	10 ns max
CLK high to ~RWE high	Twre	10 ns max
Write data valid from ~RWE low	Tdw	10 ns max
Data Hold from Write End	Tdwh	3 ns min

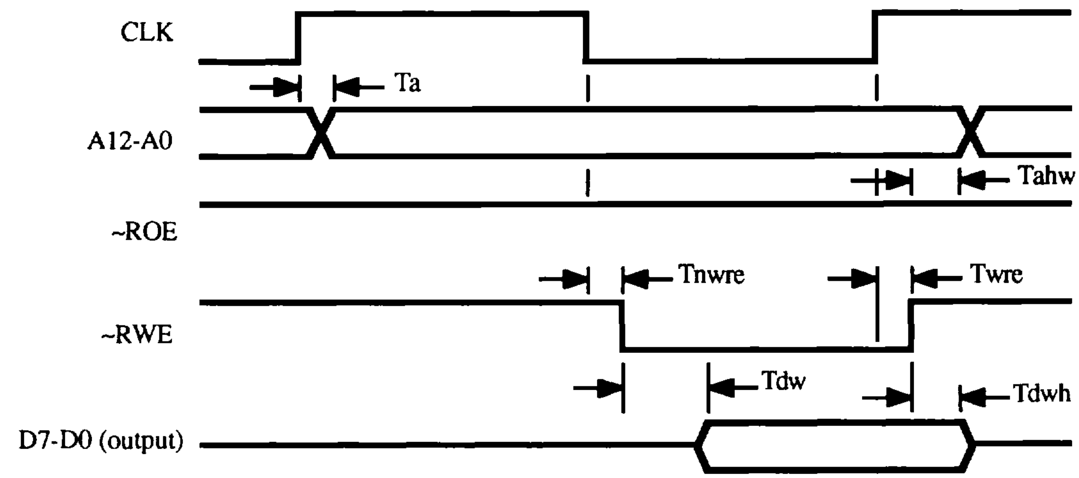

Figure 25. RAM Write Timing

Note that the data bus is always in the high-impedance state when the input clock is high. The pin capacitance will generally cause the data bus signals to have a hold time much greater than indicated above.

The following memory specifications are recommended for the various channel capacities with a clock duty cycle between 45% and 55%:

		Channel Capacity			
		60/64	48	24	
Clock Frequency	fsys	16.384	12.352	6.176	MHz
Address Access Time	t_{AA}	35	55	120	ns
Output Enable to Output Valid	t_{OE}	15	25	50	ns
Data Hold from Write End	t_{HD}	0	0	0	ns
Address Hold from Write End	t_{HA}	0	0	0	ns
Write Pulse Width	t_{PWE}	20	25	50	ns
Data Set-up to Write End	t_{SD}	15	25	50	ns

.c.9.0 MECHANICAL AND ELECTRICAL CHARACTERISTICS

.c.9.1 Package Type

The ADPCM Line Formatter is packaged in an 84-pin plastic leaded chip carrier (PLCC).

.c.9.2 Pinout Description

The pinout diagram for the ADPCM Line Formatter is shown in Figure 26.

The functions of the pins are:

SUPPLY VOLTAGE V_{cc}
Four pins are provided for power.

GROUND Gnd
Six pins are provided for ground.

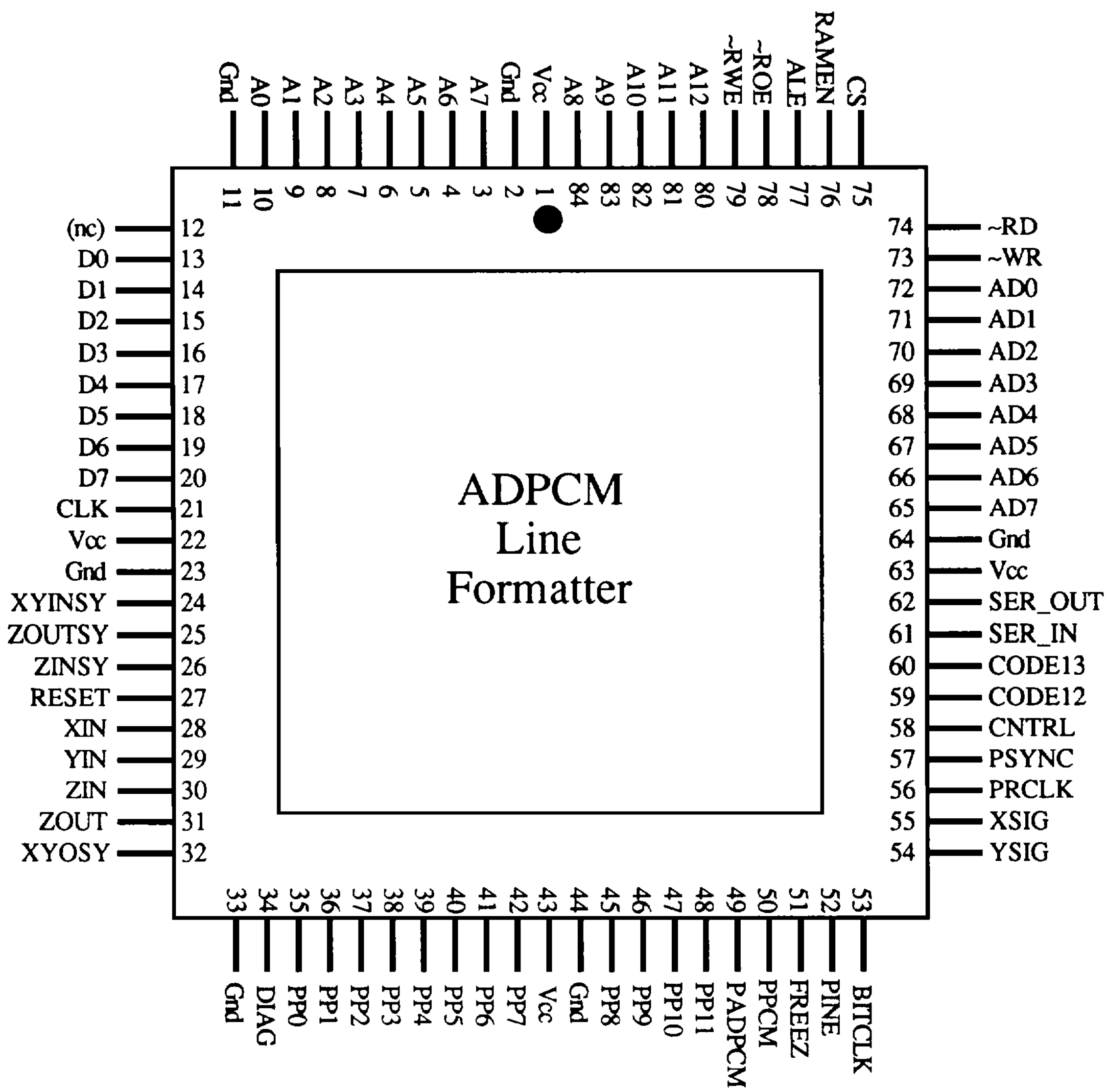

Figure 26. ADPCM Line Formatter Pinout Diagram

RAM INTERFACE ~ROE, ~RWE, A12-A0, D7-D0

Twenty-three pins are for the output enable, write enable, address, and data lines for the 8Kx8 static RAM which is connected to the integrated circuit.

CONTROLLER INTERFACE ALE, ~RD, ~WR, CS, RAMEN, AD7-AD0

Thirteen pins are connected to the 8051-series or equivalent microprocessor which is used to configure and control the ADPCM Line Formatter. ALE is the address-latch enable signal; ~RD and ~WR are the active low read and write enable control leads from the microprocessor; CS and RAMEN are two address leads from the microprocessor that enable microprocessor read and write operations and allow the RAM to be addressed, respectively. AD7-AD0 is the multiplexed address/data bus from the microprocessor.

SYSTEM CLOCK CLK

This is the system clock provided to the formatter. Its frequency depends on the number of channels processed by the ADPCM Line Formatter and whether gapped or ungapped clocking is selected.

BIT CLOCK — BITCLK

This clock signal output is the serial bit clock for the serial inputs and outputs. It is not used in parallel mode. It is exactly one eighth of the system clock frequency.

PARALLEL INPUT/OUTPUT — PP11-PP0

This is the parallel input/output bus. The PCM and ADPCM parallel words appear in PP7-PP0. PP11-PP8 contain signaling bits and serial PCM output signals in PCM Serial mode as described in Section 4.0.

PARALLEL INPUT ENABLE — PINE

This is a control signal which is synchronized to the bidirectional control bus and is used to enable input signal drivers to the bidirectional parallel input/output bus.

PCM PARALLEL SELECT — PPCM

This pin enables parallel inputs for the X and Y input and output. The parallel interface is "unbuffered" in the formatter to minimize delay.

PCM SERIAL INPUT/PARALLEL SIGNALING UPDATE — XIN,XSIG, YIN,YSIG

These are the serial input pins for the X and Y ports. XIN and YIN contain the PCM information and XSIG and YSIG contain the signaling information, which are used when out-of-band signaling is selected. In parallel PCM mode, XIN, YIN, XSIG, and YSIG are used respectively to indicate when an update of the A, B, C, or D input signaling bits should be made.

X, Y INPUT SYNC — XYINSY

This a superframe synchronization signal for the X and Y signals. In serial PCM mode, this input requires a low to high transition with the first bit of the first channel of the superframe. In parallel PCM mode, it also determines the master frame count.

ADPCM PARALLEL SELECT — PADPCM

This pin enables parallel inputs and outputs for the ADPCM or Z port. The parallel signals are provided as 8-bit bytes.

ADPCM SERIAL INPUT — ZIN

This is the serial input pin for the Z port. It is not used when parallel ADPCM is selected.

ADPCM SERIAL OUTPUT — ZOUT

This is the serial output pin for the Z port. The serial ADPCM is always present on this pin.

ADPCM OUTPUT SYNC — ZOUTSY

This is a superframe synchronization output for the Z-port output. It is low during the last eight bits of each superframe (every 3 ms) of the ADPCM serial output.

ADPCM INPUT SYNC — ZINSY

This is a superframe synchronization input for the Z-port input. This input must be low during the last eight bits of each superframe (every 3 ms) of the ADPCM serial input. This signal is used to determine the location of ADPCM signaling bits in Robbed-bit Signaling Mode. When Robbed-bit signaling is not used, the input must be connected to ground.

PCM OUTPUT SYNC — XYOSY

This is a superframe synchronization output for the X and Y port outputs. It is low during the last eight bits of each superframe (every 3 ms) of the PCM serial or parallel output. This signal is used to determine the location of PCM signaling bits in Robbed-bit Signaling Mode or in Transition Signaling Mode for PCM channels that are transmitted transparently with Robbed-bit Signaling.

ADPCM SIGNALING FREEZE — FREEZ

When high, this input "freezes" signaling from the ADPCM (ZIN) input. This can be used in any signaling mode.

ADPCM PROCESSOR CLOCK PRCLK

This is the clock signal to the ADPCM processor. It provides a clock rate of 6.144, 12.288, or 16.384 MHz for 24, 48, or 64- channel operation respectively. In 48-channel gapped-clock mode, it is gapped once per frame for eight clock cycles to develop a 12.288 MHz clock.

ADPCM PROCESSOR SYNC PSYNC

This signal synchronizes the ADPCM processor to the ADPCM Line Formatter.

ADPCM PROCESSOR SERIAL INPUT SER_IN

This is the serial multiplexed signal input to the ADPCM processor.

ADPCM PROCESSOR SERIAL OUTPUT SER_OUT

This is the serial multiplexed signal output from the ADPCM processor.

ADPCM PROCESSOR CONTROL CNTRL

This is a multiplexed control lead to the processor which controls the algorithm reset function for diagnostics, channel transparency, and ADPCM processor configuration.

ADPCM PROCESSOR TABLE SELECTION CODE12, CODE13

These two control outputs control the table selection for the ADPCM processor. These bits are used for Robbed-bit Signaling and for selecting optional ADPCM coding tables.

POWER-ON RESET RESET

This active-low signal is used to initialize the ADPCM Line Formatter.

DIAGNOSTIC TEST RESULT OUTPUT DIAG

This output goes high if there is a failure in any diagnostic test channel.

.c.9.3 DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. Leakage current for each pin is less than 10 μA in any state.

All outputs have drive current I_{OL} = 2 mA at 0.4 Volts and I_{OH} = -2 mA at 2.4 Volts. All outputs are CMOS drive levels and can be used with CMOS or TTL logic. The maximum capacitance of any input or output pin is 10 pF.

Absolute maximum ratings are given below:

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	-0.3 to +7	V
Input Voltage	V_{in}	-0.3 to V_{DD}+0.3	V
DC Current Drain	I	25	mA
DC Input Leakage Current	I_{in}	± 10	μA
Storage Temp.	T_{STG}	-40 to +125	°C

Specified operating conditions are as follows:

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temp.	T_A	-40 to +85	°C
DC Input Voltage	V_{in}	0 - V_{DD}	V

.c.9.4 AC Characteristics

All signal outputs are guaranteed to settle beyond both TTL and CMOS worst-case input thresholds into a load capacitance of up to 50 pF within 40 ns of the corresponding clock transition.

Figures 27 and 28 show the timing requirements for the microcontroller interface. The timing performance of these signals is given in the following table.

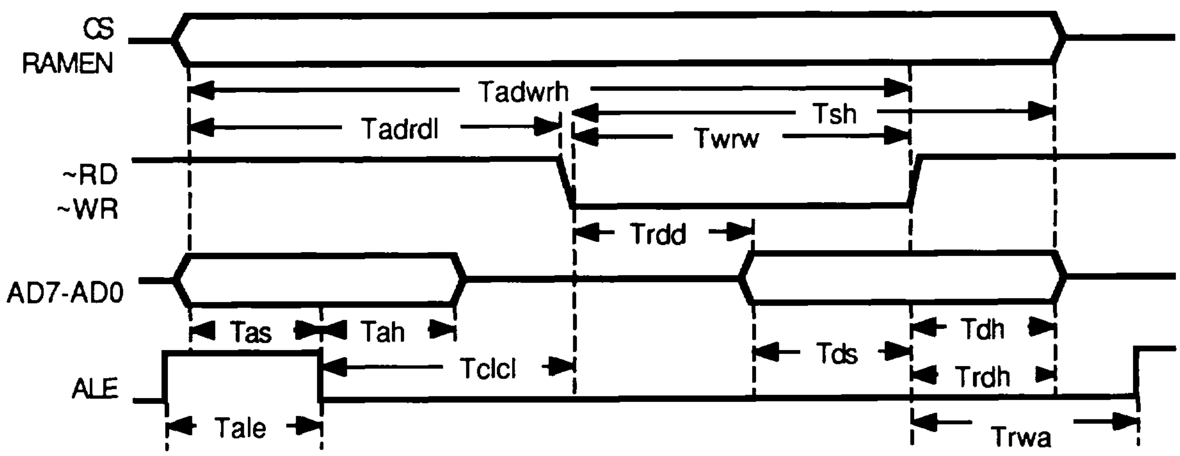

Figure 27. Microcontroller Interface Timing

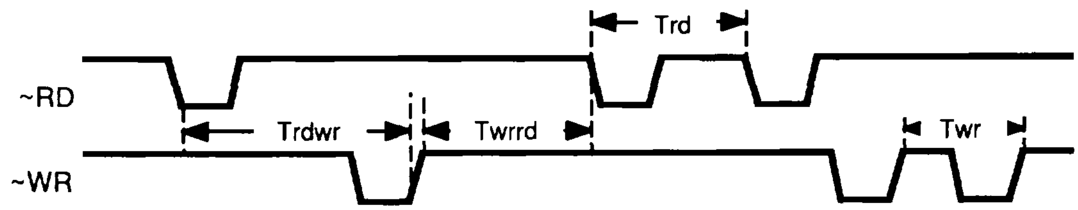

Figure 28. Microcontroller Read and Write Cycle Times to RAM

Symbol	Parameter	min	typ	max
Tale	address-latch-enable width	20		
Tadwrh	select/enable to write high	25	-	-
Tadrdl	select/enable to read low	10	-	-
Twrw	read/write pulse width	25	-	-
Trdd	read low to data available	-	-	25
Trdh	read data hold time	3	15*	-
Tas	address setup before ALE low	7	-	-
Tah	address hold after ALE low	10	-	-
Tclcl	ALE low to write/read low	10	-	-
Tds	write data stable before write high	25	-	-
Tdh	write data hold after write high	10	-	-
Trd	read cycle time	2920†	-	-
Twr	write cycle time	2920†	-	-
Trdwr	read followed by write cycle time	2920†	-	-
Twrrd	write followed by read cycle time	2920†	-	-

* The external address/data bus capacitance will increase the data hold time if the bus remains undriven.

† Time given is for a nominal 12.352 MHz system clock frequency. The minimum time allowed should be 36 times the system input clock period.

.c.9.5 Power Requirements

The formatter will meet all specifications over a temperature range of -40°C to 85°C and input voltage range of 4.75 to 5.25 Volts.

The maximum current required for the circuit in operation is 40 mA. Memories can be obtained to meet the specifications in Section 9.0 with typical current drains of 100 mA.

TABLE 1.

ADPCM LINE FORMATTER CONTROLLER ADDRESS MAP

	ADDRESS RANGE	CONTENTS
RAMEN=0:	000-003	Internal Control Registers (Write-Only)
	000-001	Internal Status Registers (Read-Only)
RAMEN=1:	000-3FF	Per-channel Control/Signaling Registers
	400-417	PCM Buffer - X Serial Input, Frame N
	420-437	PCM Buffer - Y Serial Input, Frame N
	440-47F	Encoder Signaling Buffer
	480-497	PCM Buffer - X Serial Output, Frame N
	4A0-4B7	PCM Buffer - Y Serial Output, Frame N
	4C0-4FF	Decoder Signaling Buffer
	500-517	PCM Buffer - X Serial Input, Frame N-1
	520-537	PCM Buffer - Y Serial Input, Frame N-1
	580-597	PCM Buffer - X Serial Output, Frame N-1
	5A0-5B7	PCM Buffer - Y Serial Output, Frame N-1
	5C0-5FF	Decoder Idle Signaling Buffer
	700-7FF	STPQ Error Correction Lookup Table
	800-1FFF	Diagnostic Test Input and Output Data

TABLE 2.

ADPCM LINE FORMATTER
INTERNAL CONTROL AND STATUS REGISTERS

MODE REGISTER (Address 00)

0	(reserved - set to 0)
1	Non-Signaling Mode
2	Out-of-band PCM Signaling
3	(reserved - set to 0)
4-5	Bundle 5 Signaling Mode/Gapped Clock
6-7	Processor Rate (Channel Capacity)

BUNDLE REGISTER (Address 01)

0-1	Bundle 1 Signaling Mode
2-3	Bundle 2 Signaling Mode
4-5	Bundle 3 Signaling Mode
6-7	Bundle 4 Signaling Mode

TEMPLATE REGISTER (Address 02)

0-1	Bundle 1 PCM Source
2-3	Bundle 2 PCM Source
4-5	Bundle 3 PCM Source
6-7	Bundle 4 PCM Source

PAGE REGISTER (Address 03)

0-4	RAM Address (8:12)
5	MSB-Only RAM Update
6-7	(not used)

STATUS REGISTER 0 (Address 00)

0	Bundle 1 CRC Check Result
1	Bundle 1 OOF
2	Bundle 2 CRC Check Result
3	Bundle 2 OOF
4	Bundle 3 CRC Check Result
5	Bundle 3 OOF
6	Bundle 4 CRC Check Result
7	Bundle 4 OOF

STATUS REGISTER 1 (Address 01)

0	Bundle 5 CRC Check Result
1	Bundle 5 OOF
2	ADPCM Processor Diagnostic Result

TABLE 3.

G.761 CHANNEL CONTROL WORD CONTENTS

Channel	PCM Input Read address		PCM Input Write address		PCM Output Read address		PCM Output Write address	
0	407	28B	402	31A	482	28A	480	30A
1	404	29B	406	31B	486	28B	481	31A
2	401	30A	403	0A	483	29A	484	30B
3	402	31A	407	0B	487	29B	485	31B
4	405	30B	400	1A	480	30A	482	0A
5	406	31B	404	1B	484	30B	483	0B
6	403	0A	401	2A	481	31A	486	1A
7	407	0B	405	2B	485	31B	487	2A
8	400	1A	402	3A	482	0A	480	1B
9	401	2A	406	3B	486	0B	484	2B
10	404	1B	403	4A	483	1A	481	3A
11	405	2B	407	4B	487	1B	482	4A
12	402	3A	400	5A	480	2A	485	3B
13	403	4A	404	5B	484	2B	486	4B
14	406	3B	401	6A	481	3A	483	5A
15	407	4B	405	6B	485	3B	480	6A
16	400	5A	402	7A	482	4A	487	5B
17	401	6A	406	7B	486	4B	484	6B
18	404	5B	403	8A	483	5A	481	7A
19	405	6B	407	8B	487	5B	482	8A
20	402	7A	400	9A	480	6A	485	7B
21	403	8A	404	9B	484	6B	486	8B
22	406	7B	401	10A	481	7A	483	9A
23	407	8B	405	10B	485	7B	480	10A
24	400	9A	402	11A	482	8A	487	9B
25	401	10A	406	11B	486	8B	484	10B
26	404	9B	403	12A	483	9A	481	11A
27	405	10B	407	12B	487	9B	482	12A
28	402	11A	400	13A	480	10A	485	11B
29	403	12A	404	13B	484	10B	486	12B
30	406	11B	401	14A	481	11A	483	13A
31	407	12B	405	14B	485	11B	480	14A
32	400	13A	402	15A	482	12A	487	13B
33	401	14A	406	15B	486	12B	484	14B
34	404	13B	403	16A	483	13A	481	15A
35	405	14B	407	16B	487	13B	483	17A
36	402	15A	400	17A	480	14A	482	16A
37	400	17A	404	17B	484	14B	486	16B
38	403	16A	401	18A	481	15A	485	15B
39	407	16B	405	18B	485	15B	487	17B
40	406	15B	402	19A	482	16A	480	18A
41	404	17B	406	19B	486	16B	481	19A
42	401	18A	403	20A	483	17A	484	18B
43	402	19A	407	20B	487	17B	485	19B
44	405	18B	400	21A	480	18A	482	20A
45	406	19B	404	21B	484	18B	483	21A
46	403	20A	401	22A	481	19A	486	20B
47	400	21A	405	22B	485	19B	487	21B

TABLE 3 (continued)

G.761 CHANNEL CONTROL WORD CONTENTS

48	407	20B	402	23A	482	20A	480	22A
49	404	21B	406	23B	486	20B	481	23A
50	401	22A	403	24A	483	21A	484	22B
51	402	23A	407	24B	487	21B	485	23B
52	405	22B	400	25A	480	22A	482	24A
53	406	23B	404	25B	484	22B	483	25A
54	403	24A	401	26A	481	23A	486	24B
55	400	25A	405	26B	485	23B	487	25B
56	407	24B	402	27A	482	24A	480	26A
57	404	25B	406	27B	486	24B	481	27A
58	401	26A	403	28A	483	25A	484	26B
59	402	27A	407	28B	487	25B	485	27B
60	405	26B	400	29A	480	26A	482	28A
61	406	27B	404	29B	484	26B	483	29A
62	403	28A	401	30A	481	27A	486	28B
63	400	29A	405	30B	485	27B	487	29B

TABLE 4.

PCM PORT INTERFACE

Pin Name	Parallel Mode Function	Serial Mode Function
ZIN	Not used	Serial input for Z port
ZOUT	Serial output for Z port	Serial output for Z port
XIN	Update "A" signaling input bit	Serial input for X port PCM
XSIG	Update "B" signaling input bit	Out-of-band X port signaling input
YIN	Update "C" signaling input bit	Serial input for Y port PCM
YSIG	Update "D" signaling input bit	Out-of-band Y port signaling input
PP11	"A" signaling bits	Serial output for X port data
PP10	"B" signaling bits	Serial output for X port signaling
PP9	"C" signaling bits	Serial output for Y port data
PP8	"D" signaling bits	Serial output for Y port signaling
PP7-PP0	ADPCM and unbuffered PCM bytes interleaved in both modes	

TABLE 5.

PCM AND SIGNALING BUFFER ADDRESSES
24- AND 48-CHANNEL ANSI MODES

CHANNEL	PCM INPUT	PCM OUTPUT	ENCODER SIGNALING	DECODER SIGNALING (active/idle)
X1	400/500	480/580	440	4C0/5C0
X2	401/501	481/581	441	4C1/5C1
X3	402/502	482/582	442	4C2/5C2
X4	403/503	483/583	443	4C3/5C3
X5	404/504	484/584	444	4C4/5C4
X6	405/505	485/585	445	4C5/5C5
X7	406/506	486/586	446	4C6/5C6
X8	407/507	487/587	447	4C7/5C7
X9	408/508	488/588	448	4C8/5C8
X10	409/509	489/589	449	4C9/5C9
X11	40A/50A	48A/58A	44A	4CA/5CA
X12	40B/50B	48B/58B	44B	4CB/5CB
X13	40C/50C	48C/58C	44C	4CC/5CC
X14	40D/50D	48D/58D	44D	4CD/5CD
X15	40E/50E	48E/58E	44E	4CE/5CE
X16	40F/50F	48F/58F	44F	4CF/5CF
X17	410/510	490/590	450	4D0/5D0
X18	411/511	491/591	451	4D1/5D1
X19	412/512	492/592	452	4D2/5D2
X20	413/513	493/593	453	4D3/5D3
X21	414/514	494/594	454	4D4/5D4
X22	415/515	495/595	455	4D5/5D5
X23	416/516	496/596	456	4D6/5D6
X24	417/517	497/597	457	4D7/5D7
Y1	420/520	4A0/5A0	458	4D8/5D8
Y2	421/521	4A1/5A1	459	4D9/5D9
Y3	422/522	4A2/5A2	45A	4DA/5DA
Y4	423/523	4A3/5A3	45B	4DB/5DB
Y5	424/524	4A4/5A4	45C	4DC/5DC
Y6	425/525	4A5/5A5	45D	4DD/5DD
Y7	426/526	4A6/5A6	45E	4DE/5DE
Y8	427/527	4A7/5A7	45F	4DF/5DF
Y9	428/528	4A8/5A8	460	4E0/5E0
Y10	429/529	4A9/5A9	461	4E1/5E1
Y11	42A/52A	4AA/5AA	462	4E2/5E2
Y12	42B/52B	4AB/5AB	463	4E3/5E3
Y13	42C/52C	4AC/5AC	464	4E4/5E4
Y14	42D/52D	4AD/5AD	465	4E5/5E5
Y15	42E/52E	4AE/5AE	466	4E6/5E6
Y16	42F/52F	4AF/5AF	467	4E7/5E7
Y17	430/530	4B0/5B0	468	4E8/5E8
Y18	431/531	4B1/5B1	469	4E9/5E9
Y19	432/532	4B2/5B2	46A	4EA/5EA
Y20	433/533	4B3/5B3	46B	4EB/5EB
Y21	434/534	4B4/5B4	46C	4EC/5EC
Y22	435/535	4B5/5B5	46D	4ED/5ED
Y23	436/536	4B6/5B6	46E	4EE/5EE
Y24	437/537	4B7/5B7	46F	4EF/5EF

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CAUTION

ESD-sensitive device.
Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
Do not insert this device into powered sockets.
Remove power before insertion or removal.

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