PRELIMINARY
Notice: This is not a final specification. Some parametric limits are Subject to change.

MITSUBISHI HIGH SPEED CMOS

M74HC648P/FP/DWP

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

DESCRIPTION

The M74HC648 is a semiconductor integrated circuit consisting of eight bus transceivers with inverted outputs.

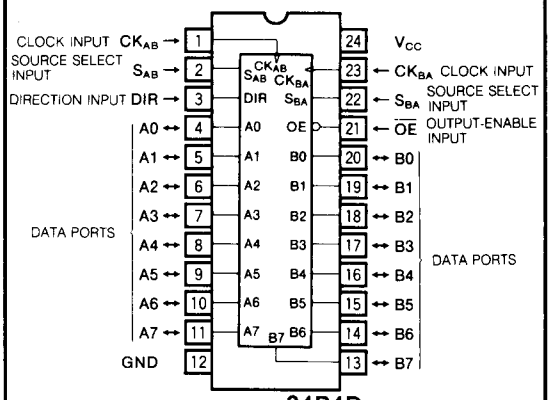
FEATURES

- High fon-out 3-state outputs (I_{OL}=6mA, I_{OH}=−6mA)
- High-speed: 70MHz clock frequency typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D
24P2
24P2V

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC648 to maintain the low power dissipation and high noise margin of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS648.

The M74HC648 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state inverted outputs. The I/O direction is controlled by output-enable input $\overline{OE}$ and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs S_{AB} and S_{BA}. The input signals are inverted when they appear at the output.

When $\overline{OE}$ is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When S_{AB} goes low, the inverted signal A, which was stored in flip flop (A) as Q_A when S_{AB} was high, appears at B. When SAB is held low and when clock input CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When S_{AB} is held high and when CK_{AB} changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the inverted signal $\overline{Q_A}$ which was stored in flip flop (A), appears at B.

When $\overline{OE}$ and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When S_{BA} goes low, and the inverted signal B, which was stored in flip flop (B) as Q_B when S_{BA} was high, appears at A. When S_{BA} is held low and clock input CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

When S_{BA} is held high and CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).At the same time, the inverted signal $\overline{Q_B}$ which was stored in flip flop (B), appears at A.

When $\overline{OE}$ is high, both A and B will become high impedance state and they will be separated. When CK_{AB} changes from low to high, the signal present at A is stored in flip flop (A). When CK_{BA} changes from low to high, the signal present at B is stored in flip flop (B).

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OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

Control inputs						Data ports				Flip Flop		Operational description
$\overline{OE}$	DIR	CK_{AB}	CK_{BA}	S_{AB}	S_{BA}	A		B		Q_A	Q_B	
H	X	X	X	X	X		X		X	Q_A^0	Q_B^0	The output of data ports A and B are disabled.
H	X	↑	X	X	X		L		X	Q_A^0	X	Data ports A and B are stored by the flip flops at the rising edge of CK_{AB} and CK_{BA}. The output of data ports A and B is disabled.
H	X	↑	X	X	X	I	H	I	X	Q_A^0	X	
H	X	X	↑	X	X		X		L	X	Q_B^0	
H	X	X	↑	X	X		X		H	X	Q_B^0	
L	H	X	X*	L	X		L		H	Q_A^0	Q_B^0	The output of data port B is enabled. (Note 2) 1) When S_{AB} is low, the data port A appears at data port B. The state of the flip flop (A) is unchanged.
L	H	X	X*	L	X		H		L	Q_A^0	Q_B^0	
L	H	X	X*	H	X	I	X	O	$\overline{Q_A^0}$	Q_A^0	Q_B^0	2) When S_{AB} is high, the output of flip flop (A) appears at data port B.
L	H	↑	X*	L	X		L		H	Q_A^0	Q_B^0	3) When S_{AB} is low, the data port A appears at data port B and is stored in flip flop (A) at the rising edge of CK_{AB}.
L	H	↑	X*	L	X		H		L	Q_A^0	Q_B^0	
L	H	↑	X*	H	X		L		$\overline{Q_A^0}$	Q_A^0	Q_B^0	4) When S_{AB} is high, the data port A is stored in flip flop (A) at the rising edge of CK_{AB}, and the output of flip flop (A) appears at data port B.
L	H	↑	X*	H	X		H		$\overline{Q_A^0}$	Q_A^0	Q_B^0	
L	L	X*	X	X	L		H		L	Q_A^0	Q_B^0	The output of data port A is enabled. (Note 3) 1) When S_{BA} is low, the data port B appears at data port A. The state of flip flop (B) is unchanged.
L	L	X*	X	X	L		L		H	Q_A^0	Q_B^0	
L	L	X*	X	X	H	O	$\overline{Q_B^0}$	I	X	Q_A^0	Q_B^0	2) When S_{BA} is high, the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	L		H		L	Q_A^0	Q_B^0	3) When S_{BA} is low, the data port B appears at data port A and is stored in flip flop (B) at the rising edge of CK_{AB}.
L	L	X*	↑	X	L		L		H	Q_A^0	Q_B^0	
L	L	X*	↑	X	H		$\overline{Q_B^0}$		L	Q_A^0	Q_B^0	4) When S_{BA} is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data pout A.
L	L	X*	↑	X	H		$\overline{Q_B^0}$		H	Q_A^0	Q_B^0	

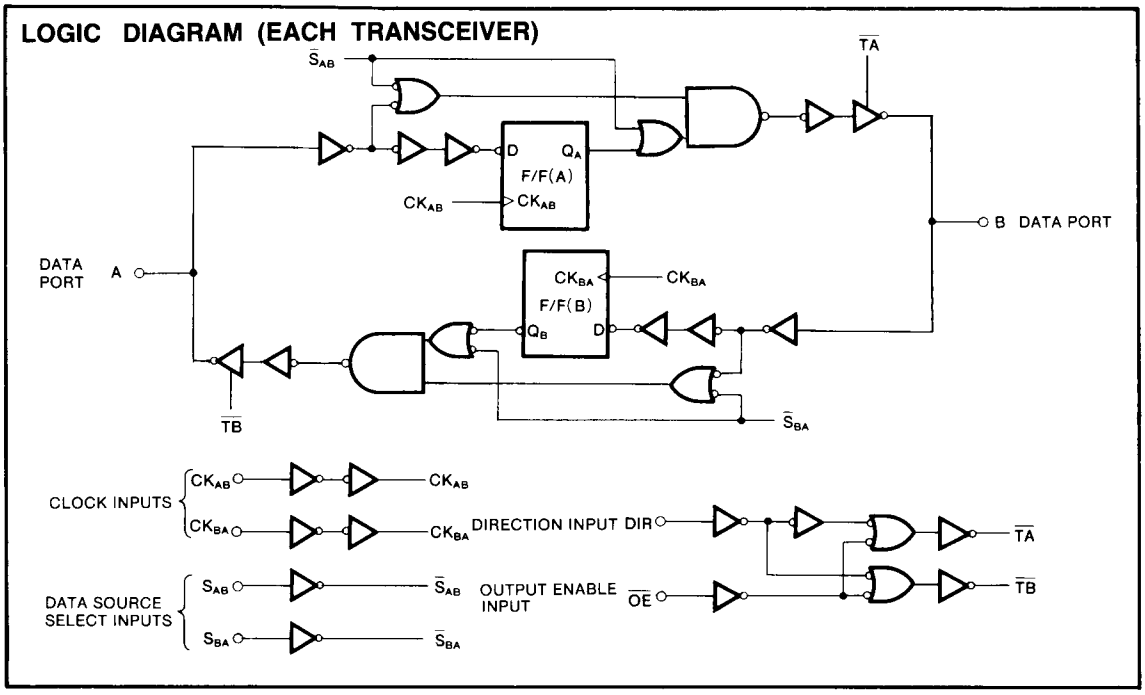
Note 1 : X : Irrelevant
↑ : Change from low to high
Q_A^0, Q_B^0 : Output state of flip flops before the rising edge of CK_{AB} and CK_{BA}.
I : Input terminal of data port
O : Output terminal data port
* : As CK_{AB} and CK_{BA} are not selected by the I/O direction signal, data from data ports A and B can be stored in the corresponding flip flops at the rising edge of CK_{AB} or CK_{BA}.

Note 2 : The outnput at data port B is given by:
$B = (\overline{A} \cdot \overline{S_{AB}}) + (\overline{Q_A} \cdot S_{AB})$

Note 3 : The output at data port B is given by:
$A = (\overline{B} \cdot \overline{S_{BA}}) + (\overline{Q_B} \cdot S_{BA})$

OCTAL 3-STATE INVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

LOGIC DIAGRAM (EACH TRANSCEIVER)



ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 4)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 4 : M74HC648FP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.
M74HC648DWP, T_a = −40∼+80℃ and T_a = 80∼85℃ are derated at −7mW/℃.

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V $\|I_O\|$ = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9			V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0			0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0			−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0			−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0			4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 50pF (Note 6)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level	C_L = 50pF (Note 6)			10	ns
t_{THL}	output transition time				10	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (A − B, B − A)				30	ns
t_{PLH}	Low-level to high-level and high-level to low-level				40	ns
t_{PHL}	output propagation time (CK_{AB} − B, CK_{BA} − A)				40	ns
t_{PLH}	Low-level to high-level and high-level to low-level				30	ns
t_{PHL}	output propagation time (S_{AB} − B, S_{BA} − A)				30	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5pF (Note 6)			30	ns
t_{PHZ}	(DIR − A, B)				30	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 6)			33	ns
t_{PZH}	(DIR − A, B)				33	ns
t_{PLZ}	Output disable time from low-level and high-level	C_L = 5pF (Note 6)			30	ns
t_{PHZ}	($\overline{OE}$ − A, B)				30	ns
t_{PZL}	Output enable time to low-level and high-level	C_L = 50pF (Note 6)			33	ns
t_{PZH}	($\overline{OE}$ − A, B)				33	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 6)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (A − B, B − A)		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK_{AB} − B, CK_{BA} − A)	C_L = 50pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLH}		C_L = 150pF (Note 6)	2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PHL}			2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (S_{AB} − B, S_{BA} − A)	C_L = 50pF (Note 6)	2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PHL}			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
t_{PLH}		C_L = 150pF (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PHL}			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
t_{PLZ}	Output disable time from low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

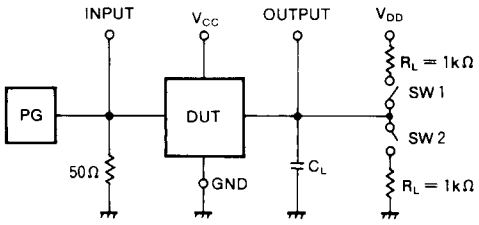
Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_{PZL}	Output enable time to low-level and high-level (DIR − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PLZ}	Output disable time from low-level and high-level ($\overline{OE}$ − A, B)	C_L = 50pF (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHZ}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}	Output enable time to low-level and high-level ($\overline{OE}$ − A, B)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZH}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PZL}		C_L = 150pF (Note 6)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PZH}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 5)								pF

Note 5 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)
The power dissipation during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions	Limits					Unit
			25℃			−40~+85℃		
		V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK_{AB}, CK_{BA} pulse width	2.0	80			101		ns
		4.5	16			20		
		6.0	14			17		
t_{su}	A, B setup time with respect to CK_{AB}, CK_{BA}	2.0	100			125		ns
		4.5	20			25		
		6.0	17			21		
t_h	A, B hlod time with respect to CK_{AB}, CK_{BA}	2.0	0			0		ns
		4.5	0			0		
		6.0	0			0		

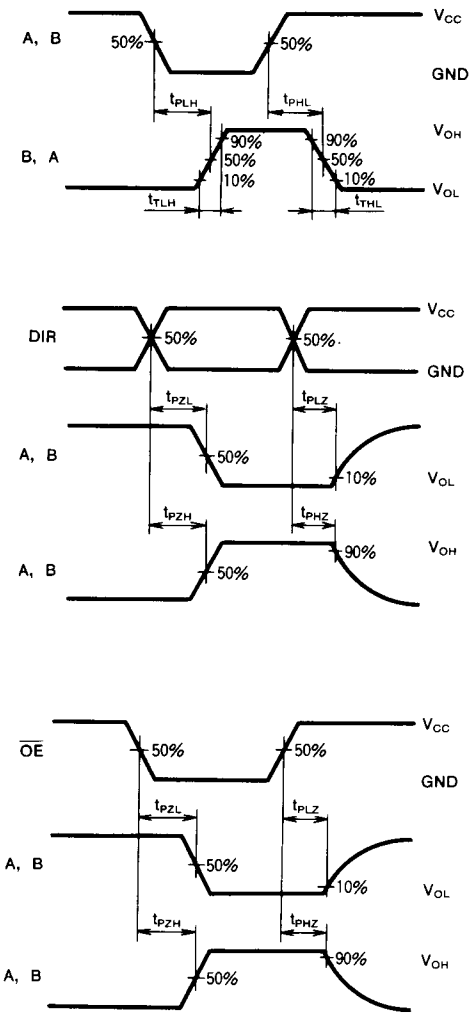
Note 6 : Test Circuit

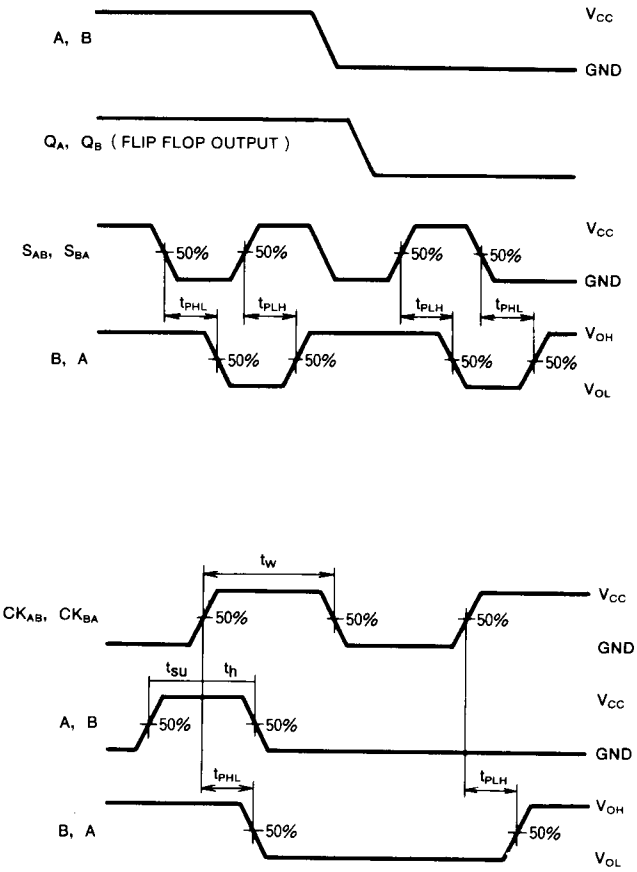


Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM





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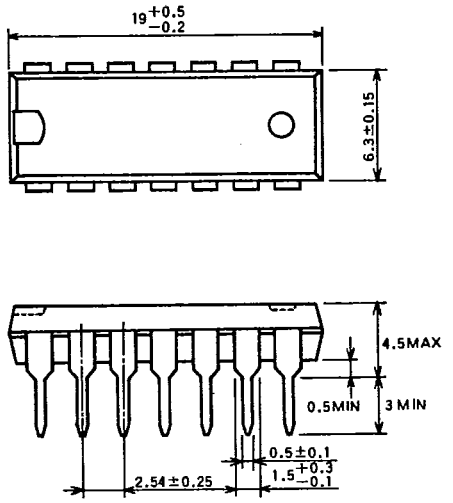
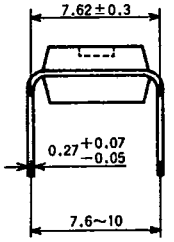
PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

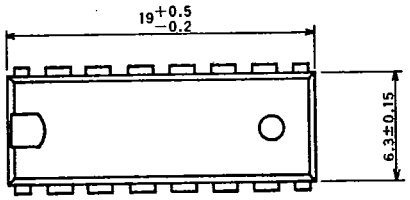
Dimension in mm

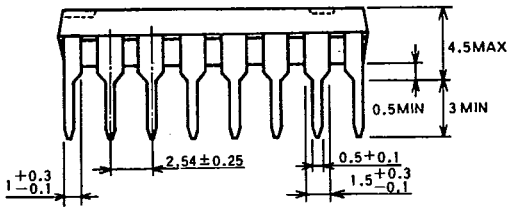


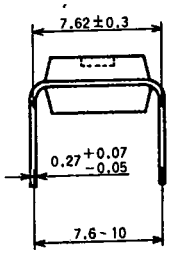


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm







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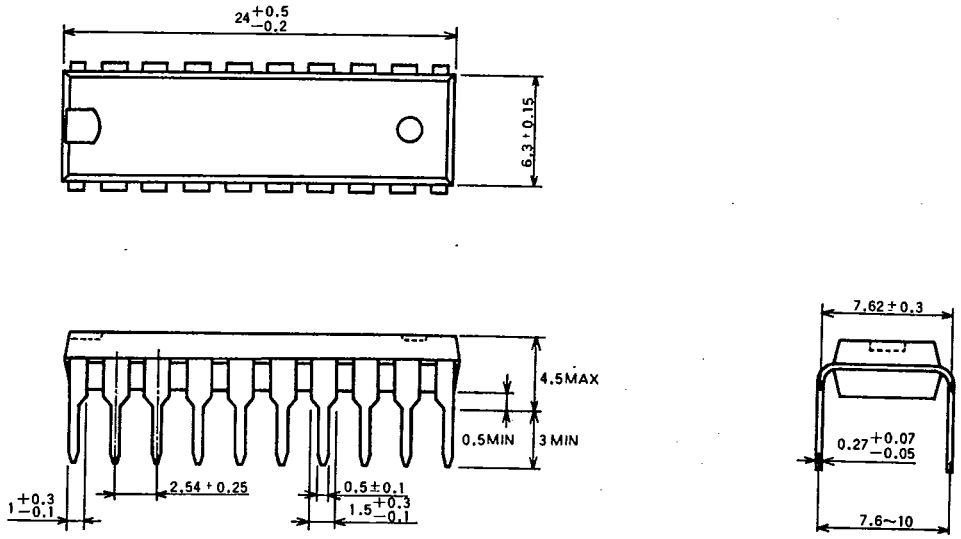
PACKAGE OUTLINES

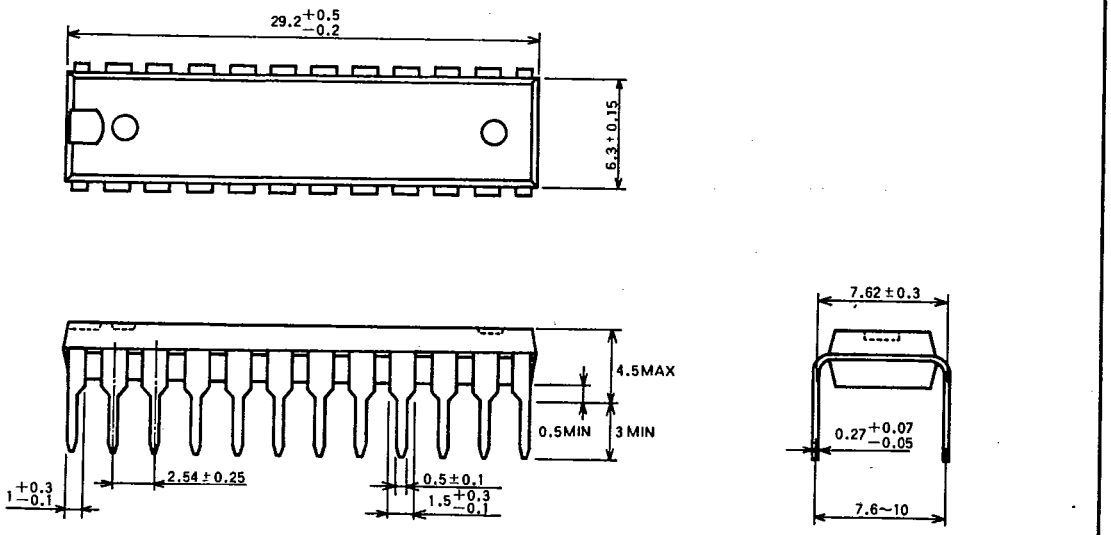
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



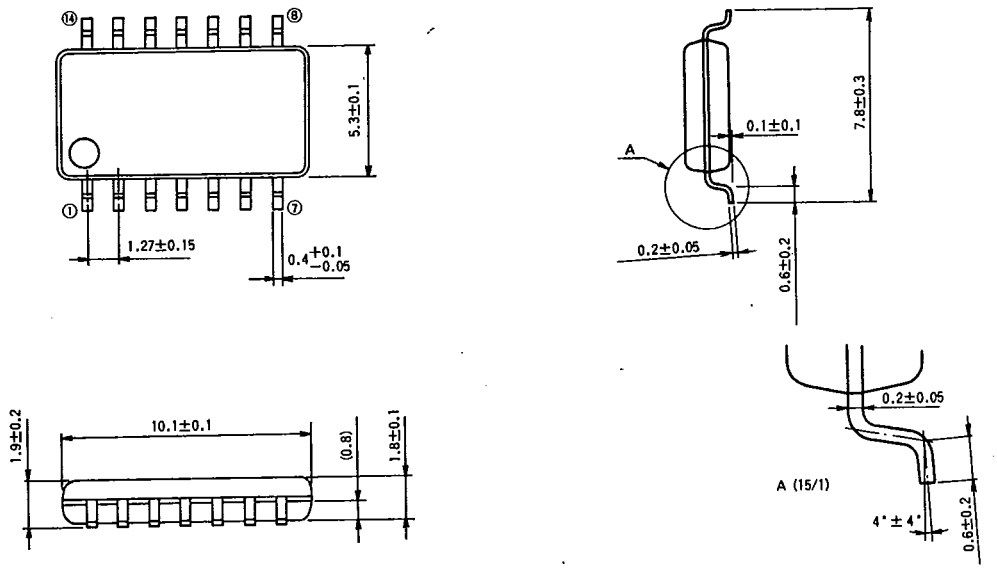
MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

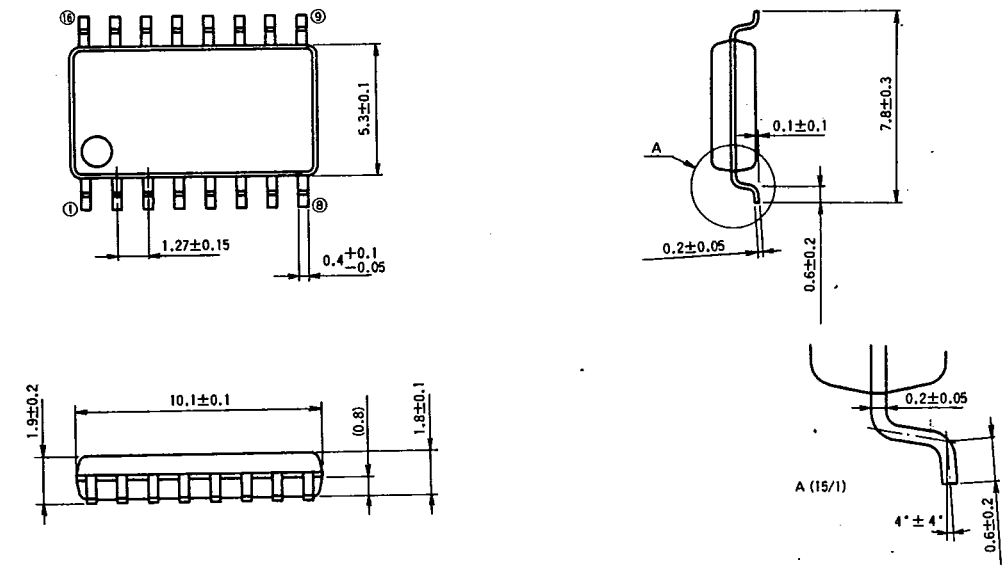
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

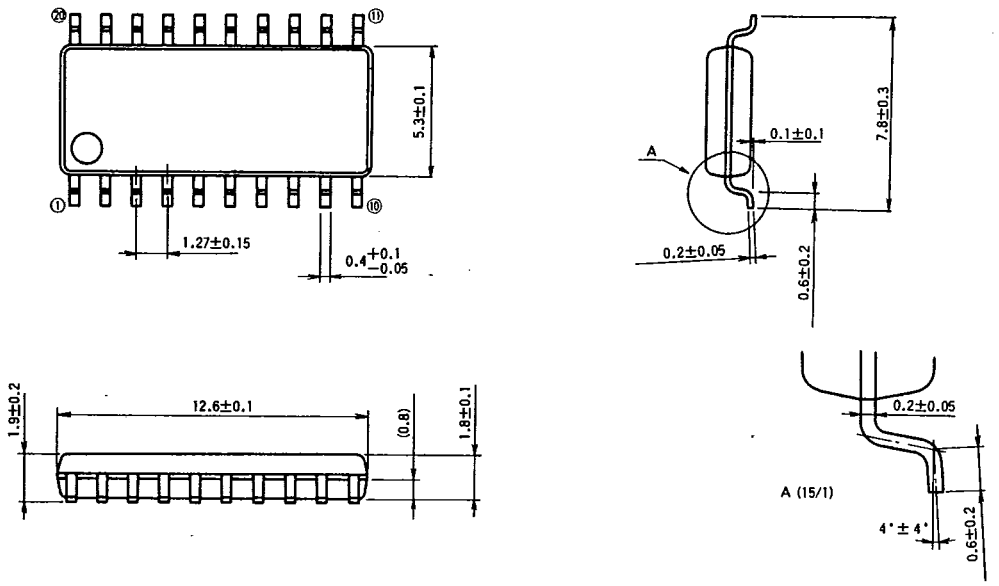
Dimension in mm



PACKAGE OUTLINES

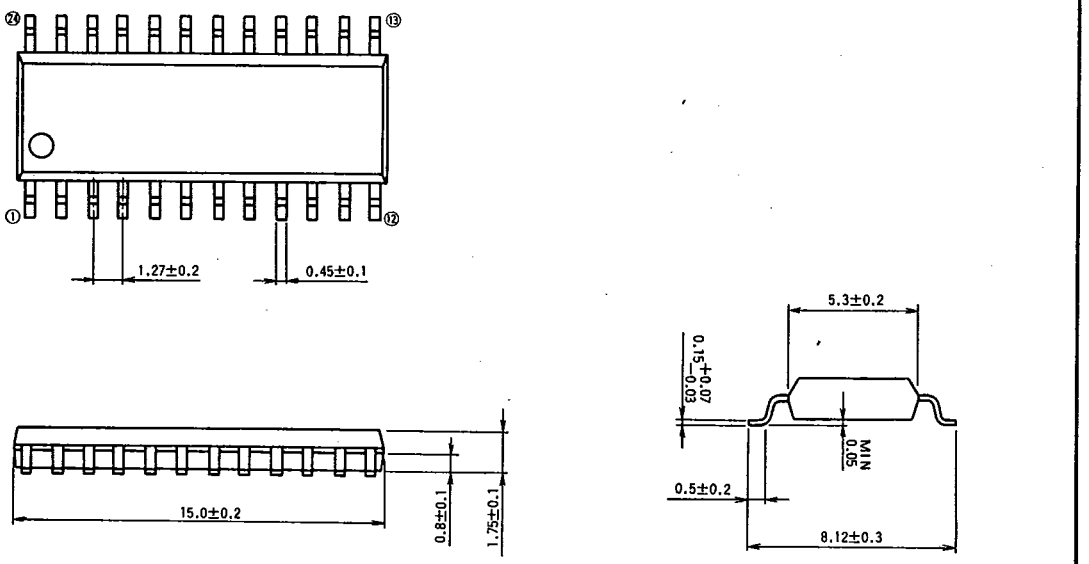
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

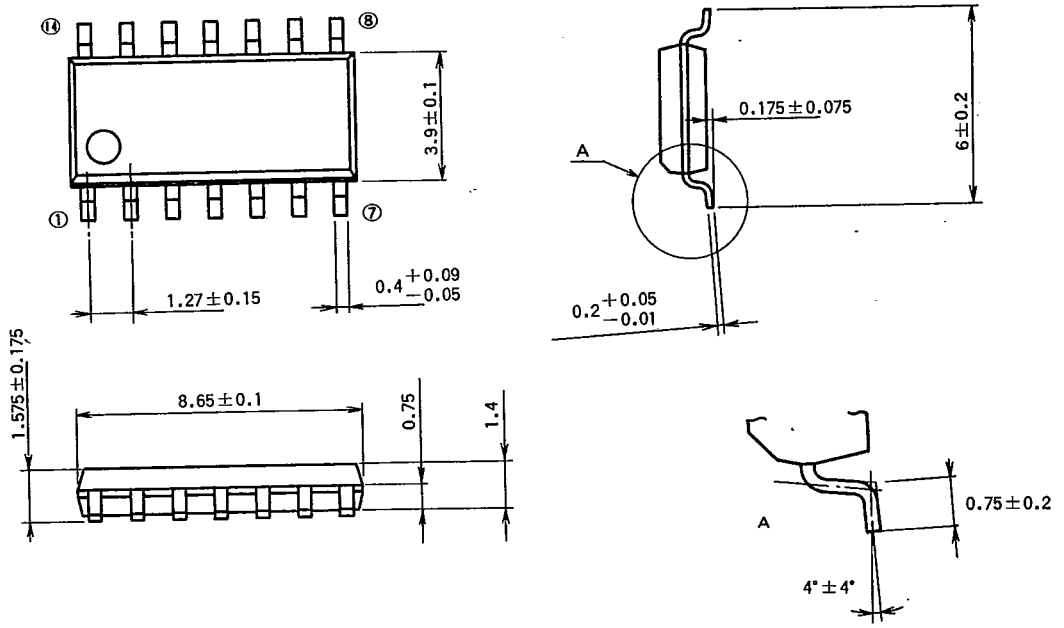


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

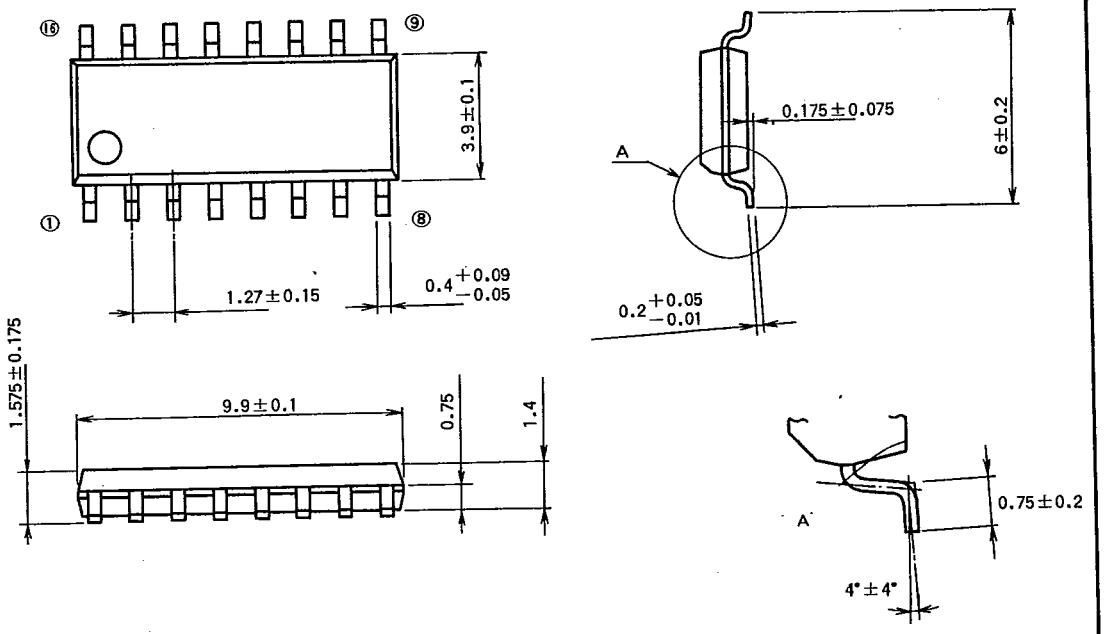
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm