

SYNCHRONOUS DRAM MODULE

MT4LSDT1632UD

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html

FEATURES

- JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
- 64MB (16 Meg x 32)
- Utilizes 125 MHz SDRAM components
- Single +3.3V $\pm 0.3V$ power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

OPTIONS

- Package
100-pin DIMM (gold)
- Timing (Cycle Timing)
8ns (125 MHz)

MARKING

G

-8

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-8	125 MHz	-	6ns	2ns	1ns
-8	100 MHz	6ns	-	2ns	1ns

*CL = CAS (READ) latency

PART NUMBER

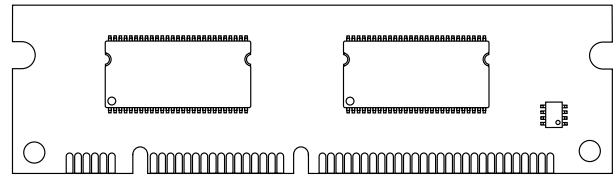
PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT4LSDT1632UDG-8_	16 Meg x 32	TSOP

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4LSDT1632UDG-8B1.

PIN ASSIGNMENT (Front View)

100-Pin DIMM

(H-5)



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	CKE1
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	S1#
5	DQ3	30	S2#	55	DQ11	80	S3#
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0	36	Vss	61	DQMB1	86	Vss
12	Vss	37	DQMB2	62	Vss	87	DQMB3
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	CK1	100	SA2

GENERAL DESCRIPTION

The MT4LSDT1632UD is a high-speed CMOS, dynamic random-access, 64MB solid-state memory organized in a x32 configuration. This module is configured as dual banks with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0 and CK1).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a

GENERAL DESCRIPTION (continued)

programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for a programmable READ or WRITE burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provide seamless, high-speed, random-access operation.

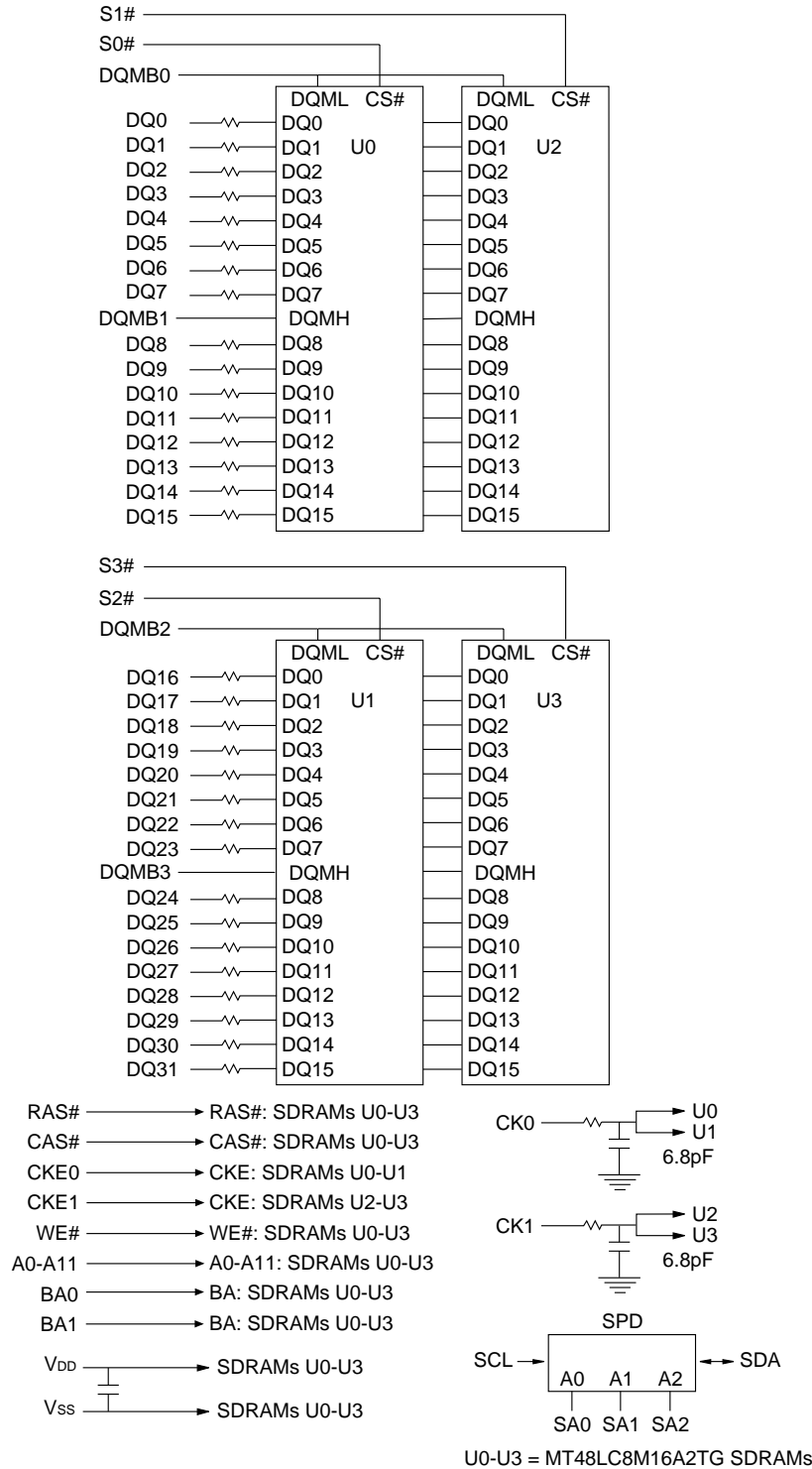
The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

**FUNCTIONAL BLOCK DIAGRAM
MT4LSDT1632UD (64MB)**



NOTE: 1. All resistor values are 10 ohms.
2. Reference designators in this diagram do not necessarily match the actual module.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
28, 72, 73	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#-S3#) define the command being entered.
25, 75	CK0, CK1	Input	Clock: CK0 and CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
27, 77	CKE0, CKE1	Input	Clock Enable: CKE0 and CKE1 activate (HIGH) and deactivate (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK0 and CK1, are disabled during power-down and self refresh modes, providing low standby power.
29, 30, 79, 80	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
11, 37, 61, 87	DQMB0-DQMB3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
19, 68	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
13-18, 63-67, 69	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A8, with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRE-CHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2-5, 7-10, 38-41, 43-46, 52-55, 57-60, 88-91, 93-96	DQ0-DQ31	Input/Output	Data I/Os: Data bus.
6, 21, 31, 42, 50, 56, 71, 81, 92	V _{DD}	Supply	Power Supply: +3.3V ±0.3V.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	V _{SS}	Supply	Ground.
48	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
23, 24, 74	RFU	–	Reserved for Future Use: These pins should be left unconnected.
22, 78	DNU	–	Do Not Use: These pins are not connected on this module but are assigned pins on the compatible DRAM version.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

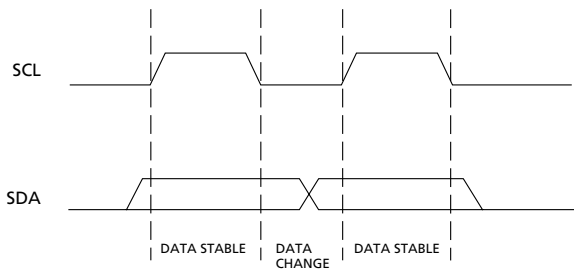
SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

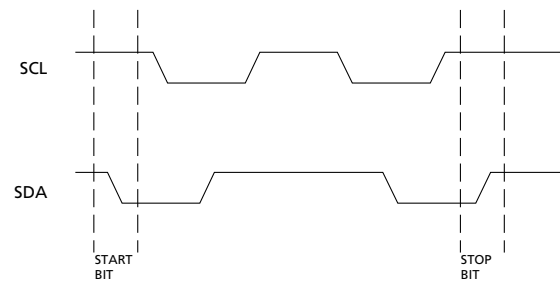
SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

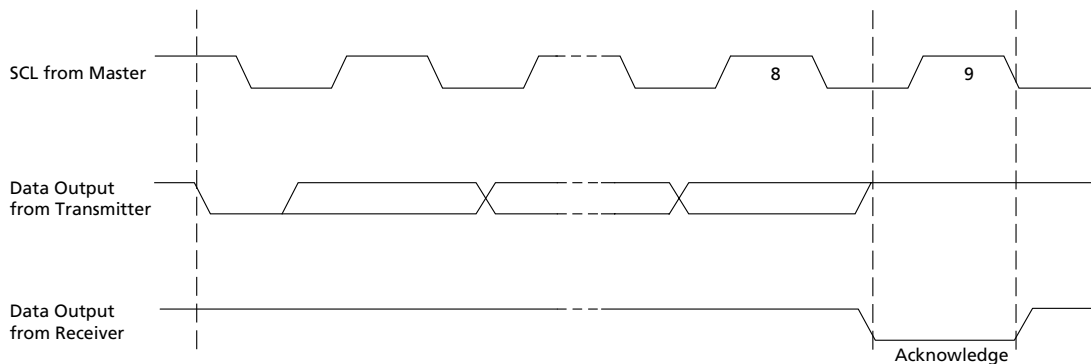
The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.



**Figure 1
Data Validity**



**Figure 2
Definition of Start and Stop**



**Figure 3
Acknowledge Response From Receiver**

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128		1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	SDRAM		0	0	0	0	0	1	0	0	04
3	NUMBER OF ROW ADDRESSES	12		0	0	0	0	1	1	0	0	0C
4	NUMBER OF COLUMN ADDRESSES	9		0	0	0	0	1	0	0	1	09
5	NUMBER OF BANKS	2		0	0	0	0	0	0	1	0	02
6	MODULE DATA WIDTH	32		0	0	1	0	0	0	0	0	20
7	MODULE DATA WIDTH (continued)	0		0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		0	0	0	0	0	0	0	1	01
9	SDRAM CYCLE TIME (CAS LATENCY = 3)	8	t_{CK}	1	0	0	0	0	0	0	0	80
10	SDRAM ACCESS FROM CLK (CAS LATENCY = 3)	6	t_{AC}	0	1	1	0	0	0	0	0	60
11	MODULE CONFIGURATION TYPE	NONPARITY		0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE	15.6 μ s/SELF		1	0	0	0	0	0	0	0	80
13	SDRAM WIDTH (PRIMARY SDRAM)	16		0	0	0	1	0	0	0	0	10
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		0	0	0	0	0	0	0	0	00
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	t_{CCD}	0	0	0	0	0	0	0	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		1	0	0	0	1	1	1	1	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4		0	0	0	0	0	1	0	0	04
18	CAS LATENCIES SUPPORTED	2, 3		0	0	0	0	0	1	1	0	06
19	CS LATENCY	0		0	0	0	0	0	0	0	1	01
20	WE LATENCY	0		0	0	0	0	0	0	0	1	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED		0	0	0	0	0	0	0	0	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0	0	0	0	1	1	1	0	0E
23	SDRAM CYCLE TIME (CAS LATENCY = 2)	10	t_{CK}	1	0	1	0	0	0	0	0	A0
24	SDRAM ACCESS FROM CLK (CAS LATENCY = 2)	6	t_{AC}	0	1	1	0	0	0	0	0	60
25	SDRAM CYCLE TIME (CAS LATENCY = 1)	–	t_{CK}	0	0	0	0	0	0	0	0	00
26	SDRAM ACCESS FROM CLK (CAS LATENCY = 1)	–	t_{AC}	0	0	0	0	0	0	0	0	00
27	MINIMUM ROW PRECHARGE TIME	20	t_{RP}	0	0	0	1	0	1	0	0	14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	20	t_{RRD}	0	0	0	1	0	1	0	0	14
29	MINIMUM RAS# TO CAS# DELAY	20	t_{RCD}	0	0	0	1	0	1	0	0	14
30	MINIMUM RAS# PULSE WIDTH	50	t_{RAS}	0	0	1	1	0	0	1	0	32
31	MODULE BANK DENSITY	32MB		0	0	0	0	1	0	0	0	08
32	COMMAND/ADDRESS SETUP	2	t_{AS}, t_{CMS}	0	0	1	0	0	0	0	0	20
33	COMMAND/ADDRESS HOLD	1	t_{AH}, t_{CMH}	0	0	0	1	0	0	0	0	10
34	DATA SIGNAL INPUT SETUP	2	t_{DS}	0	0	1	0	0	0	0	0	20
35	DATA SIGNAL INPUT HOLD	1	t_{DH}	0	0	0	1	0	0	0	0	10

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
36-61	RESERVED BYTES	–		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 2		0	0	0	0	0	0	1	0	02
63	CHECKSUM FOR BYTES 0-62			1	0	1	1	0	1	1	0	B6
64	MANUFACTURER'S JEDEC ID CODE	MICRON		0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)			1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION			0	0	0	0	0	0	0	1	01
				0	0	0	0	0	0	1	0	02
				0	0	0	0	0	0	1	1	03
				0	0	0	0	0	1	0	0	04
				0	0	0	0	0	1	0	1	05
				0	0	0	0	0	1	1	0	06
73-90	MODULE PART NUMBER (ASCII)			x	x	x	x	x	x	x	x	xx
91	PCB IDENTIFICATION CODE	1		0	0	0	0	0	0	0	1	01
		2		0	0	0	0	0	0	1	0	02
		3		0	0	0	0	0	0	1	1	03
		4		0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0		0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER			x	x	x	x	x	x	x	x	xx
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)			–	–	–	–	–	–	–	–	–

- NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description

of commands and operations, refer to the 128Mb: x4, x8, x16 SDRAM data sheet.

TRUTH TABLE 1 – COMMANDS AND DQMB OPERATION

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H ⁸	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H ⁸	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
 2. A0-A11 define the op-code written to the Mode Register.
 3. A0-A11 provide row address and BA0 and BA1 determine which bank is made active.
 4. A0-A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which bank is being read from or written to.
 5. A10 LOW: BA0 and BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0 and BA1 are "Don't Care."
 6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
 7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
 8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).

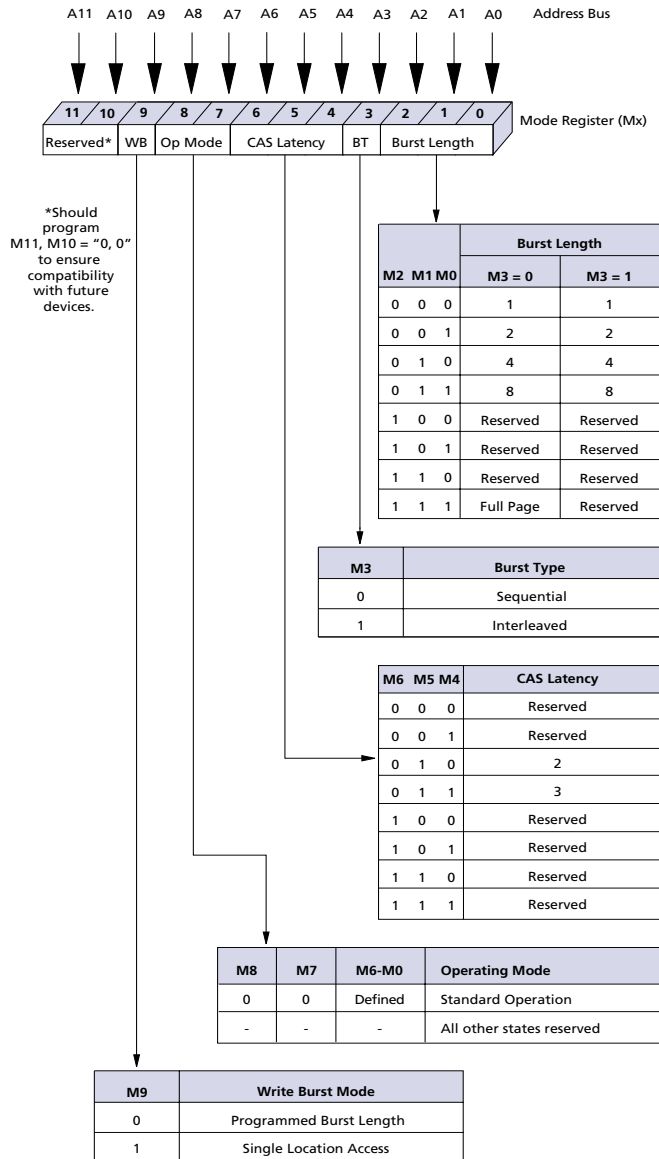


Figure 1
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	
Full Page (512)	n = A0-A8 (location 0-511)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

- NOTE:**
1. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
 2. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
 3. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
 4. For a full-page burst, the full row is selected, and A0-A8 select the starting column.
 5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
 6. For a burst length of one, A0-A8 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{DD} Supply	
Relative to V _{SS}	-1V to +4.6V
Voltage on Inputs, NC or I/O Pins	
Relative to V _{SS}	-1V to +4.6V
Operating Temperature, T _A (ambient) ..	0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Power Dissipation	4W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

 (Notes: 1, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V _{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V _{IH}	2	V _{DD} + 0.3	V	23
INPUT LOW VOLTAGE: Logic 0; All inputs	V _{IL}	-0.5	0.8	V	23
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} (All other pins not under test = 0V)	WE#, RAS#, CAS#, A0-A11, BA0, BA1	I _{I1}	-20	20	μA
	CK0-CK1, CKE0-CKE1, DQMB0-DQMB3	I _{I2}	-10	10	μA
	S0#-S3#	I _{I3}	-5	5	μA
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DD}	DQ0-DQ31	I _{OZ}	-10	10	μA
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -4mA) Output Low Voltage (I _{OUT} = 4mA)	V _{OH}	2.4	-	V	
	V _{OL}	-	0.4	V	

I_{DD} SPECIFICATIONS AND CONDITIONS

 (Notes: 1, 6, 11, 13) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES	
		-8			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN); CAS latency = 3	I _{DD1}	360	mA	3, 18, 19, 28	
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I _{DD2}	8	mA	28	
STANDBY CURRENT: Active Mode; CKE = HIGH; S0#-S3# = HIGH; All banks active after t _{RCD} met; No accesses in progress	I _{DD3}	160	mA	3, 12, 19, 28	
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3	I _{DD4}	360	mA	3, 18, 19, 28	
AUTO REFRESH CURRENT: CKE = HIGH; S0#-S3# = HIGH	t _{RC} = t _{RC} (MIN); CL = 3	I _{DD5}	800	mA	3, 12, 18, 19, 28
	t _{RC} = 15.625μs; CL = 3	I _{DD6}	180	mA	28
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD7}	6	mA	4	

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#	C _{I1}	12	22	pF	2
Input Capacitance: CE0, CE1	C _{I2}	6	12	pF	2
Input Capacitance: CK0, CK1	C _{I3}	6	10	pF	2
Input Capacitance: S0#-S3#	C _{I4}	4	7	pF	2
Input Capacitance: DQMB0#-DQMB3#	C _{I5}	7	12	pF	2
Input Capacitance: SCL, SA0-SA2	C _{I6}	–	6	pF	2
Input/Output Capacitance: DQ0-DQ31, SDA	C _{I0}	10	16	pF	2

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 8, 9, 11)

AC CHARACTERISTICS		-8			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)	CL = 3	t [†] AC	6	ns	
	CL = 2	t [†] AC	6	ns	
Address hold time		t [†] AH	1	ns	
Address setup time		t [†] AS	2	ns	
CLK high-level width		t [†] CH	3	ns	
CLK low-level width		t [†] CL	3	ns	
Clock cycle time	CL = 3	t [†] CK	8	ns	24
	CL = 2	t [†] CK	10	ns	24
CKE hold time		t [†] CKH	1	ns	
CKE setup time		t [†] CKS	2	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t [†] CMH	1	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t [†] CMS	2	ns	
Data-in hold time		t [†] DH	1	ns	
Data-in setup time		t [†] DS	2	ns	
Data-out high-impedance time	CL = 3	t [†] HZ	6	ns	10
	CL = 2	t [†] HZ	7	ns	10
Data-out low-impedance time		t [†] LZ	1	ns	
Data-out hold time (load)		t [†] OH	3	ns	
Data-out hold time (no load)		t [†] OH _N	1.8	ns	29
ACTIVE to PRECHARGE command period		t [†] RAS	50	120,000	ns
ACTIVE to ACTIVE command period		t [†] RC	70		ns
AUTO REFRESH period		t [†] RCAR	70		ns
ACTIVE to READ or WRITE delay		t [†] RCD	20		ns
Refresh period (4,096 cycles)		t [†] REF	64		ms
PRECHARGE command period		t [†] RP	20		ns
ACTIVE bank A to ACTIVE bank B command period		t [†] RRD	20		ns
Transition time		t [†] T	0.3	1.2	ns
WRITE recovery time		t [†] WR	1 CLK + 7ns	–	25
			15	ns	26
Exit SELF REFRESH to ACTIVE command		t [†] XSR	80		ns

*Specifications for the SDRAM components used on the module.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 8, 9, 11)

PARAMETER	SYMBOL	-8	UNITS	NOTES	
READ/WRITE command to READ/WRITE command	t_{CCD}	1	t_{CK}	17	
CKE to clock disable or power-down entry mode	t_{CKED}	1	t_{CK}	14	
CKE to clock enable or power-down exit setup mode	t_{PED}	1	t_{CK}	14	
DQM to input data delay	t_{DQD}	0	t_{CK}	17	
DQM to data mask during WRITES	t_{DQM}	0	t_{CK}	17	
DQM to data high-impedance during READs	t_{DQZ}	2	t_{CK}	17	
WRITE command to input data delay	t_{DWD}	0	t_{CK}	17	
Data-in to ACTIVATE command	t_{DAL}	4	t_{CK}	15, 21	
Data-in to precharge	t_{DPL}	2	t_{CK}	16, 21	
Last data-in to BURST STOP command	t_{BDL}	1	t_{CK}	17	
Last data-in to new READ/WRITE command	t_{CDL}	1	t_{CK}	17	
Last data-in to PRECHARGE command	t_{RDL}	2	t_{CK}	16, 21	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	t_{MRD}	2	t_{CK}	27	
Data-out to high-impedance from PRECHARGE command	CL = 3	t_{ROH}	3	t_{CK}	17
	CL = 2	t_{ROH}	2	t_{CK}	17

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	V_{OL}	-	0.4	V	
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to V_{DD}	I_{LI}	-	10	μA	
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to V_{DD}	I_{LO}	-	10	μA	
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$; All other inputs = GND or $3.3V + 10\%$	I_{SB}	-	30	μA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	-	2	mA	

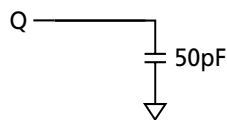
SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

(Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	t_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WRC}		10	ms	22

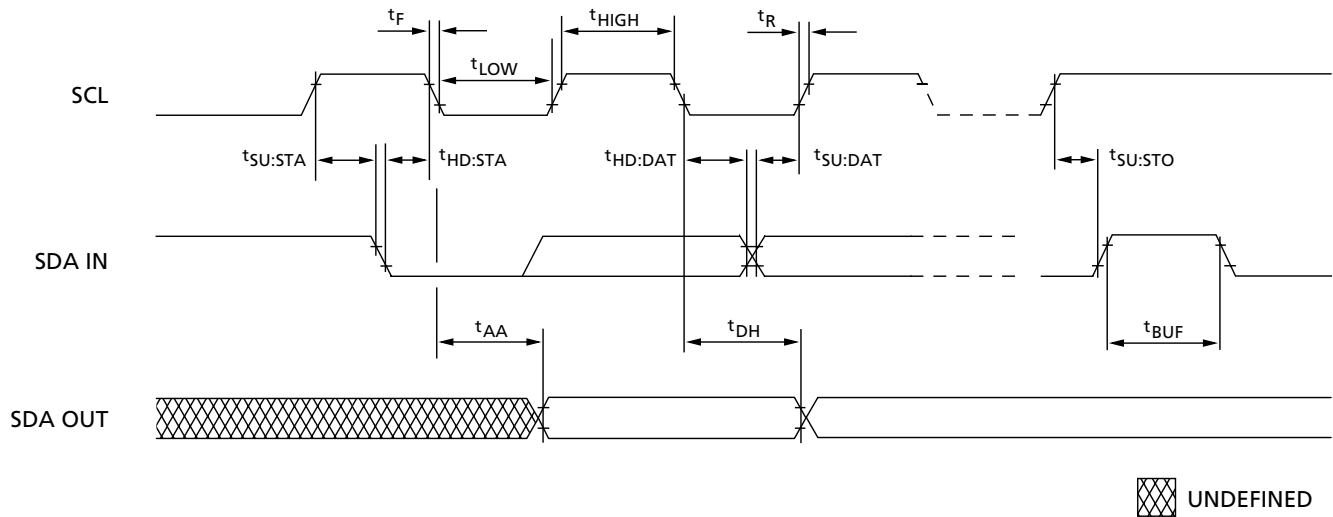
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1\text{ MHz}$.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) is ensured.
6. An initial pause of $100\mu\text{s}$ is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 1\text{ ns}$.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at $1.5V$ with equivalent load:



10. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} . The last valid data element will meet t_{OH} before going High-Z.
11. AC timing tests have $V_{IL} = 0V$ and $V_{IH} = 3V$, with timing referenced to $1.5V$ crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by t_{CKS} ; clock(s) specified as a reference only at minimum cycle rate.

15. Timing actually specified by t_{WR} plus t_{RP} ; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by t_{WR} .
17. Clocks required specified by JEDEC functionality and not dependent on any timing parameter.
18. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on $t_{CK} = 100\text{ MHz}$.
22. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to the pull-up resistor, and the EEPROM does not respond to its slave address.
23. V_{IH} overshoot: $V_{IH}(\text{MAX}) = V_{DD} + 2V$ for a pulse width $\leq 10\text{ ns}$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL}(\text{MIN}) = -2V$ for a pulse width $\leq 10\text{ ns}$, and the pulse width cannot be greater than one third of the cycle rate.
24. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR} , and PRECHARGE commands). CKE may be used to reduce the data rate.
25. Auto precharge mode only. The precharge timing budget (t_{RP}) begins 7 ns after the first clock delay, after the last WRITE is executed.
26. Precharge mode only.
27. JEDEC specifies three clocks.
28. $t_{CK} = 10\text{ ns}$ for -8.
29. Parameter guaranteed by design.

SPD EEPROM


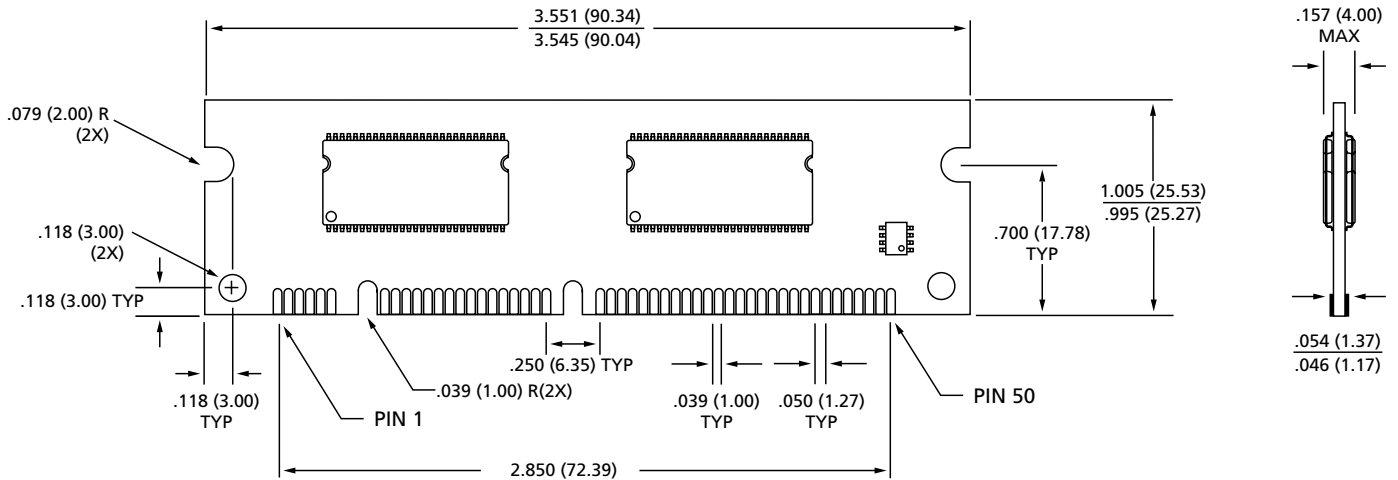
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**SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS**

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μs
t_{BUF}	4.7		μs
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μs
$t_{HD:STA}$	4		μs

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		μs
t_{LOW}	4.7		μs
t_R		1	μs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μs
$t_{SU:STO}$	4.7		μs

**100-PIN DIMM
(64MB)**



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



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