

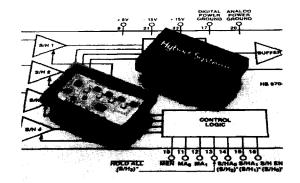
12-BIT ACCURATE QUAD SAMPLE/HOLD FOR SIMULTANEOUS/SEQUENTIAL SAMPLING

FEATURES

- Simultaneous sampling
- Sequential sampling
- Four complete 12-bit S/Hs with MUX, internal capacitors, control logic and buffered output in single 24-pin DIP
- Internally trimmed offsets and S/H step
- Control logic allows independent handling of MUX and S/Hs

DESCRIPTION

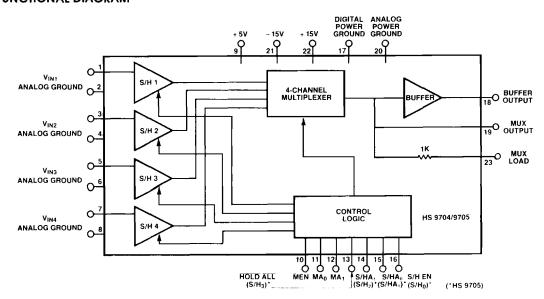
The HS9704/9705 consists of four complete 12-bit sample and holds with internal hold capacitors, MUX, control logic and a buffered output in a single 24-pin DIP. The HS9704 control logic allows simultaneous holding of all four S/Hs or holding of one at a time. The HS9705 allows the flexibility to hold any combination of S/Hs at any time. Simultaneous sampling allows the user to take a snapshot of up to four input signals, freezing their values in a 5 nanosecond aperture uncertainty across all channels. An analog ground pin is available at each sample and hold input to make it convenient



for shielding the analog input signals. The HS9704/9705 is particularly suited for use with the HS574 A/D, the HSADC85 and the HS5200 series.

The HS9704/9705 is packaged in a 24-pin DIP and is specified for operation from 0°C to +70°C for commercial grades and from -55°C to +125°C for military grades. Full screening to MIL-STD-883 Rev. C, Levels B or S, is available.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical $@+25\,^{\circ}\text{C}$ and nominal supply voltages, unless otherwise noted)

MODEL	HS 9704/HS 9705
DYNAMIC CHARACTERISTICS	
Acquisition Time to 0.01%, 20V step	4 μ sec typ, 7 μ sec (max)
Aperture Delay	200 nsec
Aperture Delay Variation between	
Channels	5 nsec
Aperture Uncertainty	200 psec
Settling Time (Hold Mode, to 0.01%)	800 nsec
Output Settling* (10V step, to 0.01%) Droop Rate	1 μsec typ, 3 μsec max
@ +25°C @ +125°C	35 V/msec 2 mV/msec
Sample to Hold Offset (Pedestal)	±1 mV typ, ±2.5 mV max
Feedthrough (Hold Mode) @ 1 kHz	- 80 dB
Power Supply Rejection Ratio	60 dB (+15V),
r over capply hejection hatte	80 dB (- 15V)
Crosstalk (Channel to Channel)	-80 dB max
	55 52 1115H
TRANSFER CHARACTERISTICS	+1
Gain	500 kHz
Full Power Bandwidth	
Slew Rate	13V/ µs
DC Gain Linearity (Sample Mode)	0.015% typ, 0.035% max
ANALOG INPUT/OUTPUT CHARACT	FERISTICS
Voltage Range	± 10V min
Absolute Max Input Voltage	± V supply
Offset Voltage Matching between S/Hs	\pm 0.3 mV typ, \pm 1 mV max
Offset Over Temperature Range	±2 mV typ, ±5 mV max
Input Bias Current	50 nA max, 100 nA @ +125°C
Input Impedance	1010
Buffered Output Resistance	0.05 ♀ typ, 0.2 ♀ max
DIGITAL INPUT CHARACTERISTICS	;
Input Voltage	
Low	<+0.8 volt
High	>+2.4 volt
Input Current	
Leakage	±1μ A
POWER REQUIREMENTS	
Supply Voltage Range	± 15V, ± 1V + 5V, ± 0.5V
Current Drain	
+ 15V	37 mA typ, 46 mA max
– 15V	37 mA typ, 46 mA max
+ 5V	5 mA typ, 8 mA max
Power Dissipation	1W typ,
	1.5W max

0°C to +70°C

-55°C to +125°C

-65°C to +150°C

24-pin ceramic DIP

TEMPERATURE RANGE

Operating

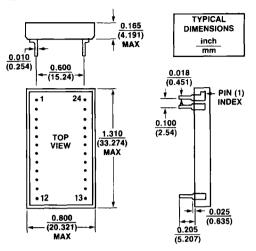
С

В

Storage MECHANICAL

Case Style

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN-OUT FOR HS 9704 (* - HS 9705)

PIN	FUNCTION	PIN	FUNCTION
1	VINO	24	NC
2	ANALOG GROUND	23	MUX LOAD**
3	V _{IN1}	22	+ 15V
4	ANALOG GROUND	21	– 15V
5	V _{IN2}	20	ANALOG POWER GROUND
6	ANALOG GROUND	19	MUX OUT
7	V _{IN3}	18	BUFFER OUT
8	ANALOG GROUND	17	DIGITAL POWER GROUND
9	+5V	16	S/HEN (S/H0)*
10	MEN	15	S/HA0 (S/H1)*
11	MAO	14	S/HA1 (S/H2)*
12	MA1	13	HOLD ALL (S/H3)*

Note: NC — No Internal Connection

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

(Exceeding any one of these parameters may cause permanent damage to the unit)

Analog Input Voltage ± 15V
Logic Input Voltage
Output Buffer Short Circuit Duration indefinite
Output Mux Short Circuit Duration indefinite @ 20 mA max
Supply Voltages ± 18V max + 5V - 0.5V to + 7V
Temperature Soldering Duration 10 sec @ 300°C Storage Temperature Range 65°C to + 150°C

^{*}Includes switching of MUX and settling of output buffer

^{**}MUX LOAD must be grounded for proper operation.

APPLICATIONS INFORMATION

(Ref. Application Note — QUAD S/H Solves Acquisition Problems)

CONTROL FUNCTIONS

All control functions are described in Tables 1, 2, and 3.

MEN	MAO	MA1	V _{ОUТ}
н	×	x	×
L	L	L	S/H0
L	Н	L	S/H1
L	L	н	S/H2
L	Н	н	S/H3

Table 1. MUX Truth Table (HS 9704/9705)

S/HEN	HOLD ALL	S/HA0	S/HA1	FUNCTION
Х	L	X	Х	ALL HOLD
L	н	L	L	ONLY S/H0 HOLD
L	н	Н	L	ONLY S/H1 HOLD
L	н	L	Н	ONLY S/H2 HOLD
L	н	Н	Н	ONLY S/H3 HOLD
Н	н	Х	Х	ALL TRACK

Table 2. S/H Truth Table (HS 9704)

S/H0	S/H1	S/H2	S/H3	FUNCTION
L	Х	X	Х	S/H0 Hold
X	L	Х	Х	S/H1 Hold
X	×	L	×	S/H2 Hold
X	×	X	L	S/H3 Hold
Ca	an hold any S/H's at	combinatior any time	n of	<u></u>

Table 3. S/H Truth Table (HS 9705)

NOTES:

1. L'indicates logic LOW 2. X indicates don't care.

S/H STEP

The S/H step (also known as the sample-to-hold offset) depends on the input voltage. We have internally trimmed the step to be less than 1 mV for a grounded input. With the internally trimmed offset matching, this makes the offsets in both track and hold mode negligible across all channels for a 12-bit system. The S/H step with $+\,10V$ input is $+\,3.5$ mV and with $-\,10V$ input is $-\,3.5$ mV and it is linear over the $\pm\,10V$ range.

This S/H step on the HS 9705 is also dependent on the S/H control lines. To improve the S/H step, pull up each S/H control line to the +5V supply through a 1K resistor.

INPUT EXPANSION

The HS 9704/05 can be easily expanded to more channels by connecting two or more devices in parallel. Also two (or multiples thereof) of the 9704/05s can be configured in a differential mode using an additional instrumentation amplifier.

Single-Ended Mode: Since the output of the analog multiplexer inside the HS 9704/05 can be disabled using the MEN input (pin 10), the output of another

multiplexer can be fed into the input of the buffer amplifier. Figure 1 shows how to connect two HS 9704/05s in parallel to achieve eight input channels.

The MUX OUTPUT pins of both devices are tied together, and because the output buffer amplifiers of both devices remain connected to the multiplexer outputs there will be two independant outputs, tracking each other within a few millivolts. Only one MUX LOAD should be grounded to avoid overloading the S/H. One of them might be used to drive the following circuit (like an A/D converter) while the other one can be used for test and measurement purposes. Normally when a probe is connected to the buffer output, it's capacitance and lead length will have some influence on the measured signal, like ringing, overshoot etc. If the other buffer output is used for measurements, the probe will have no influence on the signal which goes to the ADC.

MUX TRUTH TABLE

MEN	MAO	MA1	Vout
н	L	L	V0
Н	Н	L	V1
н	L	Н	V2
н	Н	н	V3
L	L	L	V4
L	Н	L	V5
L	L	Н	V6
L	Н	Н	V7

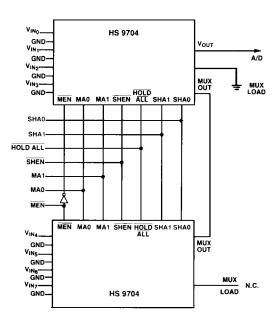


Figure 1. Single-Ended Mode

APPLICATIONS INFORMATION (continued)

INPUT EXPANSION (continued)

Differential Mode: Four differential channels can be held simultaneously, if two HS 9704/05s are connected using an additional instrumentation amplifier as shown in Figure 2. Another solution to that problem could be to use four instrumentation amplifiers in front of one Quad S/H, but this will require 16 instead of 4 precisely matching resistors and offset adjustment has to be made for four amplifiers instead of one. As in the single-ended mode more channels can be achieved by simply adding more Quad S/Hs in parallel. Four of them will be required for eight differential channels, six for 12 channels and so on.

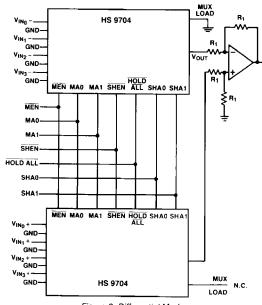


Figure 2. Differential Mode

TIMING DIAGRAMS

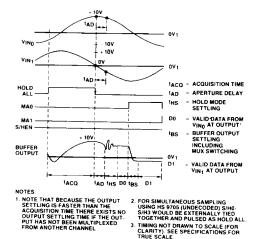


Figure 3. Timing Diagram of Simultaneous Sampling (HS 9704)2

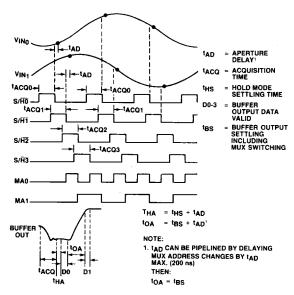


Figure 4. Pipelined Acquisition Sequential Sampling Using HS 9705.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE	-
HS 9704B	QUAD S/H, MIL-STD-883 Rev. C	-55°C to +125°C)
HS 9705B	QUAD S/H, MIL-STD-883 Rev. C (Hold any combination)	-55°C to +125°C	^
HS 9704C	QUAD S/H	0°C to +70°C	
HS 9705C	QUAD S/H (Hold any combination)	0°C to +70°C	

