VS29G01

4 Bit Microprocessor Slice

Features

- Functionally equivalent to Am2901C
- V_{REF} input flexibility for tracking 10K/10KH ECL input signals
- Available in commercial or military temperature range
- Single ECL power supply: V_{TT} = -2.0 ± 0.1 V
- Supports clock rates up to 75 MHz
- Compatible with ECL 100K signal levels
- Choice of 10ns or 15ns maximum address to result time

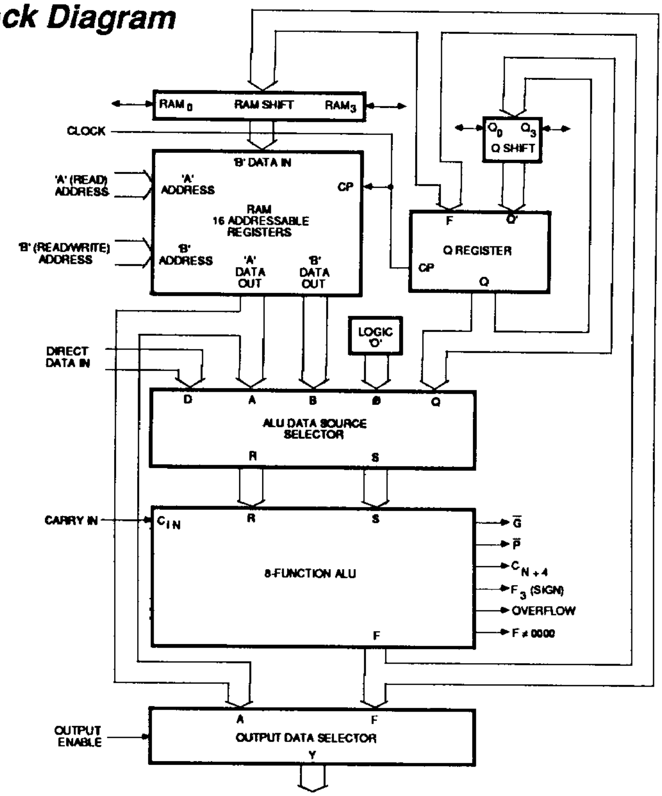
Functional Description

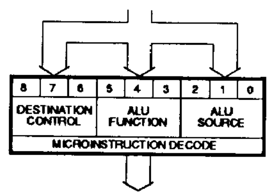
The VS29G01 is a high speed, expandable, four-bit ALU that can be used to implement high performance CPUs, peripheral controllers, and programmable microprocessors. Micro-instruction flexibility permits emulation of any high performance computer.

The device consists of a 16-word by 4-bit dual port RAM, a high-speed 4-bit ALU, and associated shifting, decoding, and multiplexing circuitry. Its 9-bit instruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function and the ALU destination register. Expandable with full look-ahead or ripple-carry, the device has an Output Enable control, and provides various status flag outputs for the ALU.

The VS29G01 is fabricated in gallium arsenide, using a high yielding enhancement/depletion mode technology that achieves high speed with low power dissipation. The VS29G01 is packaged in a ceramic 52-pin LDCC or LCC.

Block Diagram





Architecture

A detailed block diagram of the VS29G01 microprogrammable microprocessor structure is shown on page 1-3. The circuit is a four-bit slice, cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the block diagram are the 16 word by 4-bit, 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Similarly, data in any of the16-words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output field data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

As seen in the detailed block diagram, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0, and Q0. It is apparent that AD, AQ, and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The VS29G01 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the ***I 0, I 1,*** and ***I 2*** inputs. The definition of ***I 0, I 1,*** and ***I 2*** for the eight source operand combinations are shown in the 'ALU Source Operand Control' table on page 1-4. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a seperate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The ***I 3, I 4*** and ***I 5*** microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in the 'ALU Function Control' table also on page 1-4. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, ***$\overline{G}$***, and carry propogate, ***$\overline{P}$***, are outputs of the device for use with a carry look-ahead generator such as the VS29G02. A carry-out, ***Cn+4***, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in ***(Cn)*** and carry-out ***(Cn+4)*** are active HIGH.

The ALU has three other status-oriented outputs. These are ***F 3, F ≠ 0***, and overflow ***(OVR)***. The ***F 3*** output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the data outputs. ***F 3*** is non-inverted with respect to the sign bit output ***Y 3***. The ***F ≠ 0*** output is used for zero detect and can be wire OR'd between microprocessor slices. ***F ≠ 0*** output is LOW when all F outputs are LOW. The overflow output ***(OVR)*** is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output ***(OVR)*** is HIGH when overflow exists. That is, when ***Cn+3*** and ***Cn+4*** are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of the ALU destination functions are available as defined by the ***I 6, I 7,*** and ***I 8*** microinstruction inputs. These combinations are shown in the 'ALU Destination Control' table on page 1-4.

The four-bit data output field ***(Y)*** features outputs that can be directly bus organized. An output control ***(OE)*** is used to enable the outputs. When ***OE*** is LOW the ***Y*** outputs are in the high impedance state.

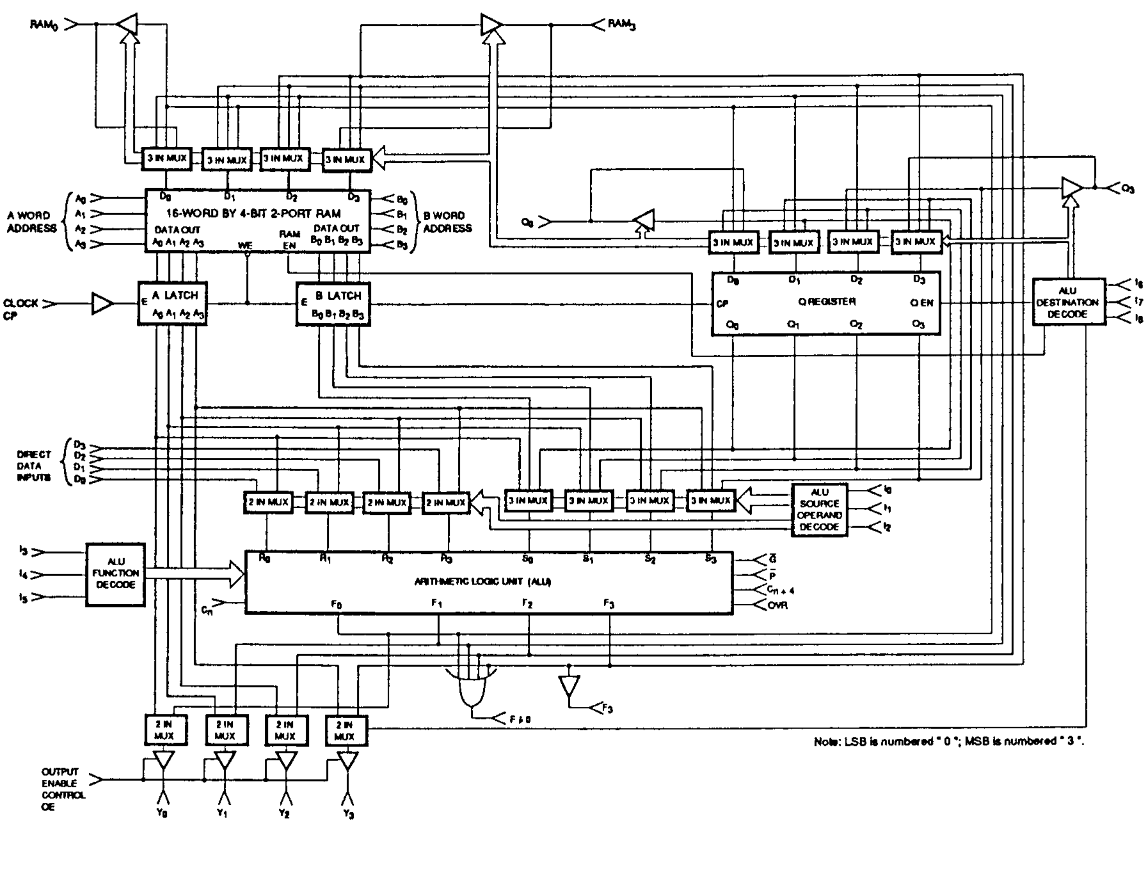
A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs *(F)* are selected at the device *Y* outputs. This selection is controlled by the ***I 6, I 7,*** and ***I 8*** microinstruction inputs. Refer to the 'ALU Destination Control' table for the selected output for each microinstruction code combination.

As was discussed previously, the ***RAM*** inputs are driven from a 3-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (x2) or shifted down one position (÷ 2). The shifter has two ports; one is labeled ***RAM 0*** and the other is labeled ***RAM 3***. Both of these ports consist of a buffer-driver and an input to the multiplexer. Thus, in the shift up mode, the ***RAM 3*** buffer is enabled and the ***RAM 0*** multiplexer input is enabled. Likewise, in the shift down mode, the ***RAM 0*** buffer and ***RAM 3*** input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the ***I 6, I 7*** and ***I 8*** micro-instruction inputs as defined in the 'ALU Function Control' table.

The Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter has two ports; one is ***Q 0*** and the other is ***Q 3***. The operation of these two ports is similar to the RAM shifter and is also controlled from ***I 6, I 7,*** and ***I 8*** as shown in the 'ALU Destination Control' table.

The clock input to the VS29G01 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B Address field when the clock input is LOW.

Detailed VS29G01 Microprocessor Block Diagram



Note: LSB is numbered " 0 "; MSB is numbered " 3 ".

Functional Tables

ALU Source Operand Control

Mnemonic	Micro Code				ALU Source Operands	
	I2	I1	I0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU Function Control

Mnemonic	Micro Code				ALU Function	Symbol
	I5	I4	I3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \nabla S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

ALU Destination Control

Mnemonic	Micro Code				RAM Function		Q-Register Function		Y Output	RAM Shifter		Q Shifter	
	I8	I7	I6	Octal Code	Shift	Load	Shift	Load		RAM 0	RAM 3	Q 0	Q 3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→ B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→ B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is an ECL input internally connected to an output in the high-impedance state.
B = Register addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Source Operand and ALU Functional Matrix

OCTAL I_{543}	ALU Function	I_{210} OCTAL							
		0	1	2	3	4	5	6	7
		ALU Source							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	Cn = L	A + Q	A + B	Q	B	A	D + A	D + Q	D
	R Plus S								
	Cn = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	Cn = L	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	- D - 1
	S Minus R								
	Cn = H	Q - A	B - A	Q	B	A	A - D	Q - D	- D
2	Cn = L	A - Q - 1	A - B - 1	- Q - 1	- B - 1	- A - 1	D - A - 1	D - Q - 1	D - 1
	R Minus S								
	Cn = H	A - Q	A - B	- Q	- B	- A	D - A	D - Q	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \nabla Q$	$A \nabla B$	Q	B	A	$D \nabla A$	$D \nabla Q$	D
7	R EX-NOR S	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

+ = Plus; - = Minus; $\vee$ = OR; $\wedge$ = AND; ∇ = EX-OR.

Source Operands and ALU Functions

There are eight source operand pairs available to the ALU as selected by the ***I 0, I 1*** and ***I 2*** instruction inputs. The ALU can perform eight functions: five logic and three arithmetic. The ***I 3, I 4*** and ***I 5*** instruction inputs control this function selection. The carry input, ***Cn***, also affects the ALU results when in the arithmetic mode. The ***Cn*** input has no effect in the logic mode. When ***I 0*** through ***I 5*** and ***Cn*** are viewed together, the 'Source Operand and ALU Function Matrix' on the previous page results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task " basis (i.e., add, subtract, AND, OR, etc.). In the arithmetic mode, the carry will have no bearing on the ALU output. The 'ALU Logic Mode Functions' table below defines the various logic operations that the VS29G01 can perform and the 'ALU Arithmetic Mode Functions' table below shows the arithmetic functions of the device. Both carry-in LOW (***Cn*** = 0) and carry-in HIGH (***Cn*** = 1) are defined in these operations.

ALU Logic Mode Functions

OCTAL I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \nabla Q$
6 1		$A \nabla B$
6 5		$D \nabla A$
6 6		$D \nabla Q$
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

ALU Arithmetic Mode Functions

OCTAL I_{543}, I_{210}	Cn = L		Cn = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	- Q - 1	2's Comp. (Negate)	- Q
2 3		- B - 1		- B
2 4		- A - 1		- A
1 7		- D - 1		- D
1 0	Subtract (1's Comp)	Q - A - 1	Subtract (2's Comp)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Logic Functions for G, P, Cn+4, and OVR

The four signals ***G, P, Cn+4,*** and ***OVR*** indicate carry and overflow conditions when the VS29G01 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to the ALU Source Operand Control table on page 5-4.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	***Function***	***P***	***G***	***Cn+4***	***OVR***
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \nabla C_4$
1	S - R	← Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R - S	← Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0+C_n}$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S, but substitute $\overline{R}_i$ for R_i in definitions →		
6	R ∇ S	← Same as $\overline{R \nabla S}$ equations, but substitute $\overline{R}_i$ for R_i in definitions →			
7	$\overline{R \nabla S}$	$G_3+G_2+G_1+G_0$	$G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1(G_0+\overline{C}_n)}$	See Note

Note: $[\overline{P}_2+\overline{G}_2\overline{P}_1+\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_2\overline{G}_1\overline{G}_0Cn] \nabla [\overline{P}_3+\overline{G}_3\overline{G}_2+\overline{G}_3\overline{G}_2\overline{P}_1+\overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0Cn]$ + = OR

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) .... -3.0 V to +0.5 V
Input Voltage Applied (2), (V_{IN}) .... -2.5 V to +0.5 V
Output Current, I_{OUT}, (DC, output HI) .... 50 mA
Maximum Junction Temperature, (T_j) .... 150°C
Case Temperature Under Bias, (T_c) .... -55° to 125°C
Storage Temperature(3), (T_{STG}) .... -65° to +150°C

Recommended Operating Conditions

Power Supply Voltage (4) - referenced to V_{CC}, (V_{TT}) .... -2.1 V to -1.9 V
Operating Temperature Range (3), (T) .... (Commercial) 0° to 70°C, (Military) -55° to +125°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{IN}) and V_{IN} must be greater than V_{TT} - 0.5 V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.
(4) When using internal ECL 100K reference level.

DC Characteristics *(Over recommended operating conditions with internal V_{REF}. $V_{CC} = V_{CCA}$ = GND, Output load = 50 Ω to -2.0 V.)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-600	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}(1)	Input HIGH current	—	10	—	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min
I_{TT}(2)	Power supply current (from V_{TT})	—	—	800	mA	Inputs LOW Outputs open

Notes: (1) Excluding I/O pins ***(RAM 0, RAM 3, Q 0,*** and ***Q 3)***.
(2) I_{TT} does not include termination currents.

AC Guaranteed Performance Characteristics

The tables below and on page 5-8 specify the guaranteed performance of the VS29G01 over the recommended operating conditions given above (with internal V_{REF}). $V_{CC} = V_{CCA}$ = GND. Package: 52-pin leaded and leadless chip carrier. All data are in ns. Test conditions are outlined on page 5-9.

A. Cycle Time and Clock Characteristics

Parameter	Part Type (Note 1) C, M	C-1
Minimum clock LOW time	9 ns	6 ns
Minimum clock HIGH time	9 ns	6 ns

AC Guaranteed Performance Characteristics *(Continued)*

B. Combinational Propagation Delays (Note 2)

Part Type (Note 1)	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1
	To Output															
From Input	*Y*		*F 3*		*Cn+4*		$\overline{G}, \overline{P}$		$F \neq 0$		*OVR*		*RAM 0, 3*		*Q 0, 3*	
A, B Address	15	10	13	9	13	9	13	9	13	9	13	9	15	10	—	—
D	13	9	12	8	11	7	11	7	12	8	12	8	13	9	—	—
Cn	13	9	12	8	11	7	—	—	12	8	12	8	13	9	—	—
I_{012}	13	9	12	8	11	7	11	7	12	8	12	8	13	9	—	—
I_{345}	13	9	12	8	11	7	11	7	12	8	12	8	13	9	—	—
I_{678}	13	9	—	—	—	—	—	—	—	—	—	—	12	8	12	8
A Bypass ALU (*I = 2XX*)	15	10	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock (L → H)	16	11	15	10	15	10	15	10	15	10	15	10	16	11	15	10
OE	9	6	—	—	—	—	—	—	—	—	—	—	—	—	—	—

C. Set-up and Hold Times Relative to Clock (CP) Input (Note 2)

Input	CP: Set-up Time Before H → L		Hold Time After L → H		Set-up Time Before H → L		Hold Time After L → H	
Part Type (Note 1)	C, M	C-1	C, M	C-1	C, M	C-1	C, M	C-1
A, B Address	7	5	2 (Note 3)	1.5 (Note 3)	$6+CP_{low}$ (Note 4)	$4+CP_{low}$ (Note 4)	2	1.5
B Address	7	5	must not change (Note 5)				2	1.5
D	—	—	—	—	11	7	2	1.5
Cn	—	—	—	—	9	6	2	1.5
I_{012}	—	—	—	—	11	7	2	1.5
I_{345}	—	—	—	—	11	7	2	1.5
I_{678}	9	6	must not change (Note 5)				2.5	2
RAM 0, 3 & Q 0, 3	—	—	—	—	4	3	2.5	2

D. Output Transition Times

Parameter	Description	Min	Typ	Max	Units
t_{TLH}	Output Transition Time (20% to 80%)		1.5		ns
t_{THL}	Output Transition Time (80% to 20%)		1.5		ns

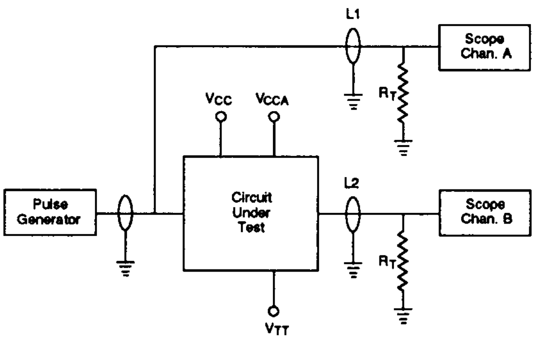
Notes:
1. ***C, M*** *data applies to the standard commercial and military versions, (part numbers: VS29G01LC, VS29G01FC, VS29G01LM, and VS29G01FM) and* ***C-1*** *applies to the enhanced speed commercial version (part numbers: VS29G01LC-1 and VS29G01FC-1).*
2. *A dash indicates a propagation delay path or set-up time constraint does not exist.*
3. *Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.*
4. *The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.* (CP_{low} *= minimum clock LOW)*
5. *Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "must not change".*

AC Test Conditions

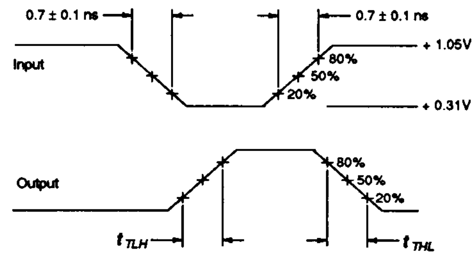
The following conditions apply to the "AC Guaranteed Performance Characteristics" indicated on pages 5-7 and 5-8.

1. V_{CC} = V_{CCA} = +2.0 Volts, V_{TT} = 0 Volts (Power supply voltages are shifted during test for compatibility with measuring devices).
2. 0.1µF decoupling capacitor is connected between ground and V_{CC}.
3. L1 = L2 = equal length 50Ω impedance lines.
4. R_T = 50Ω terminator.
5. C_L = fixture and stray capacitance of ≤ 3pF.

AC Test Circuit

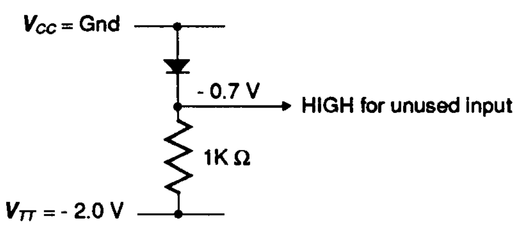


Transition Times



Application Notes

1. Unused inputs (except V_{REF}) must be forced to logic LOW or HIGH, depending on the application.
   - Unused inputs may be forced to logic LOW by tying them to - 2.0V.
   - Unused inputs may be forced to logic HIGH by the following arrangement:



2. The outputs are unterminated source followers and can be in one of two states: HIGH or high-impedance. The high-impedance (cut-off) state corresponds to logic LOW. The logic LOW level can be achieved by an external 50Ω resistor connected to -2.0V or an equivalent network when the output is in the high impedance state.

3. When the Output Enable *(OE)* input is HIGH, the ***Y*** outputs are enabled. When ***OE*** input is LOW, the ***Y*** outputs are electrically OFF (high-impedance). Since the outputs are unterminated source followers, the ***Y*** outputs can be tied with outputs of other devices to form wired-OR nets. Thus, when the ***Y*** outputs are disabled (high-impedance), other devices can access the data lines. An external 50Ω resistor connected to - 2.0V or an equivalent network must be used to provide a LOW at the output when the source follower is OFF.

4. When the internal 100K ECL reference generator is used, $V_{CC}(V_{REF})$ and $V_{TT}(V_{REF})$ must be connected , and the V_{REF} input must be undriven. A capacitor to V_{CC} is recommended.

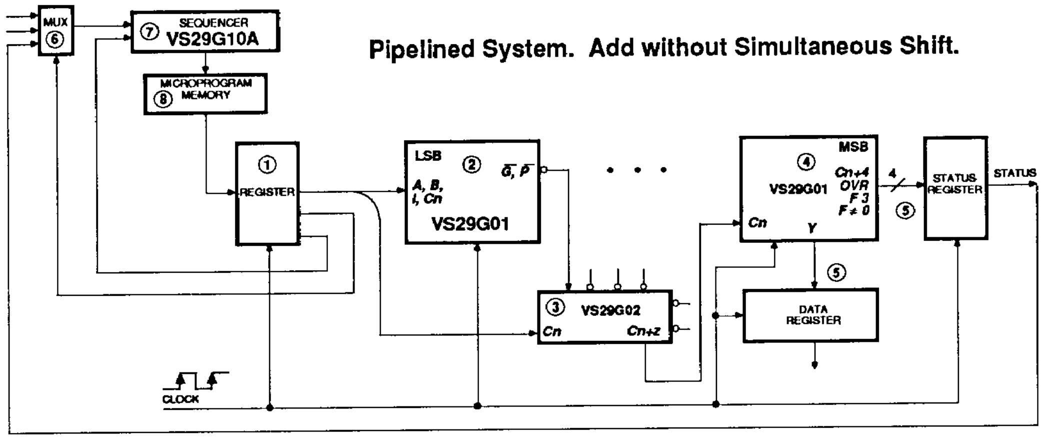
5. When V_{REF} input is used to bring in an ECL reference level like 10K/10KH, then $V_{CC}(V_{REF})$ and $V_{TT}(V_{REF})$ must be disconnected. This will reduce I_{TT} and power dissipation.

6. Note that the heat sink is connected to V_{CC}.

Minimum Cycle Time Calculations for 16-Bit Systems

Speeds used for parts other than VS29G01, VS29G02, and VS29G10A are typical of available 100K ECL parts.

Pipelined System. Add without Simultaneous Shift.

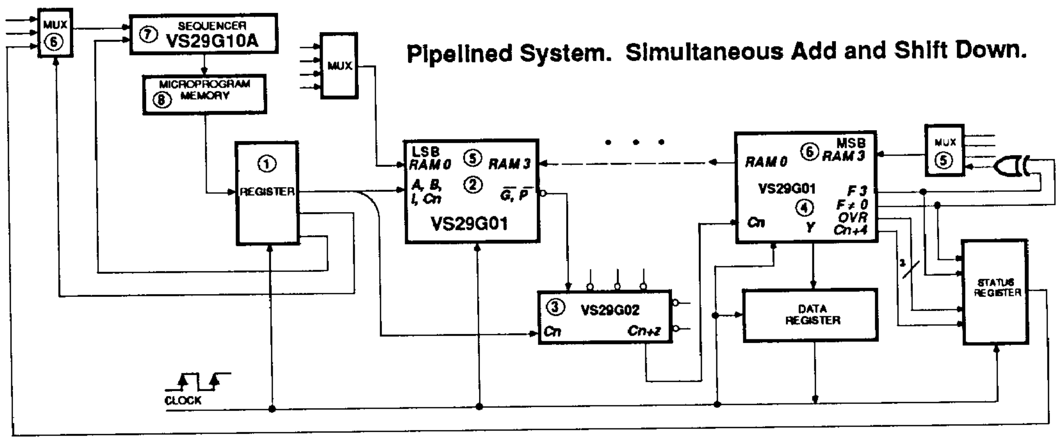


DATA LOOP		
① Register	Clock to Output	2.4 ns
+ ② VS29G01	*A, B* to $\bar{G}$, $\bar{P}$	9.0 ns
+ ③ VS29G02	$\bar{G}_0$, $\bar{P}_0$ to *Cn+z*	5.5 ns
+ ④ VS29G01	*Cn* to *Cn+4, OVR F 3, F ≠ 0, Y*	9.0 ns
+ ⑤ Register	Set-up Time	0.7 ns
		26.6 ns

Notes: 1) Minimum clock period = 27 ns
2) Speeds quoted are for the enhanced speed version of the commercial part

CONTROL LOOP		
① Register	Clock to Output	2.4 ns
+ ⑥ MUX	Select to Output	3.0 ns
+ ⑦ VS29G10A	CC to Output	8.0 ns
+ ⑧ RAM	Access Time	4.5 ns
+ ① Register	Set-up Time	0.7 ns
		18.6 ns

Pipelined System. Simultaneous Add and Shift Down.

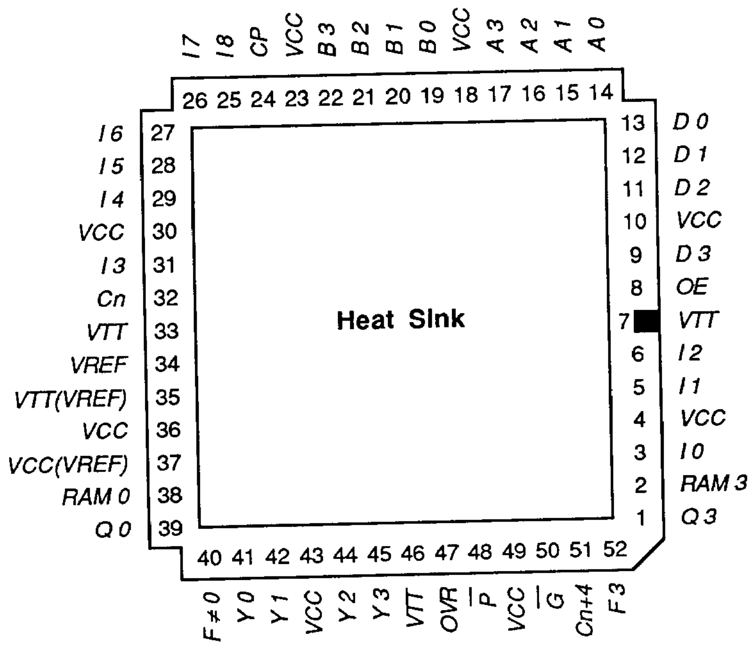


DATA LOOP		
① Register	Clock to Output	2.4 ns
+ ② VS29G01	*A, B* to $\bar{G}$, $\bar{P}$	9.0 ns
+ ③ VS29G02	$\bar{G}_0$, $\bar{P}_0$ to *Cn+z*	5.5 ns
+ ④ VS29G01	*Cn* to *F 3, OVR*	8.0 ns
+ ⑤ XOR & MUX		5.0 ns
+ ⑥ VS29G01	*RAM 3* Set-up	3.0 ns
		32.9 ns

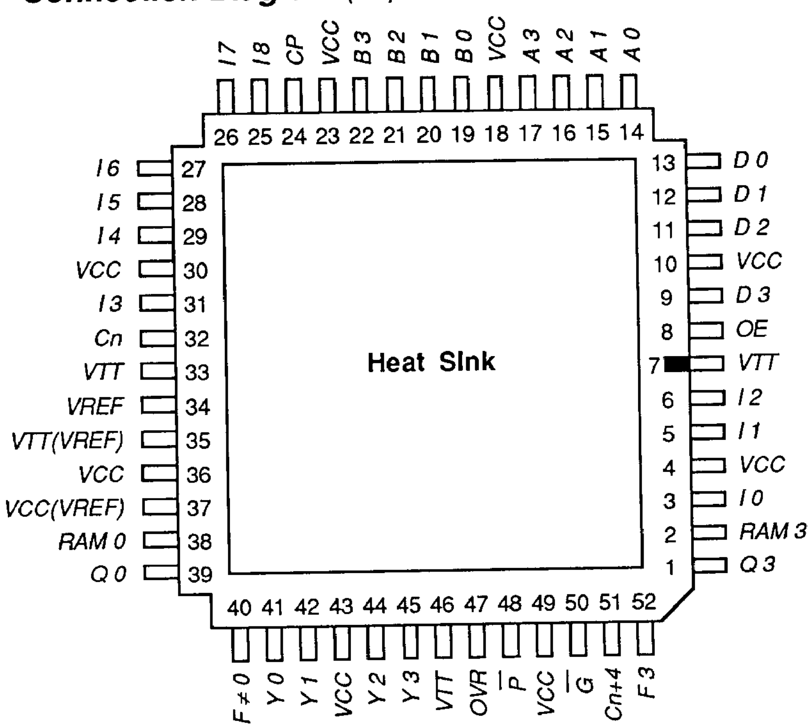
Notes: 1) Minimum clock period = 33 ns
2) Speeds quoted are for the enhanced speed version of the commercial part

CONTROL LOOP		
① Register	Clock to Output	2.4 ns
+ ⑥ MUX	Select to Output	3.0 ns
+ ⑦ VS29G10A	CC to Output	8.0 ns
+ ⑧ RAM	Access Time	4.5 ns
+ ① Register	Set-up Time	0.7 ns
		18.6 ns

Connection Diagram *(52-pin Ceramic Leadless Chip Carrier)*



Connection Diagram *(52-pin Ceramic Leaded Chip Carrier)*



Pin Description

Pin #	Name	I/O	Description
14, 15, 16, 17	***A 0 - A 3***	I	The four address inputs to the register stack used to select one registers' contents which are displayed through the A-port.
19, 20, 21, 22	***B 0 - B 3***	I	The four address inputs to the register stack used to select one registers' contents which are displayed through the B-port and into which new data can be written when the clock goes LOW.
3, 5, 6 25, 26, 27, 28, 29, 30	***I 0 - I 8***	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU *(I 0 - I 2)*, what function the ALU will perform *(I 3 - I 5)*, and what data is to be deposited in the Q-register of the register stack *(I 6 - I 8)*.
1 2	***Q 3*** ***RAM 3***	I/O	A shift line at the MSB of the Q-register *(Q 3)* and the register stack *(RAM 3)*. When the destination code on *I 6, I 7, I 8* indicates an up shift (octal 6 or 7), the outputs are enabled and the MSB of the Q register is available on the *Q 3* pin, and the MSB of the ALU output is available on the *RAM 3* pin. Otherwise, the outputs are electrically OFF (high-impedance), and the pins are electrically ECL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).
38 39	***Q 0*** ***RAM 0***	I/O	Shift lines like *Q 3* and *RAM 3*, but at the LSB of the Q-register and RAM. These pins are tied to the *Q 3* and *RAM 3* pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.
9, 11, 12, 13	***D 0 - D 3***	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. *D 0* is the LSB.
41, 42, 44, 45	***Y 0 - Y 3***	O	The four data outputs. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code *I 6, I 7, I 8)*.
8	***OE***	I	Output enable. When *OE* is LOW, the *Y* outputs are OFF (high-impedance). When *OE* is HIGH the *Y* outputs are enabled.
48, 50	***G, P***	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the VS29G02 for carry look-ahead.
47	***OVR***	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit.
40	***F ≠ 0***	O	This output goes LOW if the data on the four ALU outputs *F 0 - F 3* are all LOW. This indicates the result of an ALU operation is zero.
52	***F 3***	O	The most significant ALU output bit.
32	***Cn***	I	The carry-in of the the internal ALU.
51	***Cn+4***	O	The carry-out of the internal ALU.
24	***CP***	I	The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM, which comprises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.
34	V_{REF}	I	ECL reference level input.
37	$V_{CC}(V_{REF})$		Ground for internal reference generation.
35	$V_{TT}(V_{REF})$		-2.0 V supply for internal reference generation.
4, 10, 18, 23, 30, 36, 43, 49	V_{CC}		Ground connection.
7, 33, 46	V_{TT}		-2.0 V supply connection