SL9999

400MHz ADC DRIVER-AMPLIFIER

The Plessey SL9999 is a monolithic high speed high performance operational amplifier. Although primarily intended to drive the inputs of analog to digital converters, the device is capable of driving any other circuit including those that present a low impedance and high capacitive load. Many other internal features such as programmable open loop gain, programmable output current, internal band gap voltage reference, DC buffer and output DC offset circuitry give the device the flexibility for use in a wide range of applications.

ORDERING INFORMATION

SL9999C **DP** (Commercial Plastic DIL 0° to 70°C)
SL9999B **DG** (Commercial Ceramic DIL -40° to +85°C)
SL9999B **LC** (Commercial LCC -40° to +85°C)
SL9999NA **IC** (Naked Chip)

FEATURES

- Gain-Bandwidth Product 2GHz at 20dB
- Unity Gain-Bandwidth 400MHz
- Slew Rate 1300V/ µs Rising (typ)
- Slew Rate 630/V µs Falling (typ)
- ±50mA Output Current (Programmable)
- Non-saturating
- High Output Drive
- On-chip LF Buffer for Applying DC Offset
- Flexible Supply Range:
  V_{CC} = +8V to +12V
  V_{EE} = -4.5V to -5 5V
- Output Signal Handling (V_{CC} = +12V, V_{EE} = -5.2V)
  V_{out} = 6V p-p (max.)
- Input Signal Handling (V_{CC} = +12V, V_{EE} = -5.2V)
  V_{in} = +2.8V to -2 5V (max.)

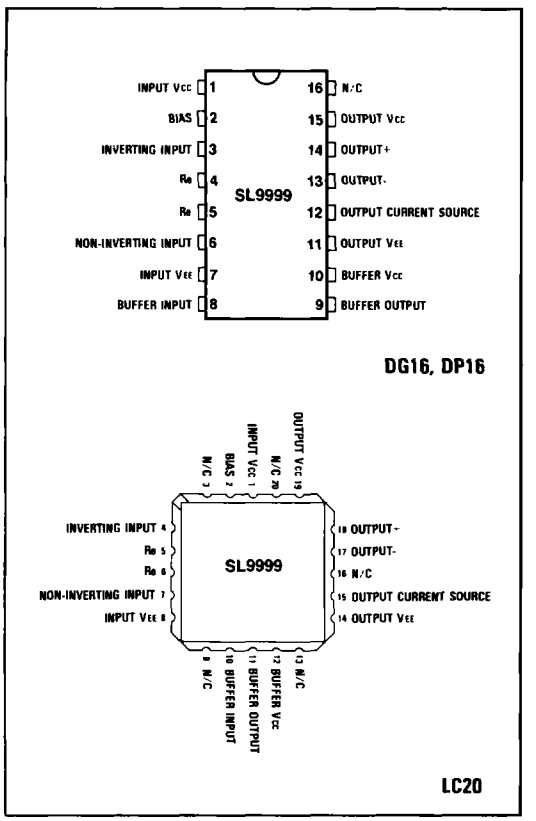


Fig.1 Pin connections - top view

APPLICATIONS

- High Speed Flash ADC Driver
- Wideband, Buffer/Level Shifter
- Wideband IF Amplification
- Video Amplifier/Line Driver
- Fast Settling Pulse Amplifier
- High Speed Op-Amp Applications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})	20V
Input Voltage (Inv I/P to Non-Inv I/P)	±5V
Storage Temperature	-65° C to +175° C
Chip Operating Temperature	+175° C
Operating Temperature: DIL	-40° C to +85° C
Thermal Resistances:	
DG Chip-to-Ambient: DIL	120° C/W
DG Chip-to-Case: DIL	40° C/W
DP Chip-to-Ambient: DIL	100° C/W
DP Chip-to-Case: DIL	40° C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25° C, V_{CC} - +12V, V_{EE} -5V, Test circuit Fig 3.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Equivalent input noise		33		nV/√Hz	50Ω source impedance, BW = 100MHz
Supply current (no load)		35	43	mA	V_{CC} = +12V, V_{EE} = -5V
Gain-bandwidth product		2		GHz	×10 gain
Unity gain bandwidth (small sig)		400		MHz	R_e = 820Ω, R_L = 50Ω
Slew rate RISING	800	1300		V/μs	R_L = 50Ω
Slew rate FALLING	500	630		V/μs	R_L = 50Ω
Settling time		24		ns	To 1% (×10 gain)
Open loop gain		65		dB	50Ω load
Maximum I_{out}			±50	mA	Programmable See Application Notes
Output bias current	15	17	20	mA	Pin 12 O/C
Supply line rejection		40		dB	Referred to input
Supply voltage V_{EE} to V_{CC}	12.5		18	V	
Common mode rejection	55			dB	50Ω load
Input offset (Note 1)		±5	±15	mV	R_e = 100Ω
Input bias current		4.5	18	μA	
Buffer bandwidth		60		MHz	-3dB R_L = 1kΩ (Pulldown resistor)
Buffer output current			15	mA	

NOTE
Input offset is dependent on R_e. For lowest offset R_e = 0 ohms

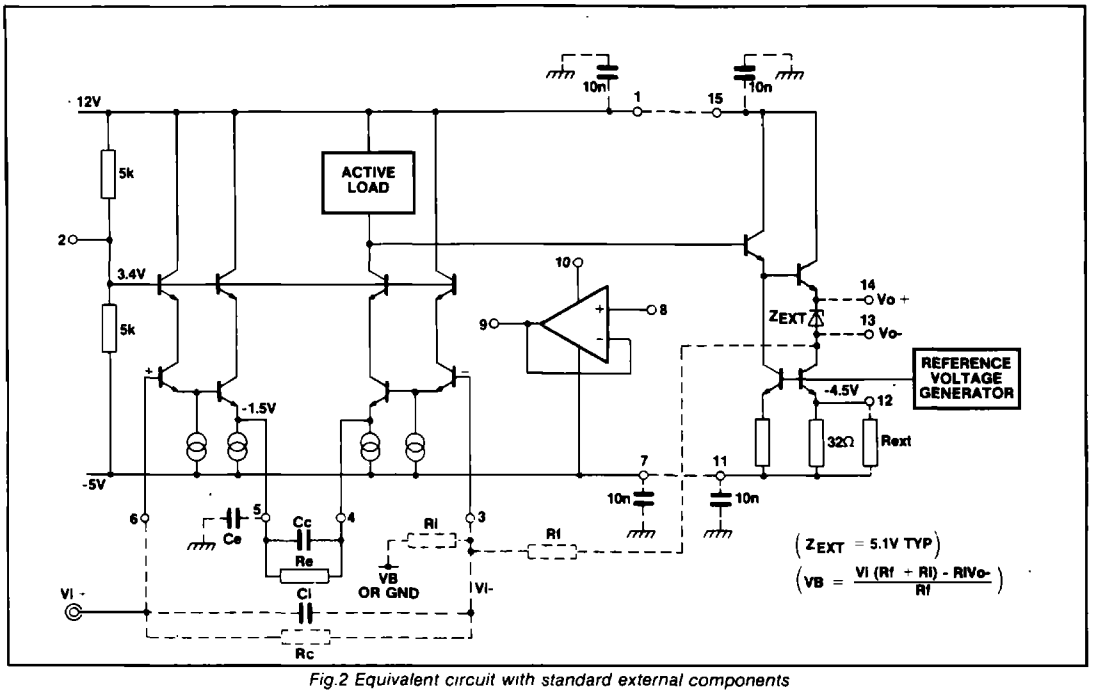


Fig.2 Equivalent circuit with standard external components

APPLICATION NOTES

The SL9999 may be used as a high frequency amplifier in any of the usual op-amp configurations (amplifiers, integrators, etc.).

In most applications, the output of the SL9999 is taken from pin 13 (V_{out-}), DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 (V_{out+}, see Fig.2). Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to V_B.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give a range of DC levels at the output.

Biasing Conditions (25°C)

For undistorted outputs the peak signal voltages on Vo +, Vo- and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geqslant \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leqslant V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geqslant V_{EE} + 1.4V$

D. $Vi+ \text{ and } Vi- \leqslant \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+ \text{ and } Vi- \geqslant V_{EE} + 3.2V$

Bias voltage values at several nodes are indicated on Fig.2.

R_{ext} is connected from pin 12 to pin 11 (V_{EE}) to increase output bias current I_{out}. This current should not exceed 50mA. The value of R_{ext} is calculated as follows:

$$R_{ext} \cong \left[\frac{500}{I_{out} - 16}\right] \Omega$$

where I_{out} is in mA.

The on-chip LF buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. Also it is important to keep stray capacitance at the summing junction to an absolute minimum.

A ground plane should be used to minimise any earth induced currents between the input and output circuits.

The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be close to the device supply pins. We also recommend electrolytic capacitors in parallel with Ceramic for supply decoupling.

Locate the signal source and load close to the circuit with proper termination - for 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition.

Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor (R_e) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain decreases the value of R_e should be increased.

A graph of recommended R_e with gain is given in Fig.4.

Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and to provide DC offset of the output.

For -5V, +12V range a 4.7V to 5.1V Zener may be used.

For lower cost applications a bypassed resistor can conveniently replace the Zener diode. Its value may be calculated from the voltage drop and current through the output stage. For example, for 15mA output current a 330Ω resistor could be used.

Although some power is dissipated in the external Zener, a heatsink on the SL9999 will be necessary if power >800mW is to be dissipated.

Bandwidth Compensation

Bandwidth at higher gains can be improved by a capacitor (C_c) across the degeneration resistor R_e. For example, a non-inverting closed loop gain of 10, 10pF will increase the bandwidth to 280MHz at 50Ω load condition.

A decoupling capacitor (C_e) from pin 5 will compensate the first pole roll-off and hence reduce the noise bandwidth. For a 200MHz bandwidth an 18pF capacitor may be used with the suggested PCB layout on page 6.

A capacitor (C_i) and resistor (R_c) of suitable value between the two inputs will reduce high frequency peaking.

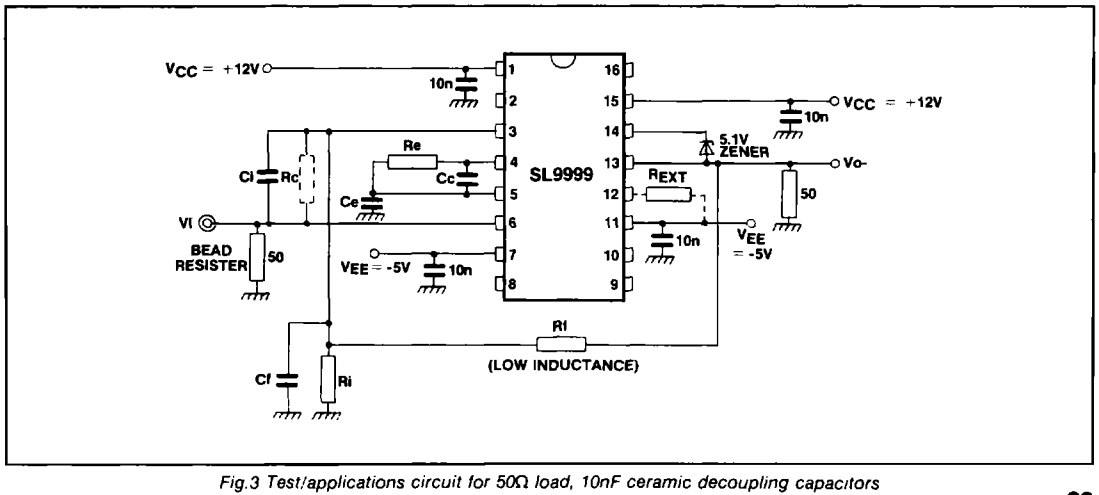


Fig.3 Test/applications circuit for 50Ω load, 10nF ceramic decoupling capacitors

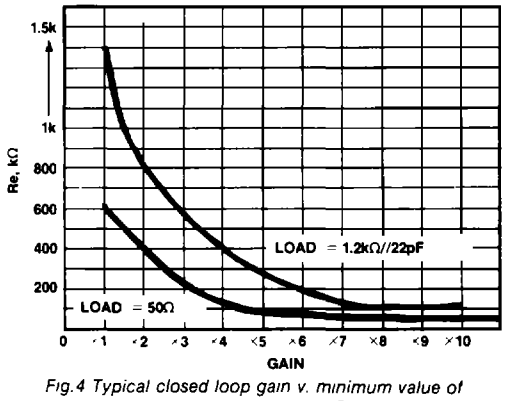


Fig.4 Typical closed loop gain v. minimum value of degeneration resistor R_e

NOTE: Input offset is proportional to R_e value

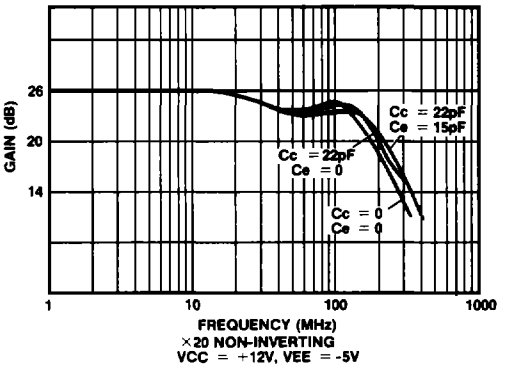


Fig.5 Typical frequency response for the test circuit of Fig.3, ×20 gain, non-inverting, 50Ω load, R_f = 10.6kΩ, R_1 = 560Ω, R_e = 22Ω.

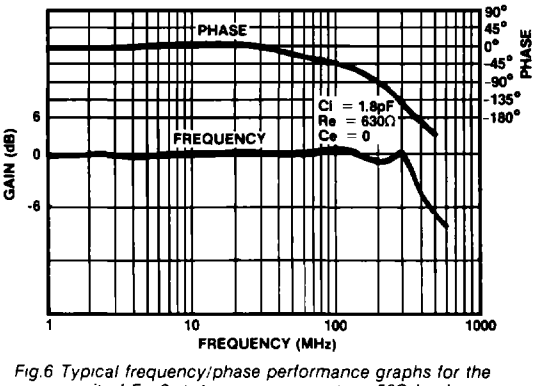


Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.3, ×1 gain, non-inverting, 50Ω load, R_f = 560Ω, R_1 = ∞.

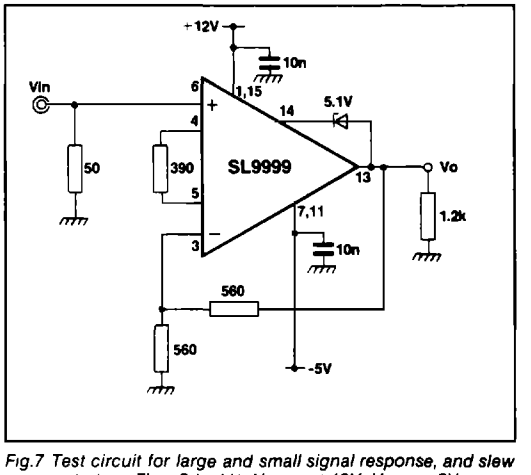


Fig.7 Test circuit for large and small signal response, and slew rate (see Figs. 8 to 11). V_{CC} = +12V, V_{EE} = -5V.

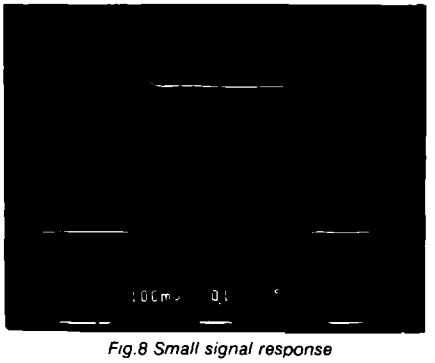


Fig.8 Small signal response

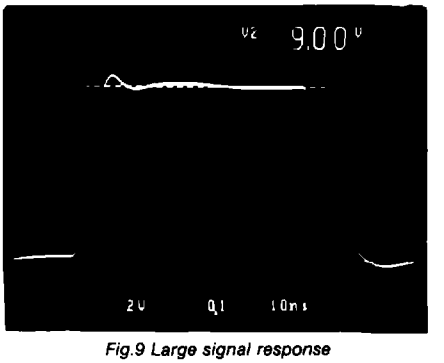


Fig.9 Large signal response

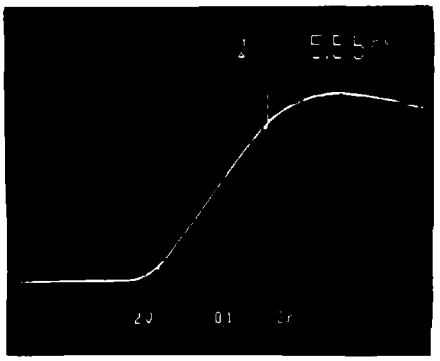


Fig.10 Rising edge 10% to 90% points 1300V/μs

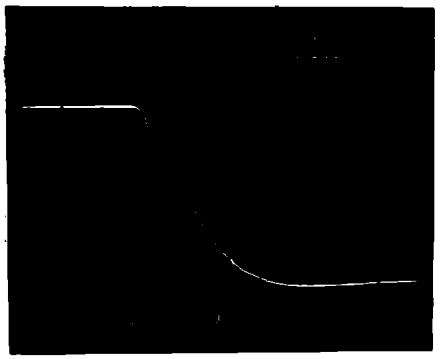


Fig.11 Falling edge 10% to 90% points 630V/μs

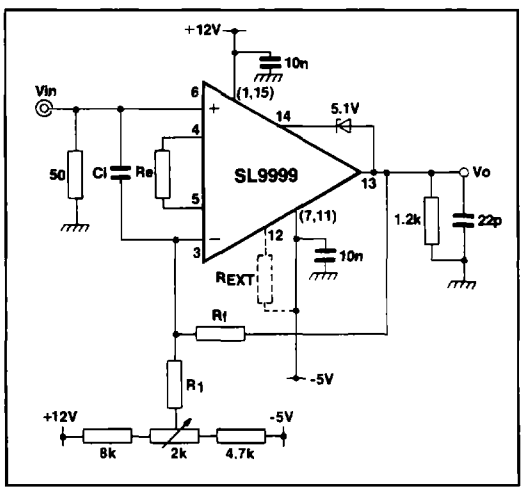


Fig.12 Application circuit for capacitor load e.g. high speed flash ADC input

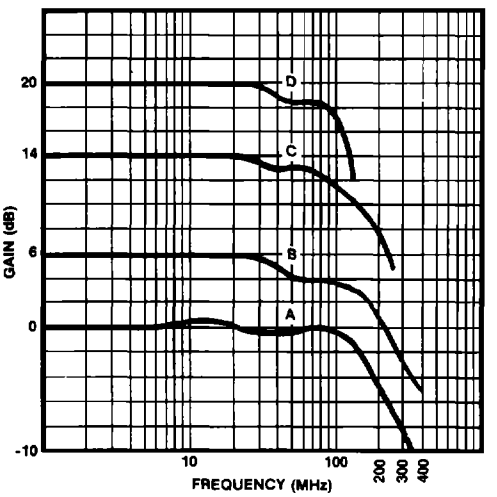


Fig.13 Typical frequency response plots for the circuit of Fig.12 (Load 22pF//1.2kΩ).

TYPICAL APPLICATION

Response (see Fig.13)	Gain	R_f (Ω)	R_i (Ω)	R_e (Ω)	C_f (Pf)	R_{ext} (Ω)	VO/P (p-p)	V_{CC} (V)	V_{EE} (V)
A	×1	2.2k	∞	1.8k	0	∞	1	+12	-5
B	×2	560	560	1.2k	18	50	2	+12	-5
C	×5	2.2k	560	270	10	∞	1	+12	-5
D	×10	5.6k	560	68	0	10	1	+12	-5

Table 1 Recommended components values for the test circuit of Fig.12

NOTE
C_f and C_i are dependent on layout and used to compensate the effects of strays

For applications that require accurate gain flatness over the full frequency range, the inverting mode of operation is recommended. See Fig.14.

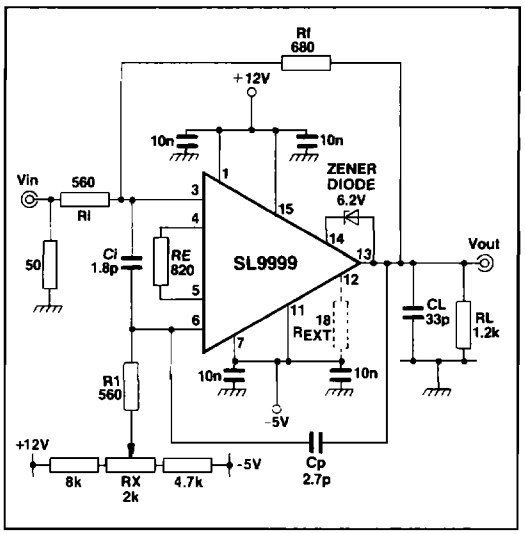


Fig.15 Typical test/applications circuit for inverting mode. Load 33pF/1.2kΩ.

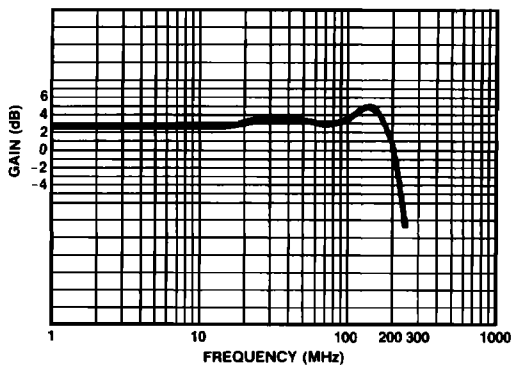
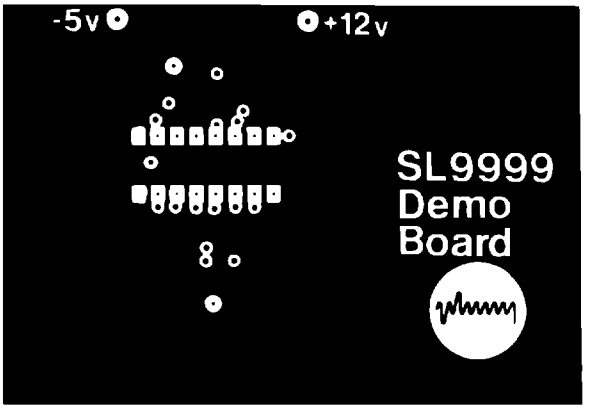
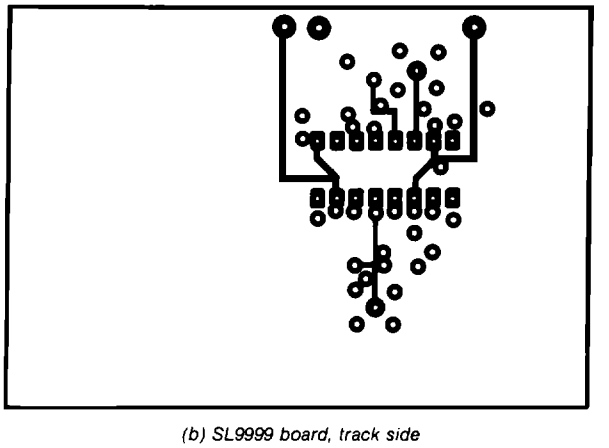


Fig.16 Frequency response of SL9999 with C_L = 33pF, C_P = 2.7pF, R_f = 680, R_L = 1.2k, C_i = 1.8pF, R_I = 560, V_O = 1V p-p (See Test Circuit of Fig.15)

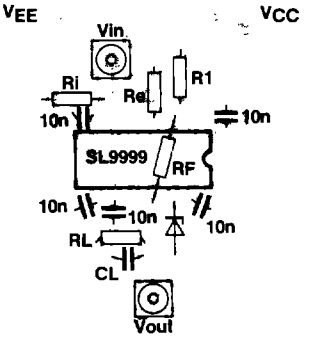
CONSTRUCTION



(a) SL9999 ground plane, component side

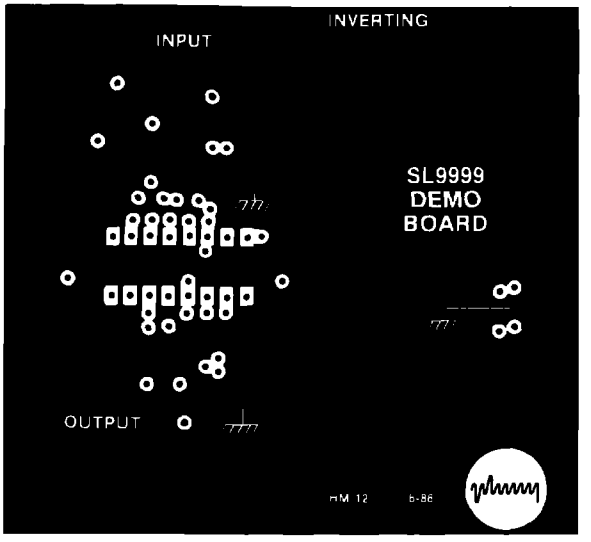


(b) SL9999 board, track side

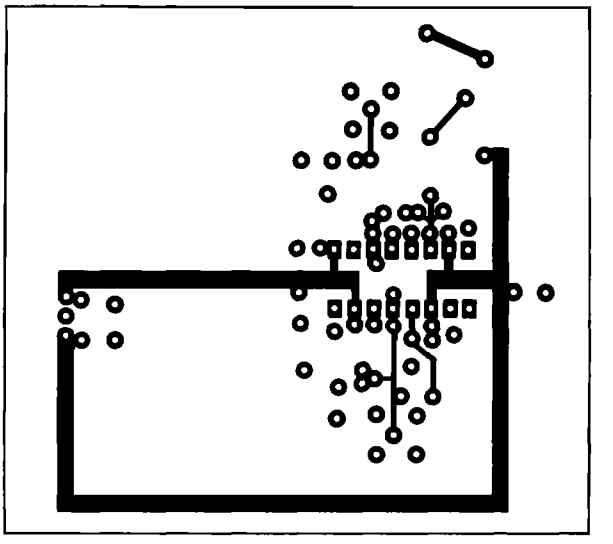


(c) Component location. NOTE: I/P and O/P are sub-vis type 50Ω connectors.

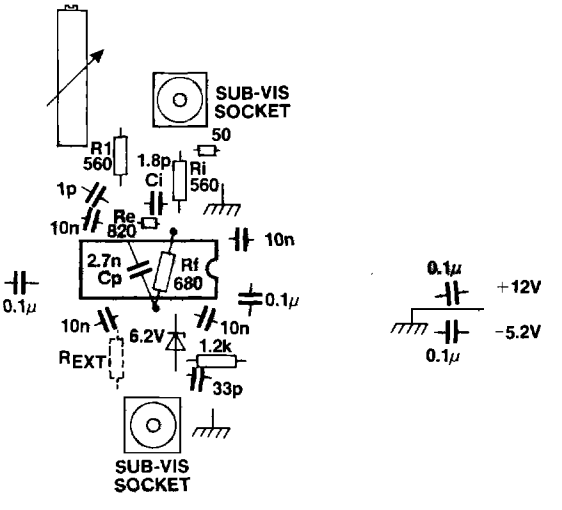
Fig.16 PCB layout for SL9999 demonstration board (Fig.12) viewed from component side and underside



(a) SL9999 ground plane, component side



(b) SL9999 board, track side



(c) Component location (1:1 scale)

Fig.17 PCB layout for SL9999 demonstration board. NOTE: I/P and O/P are sub-vis type 50Ω connectors. R and C are on the track side. Gold socket pins to mount SL9999 for test circuit