

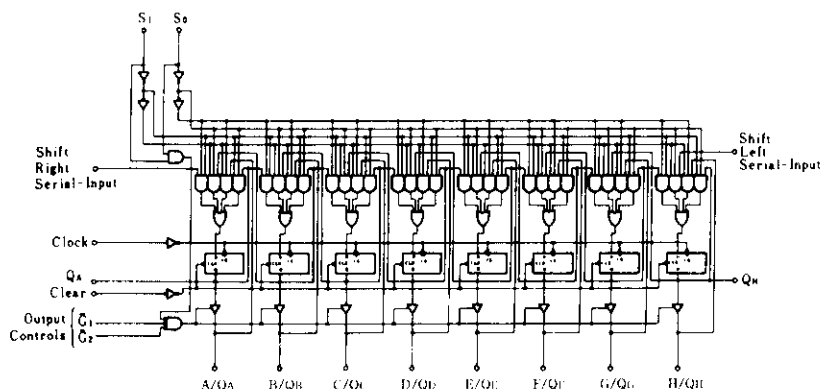
HD74LS299 • 8-bit Universal Shift/Storage Registers (with three-state outputs)

This eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

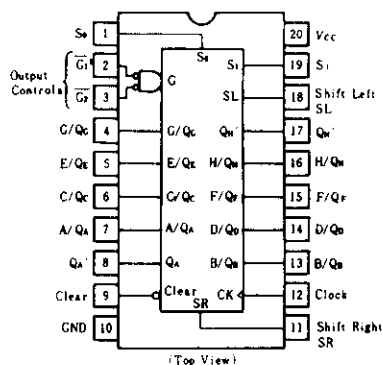
Synchronous parallel loading is accomplished by taking both function select lines, S_0 and S_1 , high. This places the three-

state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	7.0	V
Output voltage (off-state)	$V_{O(off)}$	5.5	V
Operating temperature range	T_{op}	-20 ~ +75	°C
Storage temperature range	T_{stg}	-65 ~ +150	°C

■ FUNCTION TABLE

Mode	Inputs							Inputs/Outputs								Outputs		
	Clear	Function Select		Output Control		Clock	Serial		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H
		S ₁	S ₀	$\overline{G}_1 \uparrow$	$\overline{G}_2 \uparrow$		S _L	S _R										
Clear	L	x	L	L	L	x	x	x	L	L	L	L	L	L	L	L	L	L
	L	L	x	L	L	x	x	x	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	x	x	x	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	x	x	L	L	L	x	x	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	x	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	x	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Cn}
Shift Left	H	H	L	L	L	↑	H	x	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	x	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	x	x	↑	x	x	a	b	c	d	e	f	g	h	a	b

Notes) 1. H; high level, L; low level, X; irrelevant

2. ↑; transition from low to high level

3. a~h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.

4. Q_{A0}~Q_{H0}; the level of Q_A through Q_H, respectively, before the indicated steady-state input conditions were established.

5. Q_{An}~Q_{Hn}; the level of Q_A through Q_H, respectively, before the most-recent ↑ transition of the clock.

6. ↑ =; When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Output current	$Q_A \sim Q_H$	—	—	-2.6	mA
	$Q_A' \text{ or } Q_H'$	—	—	-0.4	
Output current	$Q_A \sim Q_H$	—	—	24	mA
	$Q_A' \text{ or } Q_H'$	—	—	8	
Clock frequency	f_{max}	0	—	25	MHz
Clock pulse width	Clock high	30	—	—	ns
	Clock low	10	—	—	
Clear pulse width	Clear low	20	—	—	ns
Setup time	Select	35 †	—	—	ns
	High-level data	20 †	—	—	
	Low-level data	20 †	—	—	
	Clear inactive-state	20 †	—	—	
Hold time	Select	10 †	—	—	ns
	Data	10 †	—	—	

† The arrow indicates the rising edge.

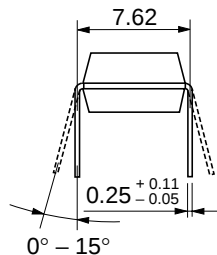
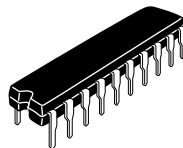
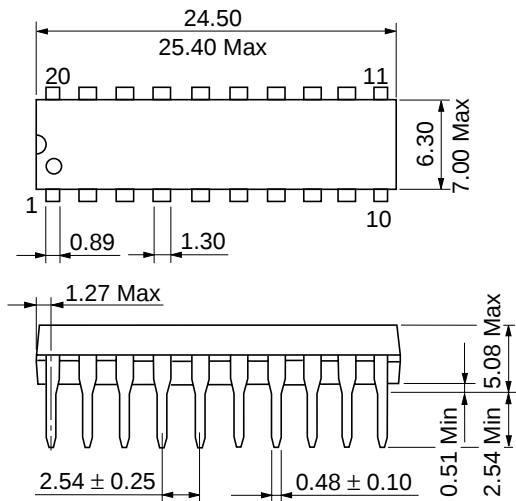
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	$Q_A \text{ thru } Q_H$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OH}=-2.6\text{mA}$	2.4	—	V
	$Q_A' \text{ or } Q_H'$		$I_{OH}=-400\mu\text{A}$	2.7	—	
	$Q_A \text{ thru } Q_H$	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$	$I_{OL}=12\text{mA}$	—	0.4	V
	$Q_A' \text{ or } Q_H'$		$I_{OL}=24\text{mA}$	—	0.5	
Output current	$Q_A \text{ thru } Q_H$	I_{OZH}	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}, V_O=2.7\text{V}$	—	—	40 μA
	$Q_A \text{ thru } Q_H$	I_{OZL}	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}, V_O=0.4\text{V}$	—	—	-400 μA
Input current	$S_0, S_1, A \sim H$	I_{IN}	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	40 μA
	Any other			—	—	20 μA
	S_0, S_1	I_{IL}	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.8 mA
	Any other			—	—	-0.4 mA
	S_0, S_1	I_I	$V_{CC}=5.25\text{V}$	$V_I=7\text{V}$	—	0.2 mA
	$A \sim H$			$V_I=5.5\text{V}$	—	0.1 mA
	Any other			$V_I=7\text{V}$	—	0.1 mA
Short-circuit output current	$Q_A \text{ thru } Q_H$	I_{OS}	$V_{CC}=5.25\text{V}$	-30	—	-130 mA
	$Q_A' \text{ or } Q_H'$			-20	—	-100 mA
Supply current	I_{CC}	$V_{CC}=5.25\text{V}$	—	33	53	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V

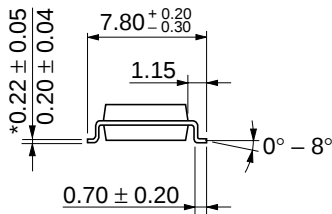
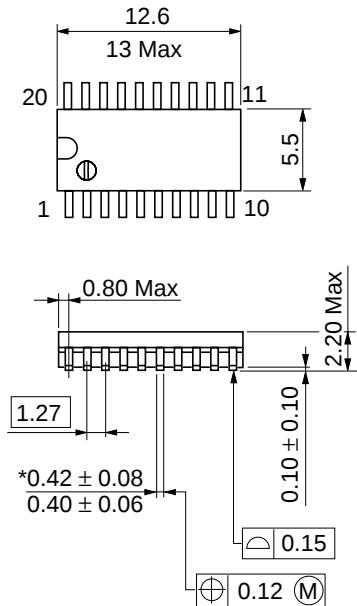
* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15\text{pF}, R_L=2\text{k}\Omega$	25	35	—	MHz
Propagation delay time	t_{PLH}	Clock	Q_A' or Q_H'		—	22	33	ns
	t_{PHL}				—	26	39	
	t_{PNL}	Clear	Q_A' or Q_H'		—	27	40	ns
	t_{PLH}			Clock	$Q_A \sim Q_H$	—	17	
	t_{PHL}	—	26			39		
	Output enable time	t_{ZH}	$\overline{G}_1, \overline{G}_2$	$Q_A \sim Q_H$	$C_L=45\text{pF}, R_L=665\Omega$	—	26	
t_{ZL}		—				13	21	ns
Output disable time	t_{HZ}	$\overline{G}_1, \overline{G}_2$	$Q_A \sim Q_H$	—		19	30	ns
	t_{LZ}			—		10	15	ns
				—	10	15	ns	



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

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