NOVEMBER 1983 — REVISED NOVEMBER 1985

- **65,536 X 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **22-Pin Single-In-Line Package (SIP)**
- **Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier**
- **Long Refresh Period . . . 4 ms (256 cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

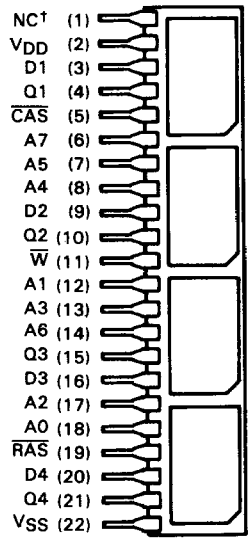
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TM4164EC4-12	120 ns	75 ns	230 ns	260 ns
TM4164EC4-15	150 ns	90 ns	260 ns	285 ns
TM4164EC4-20	200 ns	135 ns	326 ns	345 ns

- **Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines with an "Early Write" Feature**
- **Low Power Dissipation:**

	OPERATING (TYP)	STANDBY (TYP)
TM4164EC4-12	800 mW	70 mW
TM4164EC4-15	700 mW	70 mW
TM4164EC4-20	540 mW	70 mW

- **Operating Free-Air Temperature . . . 0°C to 70°C**
- **Upward Compatible with 256K X 4 Single-In-Line Package**

SINGLE-IN-LINE PACKAGE
(TOP VIEW)



†Reserved for A8 on TM4256EC4

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D1-D4	Data Inputs
NC	No Connection
Q1-Q4	Data Outputs
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164EC4 is a 256K, dynamic random-access memory module organized as 65,536 × 4 bits in a 22-pin single-in-line package comprising four TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with four 0.1 μF decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164EC4 has a density of six devices per square inch (approximately 2.4X the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164EC4 is rated for operation from 0°C to 70°C.

upward compatibility

Future 256K × 4 memory modules in single-in-line packages will have identical pin functions and spacing, and will be directly upward compatible. Pin 1 of the TM4256EC4 (256K X 4 SIP) module will be memory address A8.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the four chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, the data-outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D1-D4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q1-Q4)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns them to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single module, the row address and $\overline{RAS}$ are applied to multiple modules. $\overline{CAS}$ is then decoded to select the proper module.

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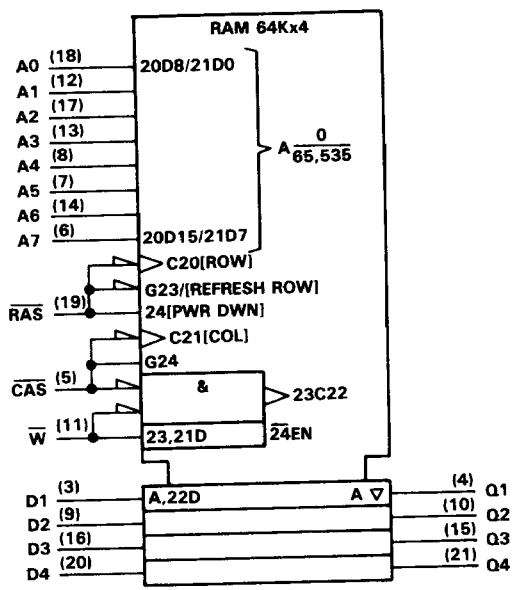
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

single-in-line package and components

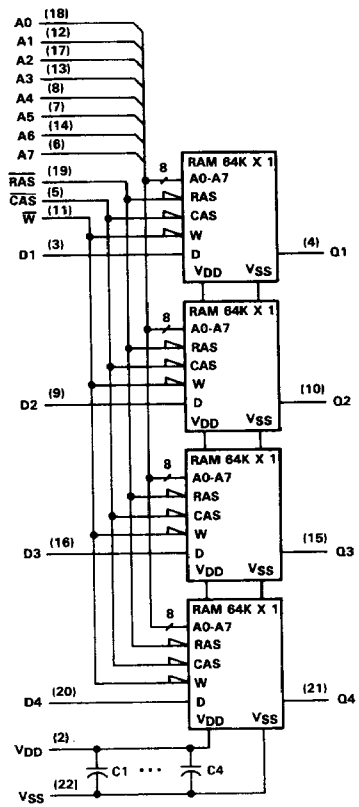
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 2 and 3)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EC4-12			TM4164EC4-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		160	192		140	180	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open,		14	20		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		112	160		100	148	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		112	160		100	148	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164EC4-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		108	148	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		14	20	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		80	128	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		80	128	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	20	pF
$C_{i(D)}$	Input capacitance, data input	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	32	pF
$C_{i(W)}$	Input capacitance, write enable input	32	pF
C_o	Output capacitance	6	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EC4-12		TM4164EC4-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164EC4-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164EC4-12		TM4164EC4-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	5	50	5	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		105		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		100		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		50		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	50		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	45	30	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164EC4-20 MIN	TM4164EC4-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	125		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	60		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	35	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycles times assume t_t = 5 ns.

‡Page mode only.

§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

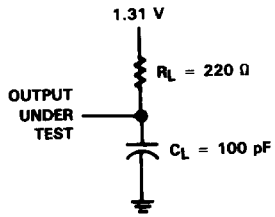
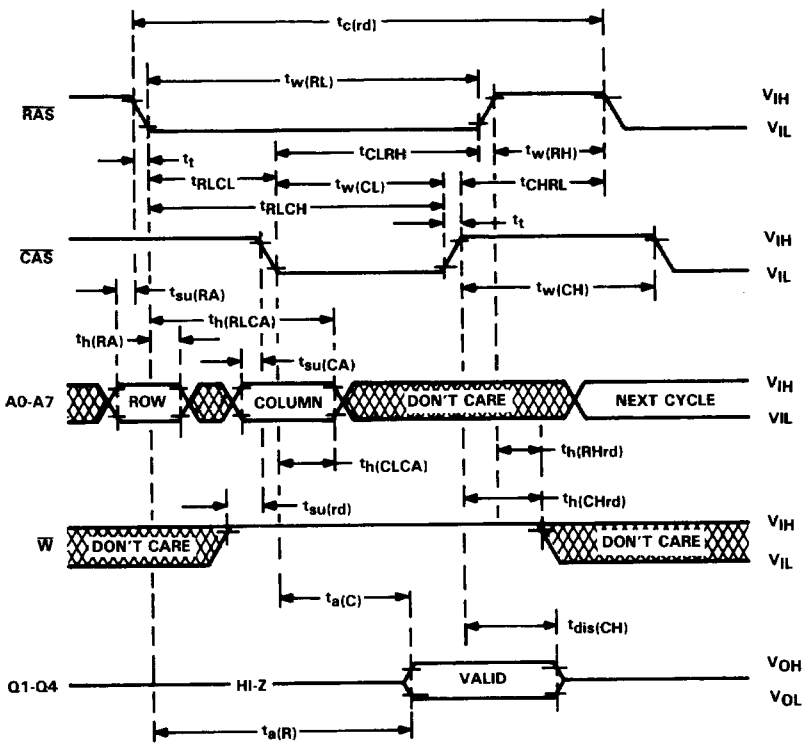
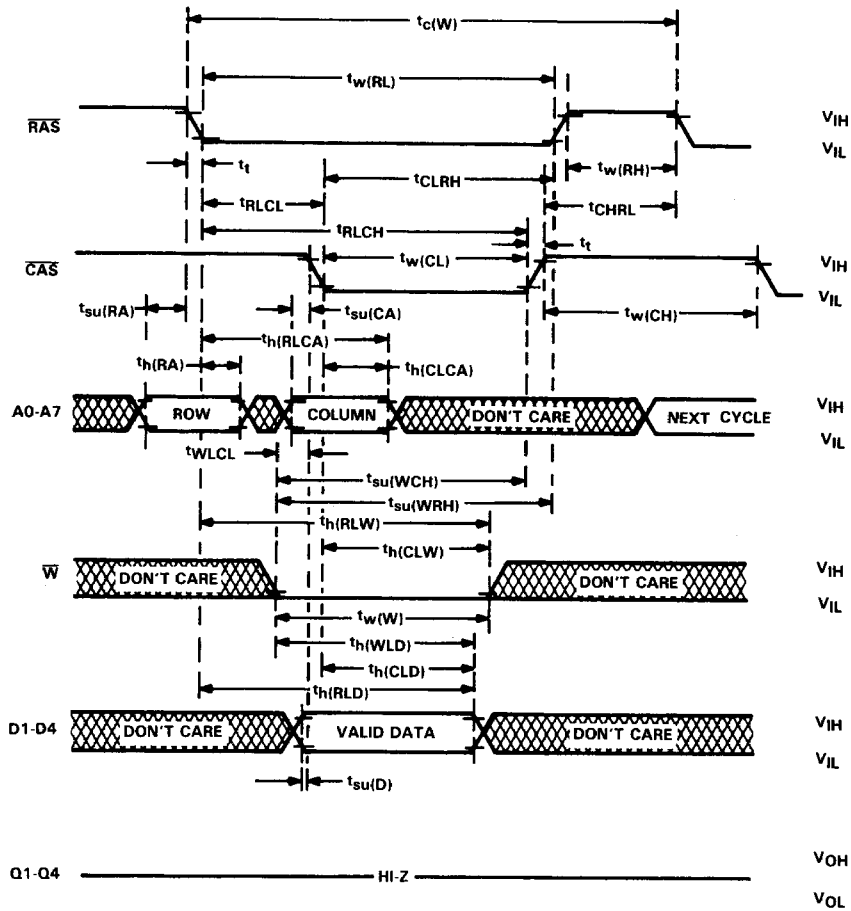


FIGURE 1. LOAD CIRCUIT

read cycle timing



early write cycle timing



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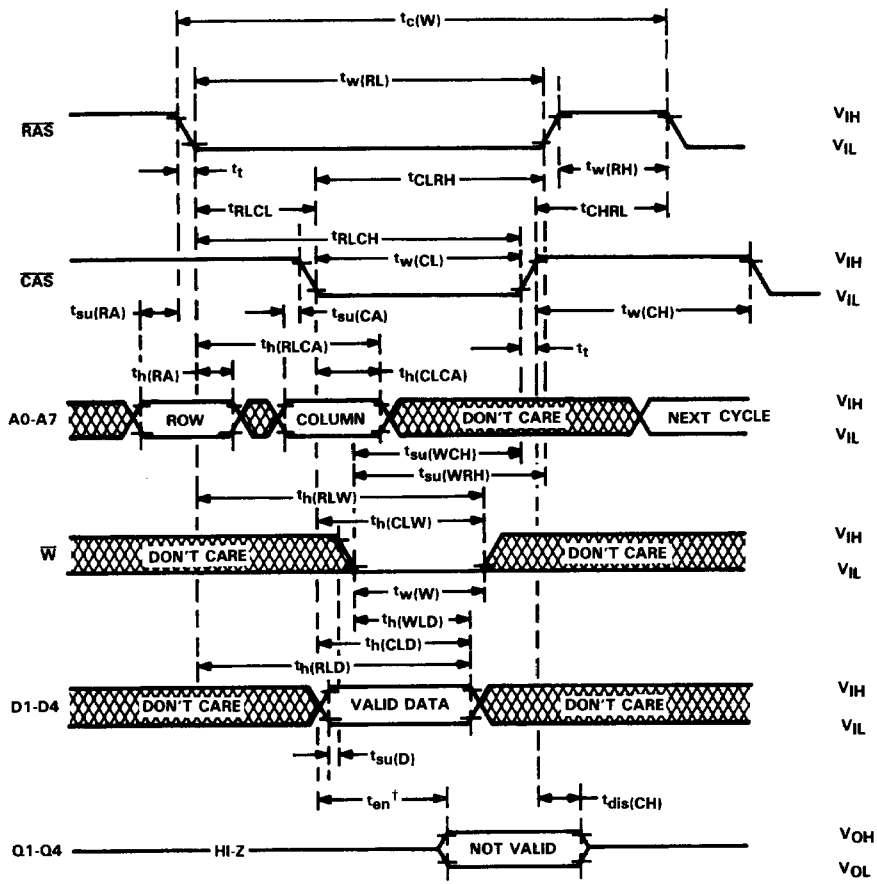
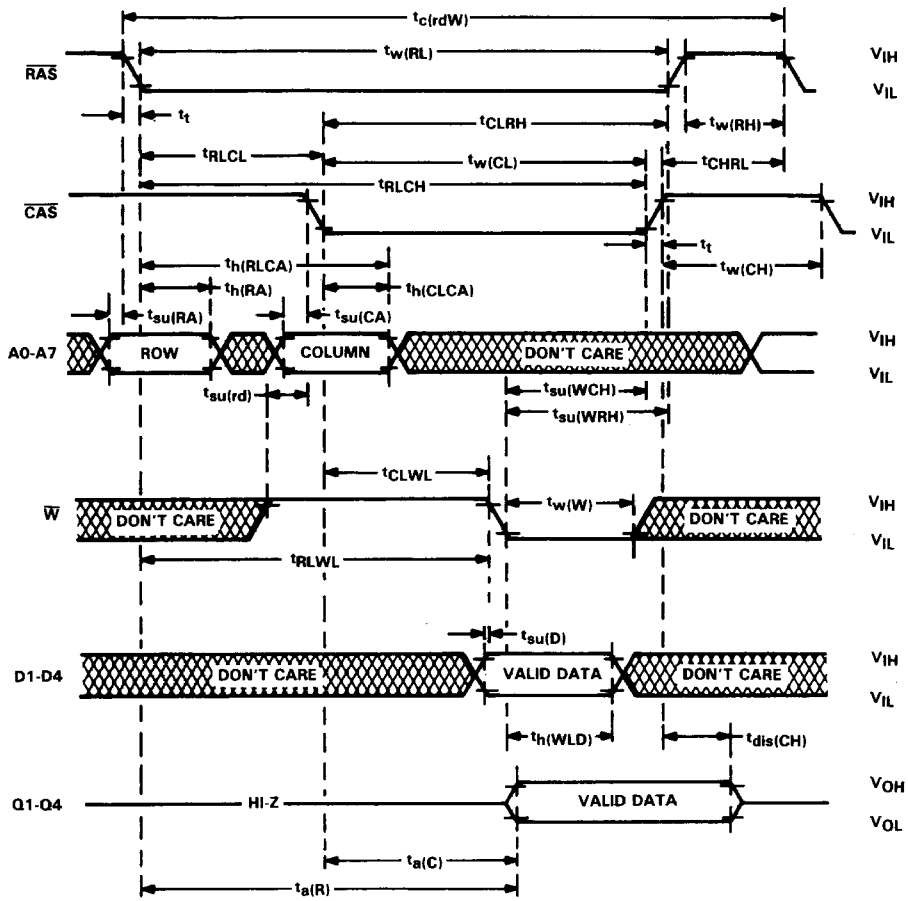
write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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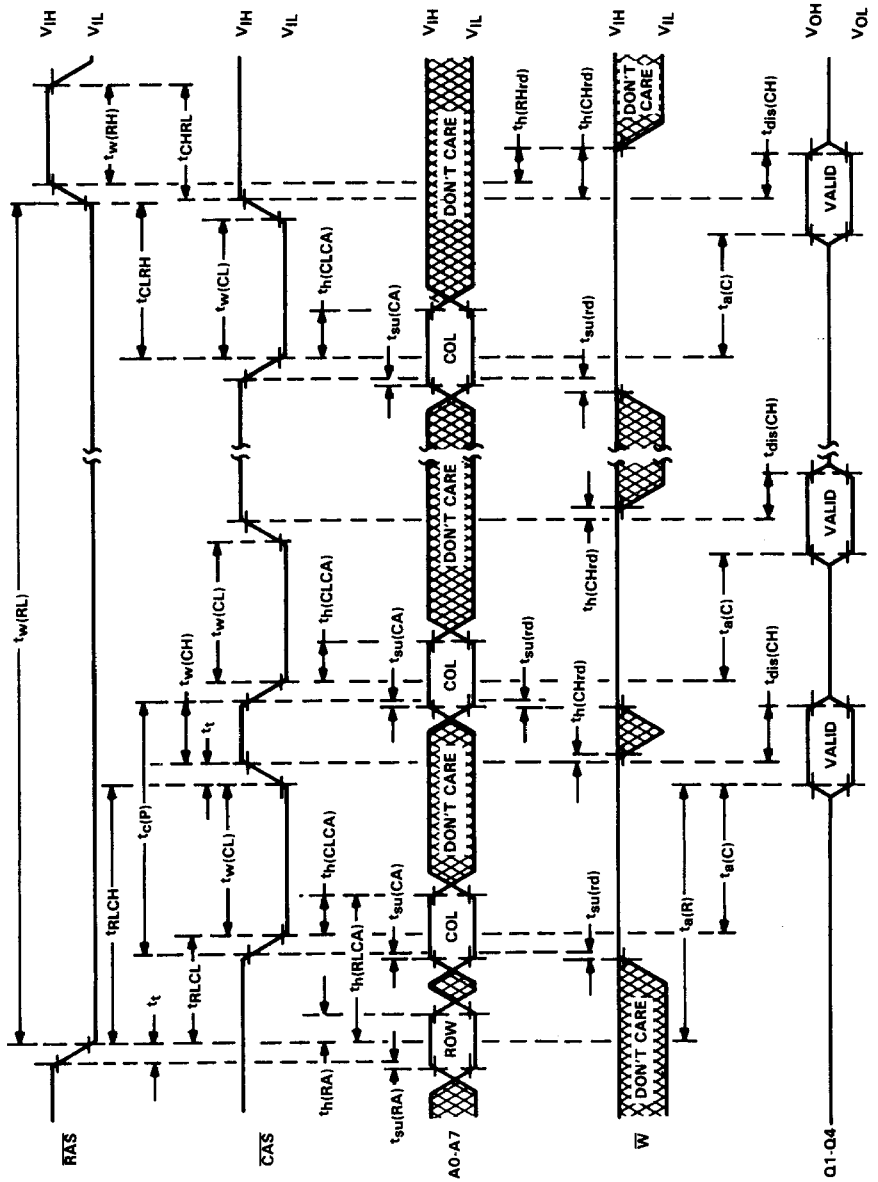
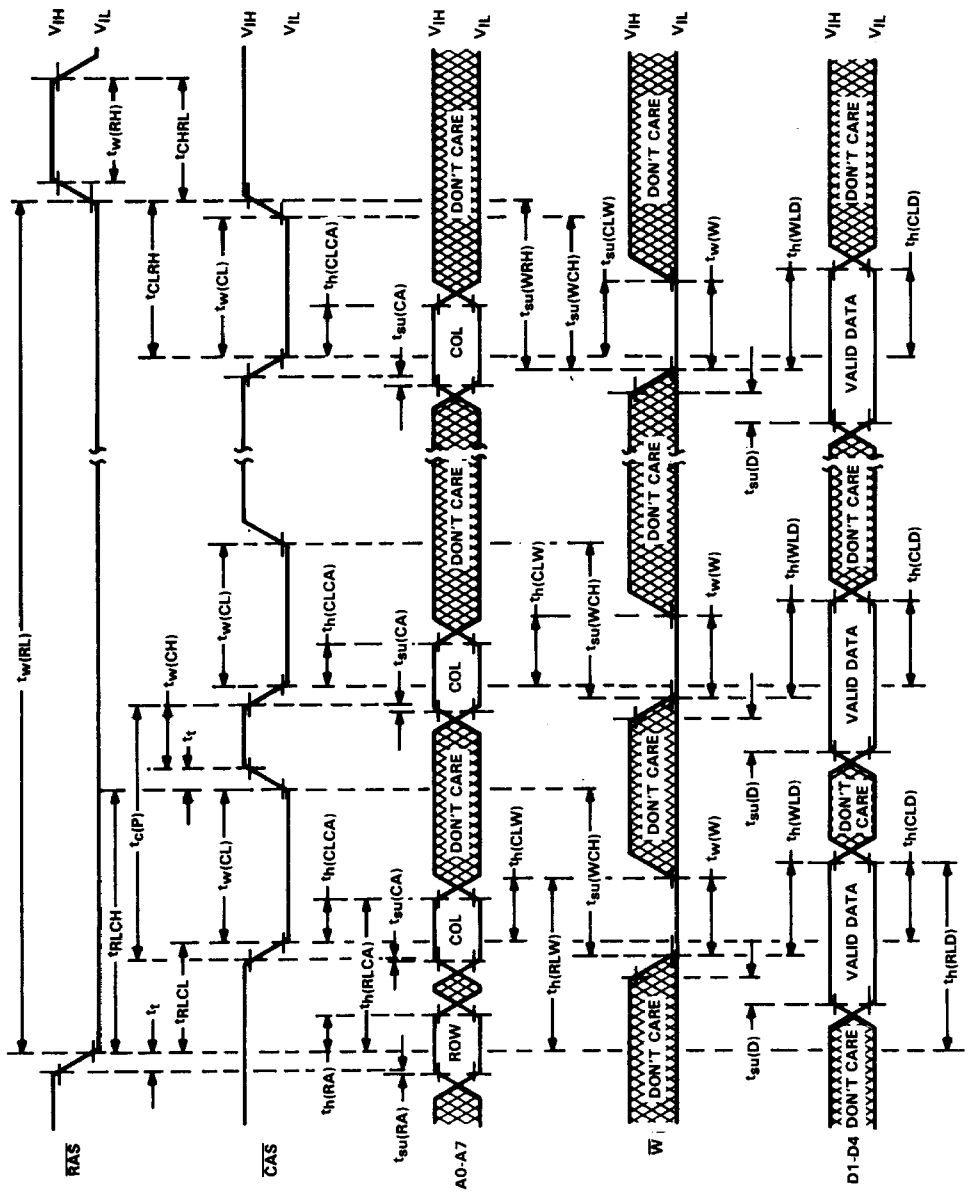
page-mode read cycle timing



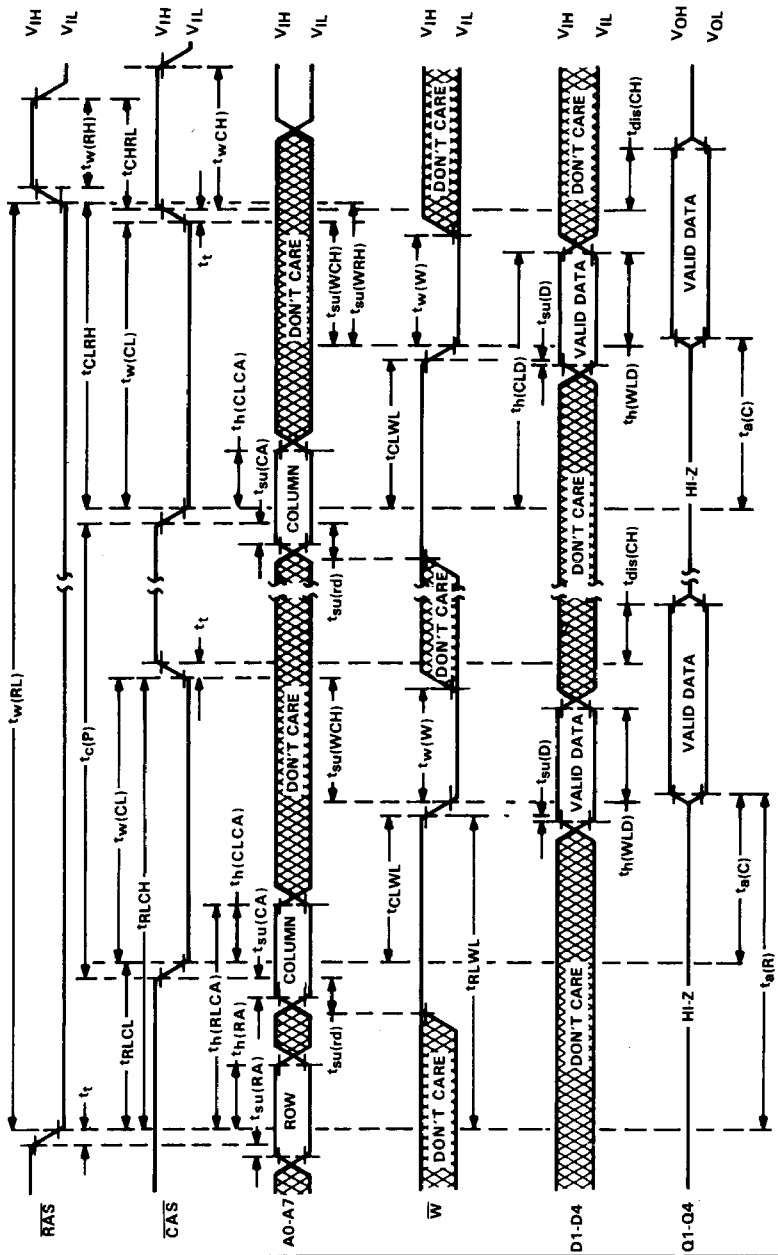
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and ready-modify-write timing specifications are not violated.

page-mode write cycle timing



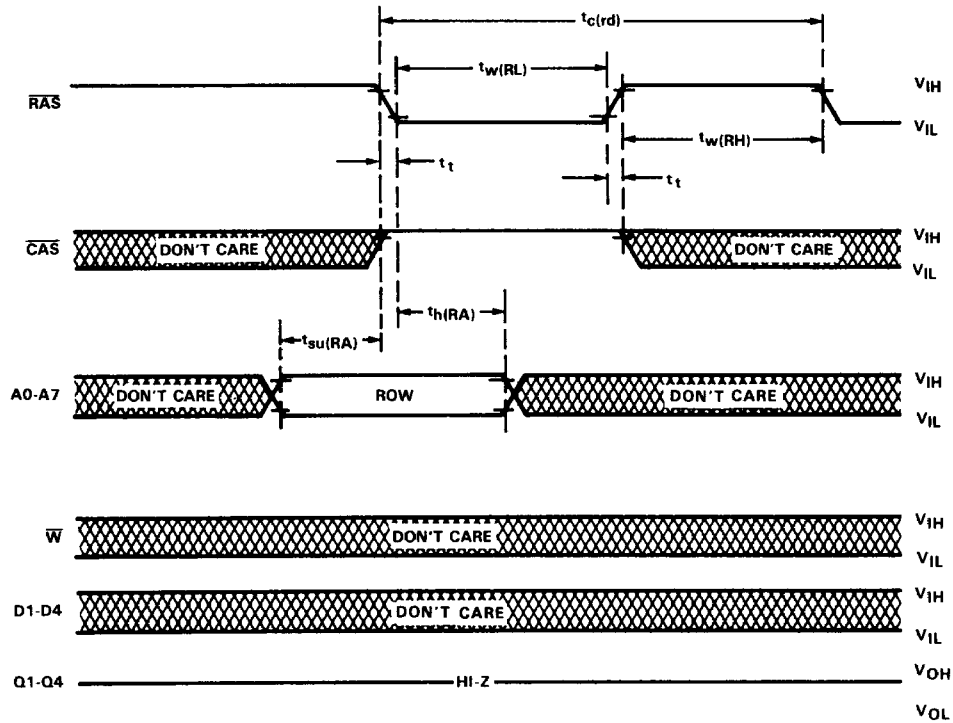
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

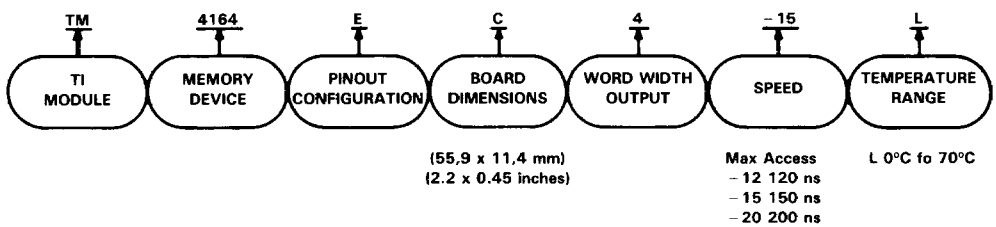


NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



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