HD74HC4017 ● Decade Counter/Divider

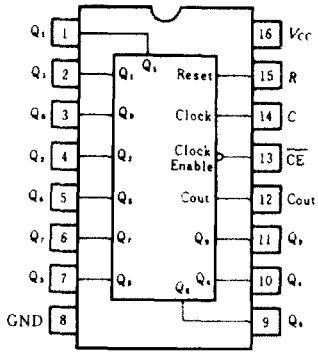
The HD74HC4017 is a 5-stage divide-by-10 Johnson counter with ten decoded outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson decade counter configuration.

The ten decoded outputs are normally low and go high only at their respective decimal time periods. A high signal on Reset R asynchronously clears the decade counter and sets the carry output and Y_0 high. With $\overline{CE}$ low, the count is advanced on a low-to high transition at C input. Alternatively, if C is high, the count is advanced on a high-to-low transition at $\overline{CE}$. Each decoded output remains high for one full clock cycle. The carry output is high while Q_0, Q_1, Q_2, Q_3 or Q_4 is high, then is low while Q_5, Q_6, Q_7, Q_8 or Q_9 is high.

■ FEATURES

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

C	CE	R	Decode Output = n
L	×	L	n
×	H	L	n
×	×	H	Q_0
↗	L	L	n + 1
↘	×	L	n
×	↗	L	n
H	↘	L	n + 1

Notes) 1. × : Don't Care.
2. If n < 5 Carry = "H", Otherwise = "L"

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta = 25°C min	Ta = 25°C typ	Ta = 25°C max	Ta = −40~+85°C min	Ta = −40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in} = V_{IH} or V_{IL}	I_{OH} = −20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH} = −4mA	4.18	—	—	4.13	—	
		6.0		I_{OH} = −5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in} = V_{IH} or V_{IL}	I_{OL} = 20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL} = 4mA	—	—	0.26	—	0.33	
		6.0		I_{OL} = 5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in} = V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in} = V_{CC} or GND, I_{out} = 0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C			Ta=−40~+85°C		Unit
				min.	typ.	max.	min.	max.	
Maximum Clock Frequency	f_{max}	2.0		—	—	6	—	5	MHz
		4.5		—	—	31	—	27	
		6.0		—	—	36	—	31	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	C to Q	—	—	230	—	290	ns
		4.5		—	20	46	—	58	
		6.0		—	—	39	—	49	
	t_{PLH} t_{PHL}	2.0	C to Cout	—	—	230	—	290	ns
		4.5		—	19	46	—	58	
		6.0		—	—	39	—	49	
	t_{PLH} t_{PHL}	2.0	$\overline{CE}$ to Q	—	—	250	—	315	ns
		4.5		—	21	50	—	63	
		6.0		—	—	43	—	54	
	t_{PLH} t_{PHL}	2.0	$\overline{CE}$ to Cout	—	—	250	—	315	ns
		4.5		—	20	50	—	63	
		6.0		—	—	43	—	54	
	t_{PLH} t_{PHL}	2.0	R to Q	—	—	230	—	290	ns
		4.5		—	18	46	—	58	
		6.0		—	—	39	—	49	
	t_{PLH}	2.0	R to Cout	—	—	230	—	290	ns
		4.5		—	13	46	—	58	
		6.0		—	—	39	—	49	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	5	—	20	—	
		6.0		14	—	—	17	—	
Setup Time	t_{su}	2.0		75	—	—	95	—	ns
		4.5		15	5	—	19	—	
		6.0		13	—	—	16	—	
Hold Time	t_h	2.0		50	—	—	65	—	ns
		4.5		10	4	—	13	—	
		6.0		9	—	—	11	—	
Removal Time	t_{rem}	2.0		100	—	—	125	—	ns
		4.5		20	−3	—	25	—	
		6.0		17	—	—	21	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	6	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF