

Two Stage Power Factor Converter

FEATURES

- Single Chip Solution for Power Factor Corrected Power Systems
- Worldwide Operation Without Switches
- Fixed Frequency PWM Drive for Both Pre- and Post- Regulators
- Low Offset Analog Multiplier/Divider
- 5 MHz, Low Offset Current Amplifier
- Trimmed $\pm 6\%$ Oscillator Frequency
- Over Voltage Fault Comparator
- Low I_{cc} Startup Current, 650 μ A Typical
- Trimmed $\pm 1\%$ 7.5V Reference
- Independent Maximum Multiplier Output Current Clamp
- 15/10V, 11/10V UVLO Thresholds
- Single-Ended or Double-Ended Post-Regulator Output Configurations
- 1A Totem Pole MOSFET Drivers

DESCRIPTION

The UC1891/2/3/4 family of power supply controller ICs combine an active Power Factor corrected boost pre-regulator with a Voltage mode PWM down converter for post regulation. Line voltage feedforward in the pre-regulator allows the converter to achieve near unity power factor over the full international range of line voltages. The post regulator is configurable for either single-ended or push-pull topologies providing a true single chip solution for PFC power systems.

The boost pre-regulator front end is implemented with line-compensated, average current mode control, for low distortion, continuous input current. Average current mode control accurately maintains sinusoidal line current without the need for slope compensation, unlike peak current mode control. The pre-regulator employs a low offset high bandwidth current amplifier, a separate voltage amplifier, an analog multiplier/divider, 1A totem pole MOSFET driver, and latched overvoltage and overcurrent comparators.

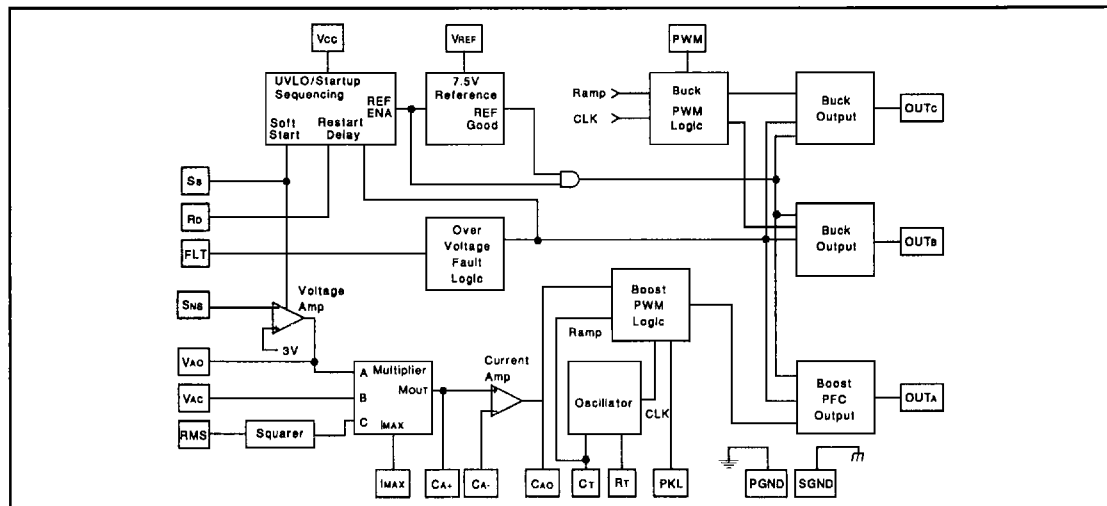
The PWM post-regulator section is configurable as either a single-ended or double-ended controller. A PWM comparator, PWM latch, toggle FF, and Dual 1A totem pole MOSFET drivers are included to realize the desired configurations. Voltage control can be implemented through an optical coupler from an isolated output.

An accurate fixed-frequency oscillator provides synchronization for both controllers. Restart delay and softstart circuits deliver highly predictable startup and fault management for the controllers. Part selectable UVLO thresholds provide the flexibility to start the controller from an auxiliary winding or a separate 12V regulator.

Additional features include low (1mA) startup current, a 1% trimmed 7.5V reference, and an independent multiplier maximum output current clamp.

These devices are available in the 28-pin QP package as well as the 24-pin J and 24-pin N packages.

BLOCK DIAGRAM



PRODUCT SCHEDULE

		Post Regulator Outputs	
		Alternating (Max DC < 50%)	Parallel (Max DC < 100%)
UVLO Thresholds	15V on, 10V off	1891	1893
	11V on, 10V off	1892	1894

CONNECTION DIAGRAM

**DIL-24 (TOP VIEW)
N or J PACKAGE**

OUTb 1, OUTc 2, N/C 3, PWM 4, Rd 5, Ss 6, Sns 7, VAO 8, N/C 9, CT 10, SGND 11, Rt 12, PGND 24, Vcc 23, OUTA 22, VREF 21, PKL 20, CAO 19, FLT 18, RMS 17, CA- 16, VAC 15, CA+ 14, IMAX 13

**PLCC-28 (TOP VIEW)
QP PACKAGE**

4 3 2 1 28 27 26, 5 25, 6 24, 7 23, 8 22, 9 21, 10 20, 11 19, 12 13 14 15 16 17 18

PACKAGE PIN FUNCTIONS

Function	Pin #
IMAX	1
CA+	2
VAC	3
CA-	4
RMS	5
FLT	6
CAO	7
PKL	8
VREF	9
OUTA	10
Vcc	11
PGND	12-18
OUTb	19
OUTc	20
Rd	22
Ss	23
SNS	24
VAO	25
CT	26
SGND	27
Rt	28

ELECTRICAL CHARACTERISTICS: Unless specified Vcc=18V, Rt=15k, CT=1.5nF, RlMAX=15k, PKL=1V, VRMS=1.5V, I VAC=100µA, VCA=0V CAO=3V, VAO=5V, VSNS=3.0V, -55°C < TA < 125°C for the UC189X, -40°C < TA < 85°C for the UC289X, and 0°C < TA < 70°C for the UC389X, TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Off	CAO, VAO = 0V, Vcc = UVLO-0.5V		600	1200	µA
Supply Current, On			25	30	mA
Vcc Turn-on Threshold	1891, 1893		15	16	V
Vcc Turn-off Threshold		9	10		V
Vcc Turn-on Threshold	1892, 1894		11	11.5	V
Vcc Turn-off Threshold		9	10		V
Voltage Amplifier					
Input Voltage	VAOUT = 3.5v	2.9		3.1	V
VSENSE Bias Current		-500	25	500	nA
Open Loop Gain	VAOUT=2 to 6v	70	100		dB
VOUT High	ILOAD = -200µA		5.8		V
VOUT Low	ILOAD = 200µA		0.3	0.5	V
Output Short Circuit Current	VAOUT = 0v		1.5	2.2	mA
Gain Bandwidth Product	FIN=100kHz, 10mV p-p		1		mHz

UC1891/2/3/4
UC2891/2/3/4
UC3891/2/3/4

ELECTRICAL CHARACTERISTICS (cont.):

Unless specified $V_{CC}=18V$, $R_T=15k$, $C_T=1.5nF$, $R_{IMAX}=15k$, $PKL=1V$, $V_{RMS}=1.5V$, $I_{VAC}=100\mu A$, $V_{CA}=0V$, $C_{AO}=3V$, $V_{AO}=5V$, $V_{SNS}=3.0V$, $-55^\circ C < T_A < 125^\circ C$ for the UC189X, $-40^\circ C < T_A < 85^\circ C$ for the UC289X, and $0^\circ C < T_A < 70^\circ C$ for the UC389X, $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amplifier					
Input Offset Voltage		-1		2	mV
Input Bias Current (sense)		-500		500	nA
Gain		80	110		dB
Output Swing	0.5 to 7.5V				
Short Circuit Current	$C_{AOUT} = 0V$		1.5	2	mA
PSRR	$V_{CC} = 12$ to 24V	65	85		dB
Common Mode Range		-0.3		4	V
Gain Bandwidth Product	$f_{IN} = 100$ kHz, 10mV p-p	2	3.5		mHz
Reference					
Output Voltage	$I_{REF} = 0mA$, $T_A = 25^\circ C$	7.425	7.5	7.575	V
	$I_{REF} = 0mA$	7.35	7.5	7.65	V
Load Regulation	$I_{REF} = 1$ to 10mA	-15		15	mV
Line Regulation	$V_{CC} = 15$ to 35V	-10		10	mV
Short Circuit Current	$V_{REF} = 0V$	15	40	70	mA
Oscillator					
Initial Accuracy	$T_A = 25^\circ C$	48		53	kHz
Voltage Stability	$V_{CC} = 12$ to 18V		1		%
Total Variation	Line, Temp	45		55	kHz
Ramp Amplitude (p-p)		4.8		5.6	V
Ramp Valley Voltage		0.8		1.3	V
Fault Management					
Fault Comparator V_{TH}		1.9	2	2.1	V
Fault Comp Input Bias	$V_{FAULT} = 2.5V$		0.3	3	μA
Fault Propagation Delay			250		ns
S_s Charge Current	$V_{SOFTSTART} = 2.5V$	3	10	20	μA
PK Limit Offset Voltage		-10		10	mV
PK Limit Input Current	$V_{PKLIMIT} = -0.1V$	-200	-100		μA
PK Limit Prop. Delay			200		ns
Multiplier					
Output Current - IAC Limited	$I_{AC} = 100\mu A$, $V_{RMS} = 1V$	-220	-200	-180	μA
Output Current - Zero	$I_{AC} = 0\mu A$	-2	-0.2	2	μA
Output Current - R_{MULT} Limited	$I_{AC} = 500\mu A$	-280	-250	-220	μA
Output Current - Power Limited	$I_{AC} = 100\mu A$, $V_{RMS} = 1.5V$, $V_A = 5.6V$	-230	-205	-180	μA
Output Current	$I_{AC} = 100\mu A$, $V_{RMS} = 1.5V$, $V_A = 2V$	-55	-45	-35	μA
Output Current	$I_{AC} = 100\mu A$, $V_{RMS} = 1.5V$, $V_A = 5V$	-215	-180	-145	μA
Output Current	$I_{AC} = 100\mu A$, $V_{RMS} = 5V$, $V_A = 2V$	-20	-4	0	μA
Output Current	$I_{AC} = 100\mu A$, $V_{RMS} = 5V$, $V_A = 5V$	-25	-16	5	μA
Gain Constant	Refer to Note 1		-1		
Gate Drivers A, B, C					
Output High Clamp Voltage	No load, $V_{CC} = 18$ to 35V	14	15	16	V
Output High Voltage	$I_{OUT} = -200mA$, $V_{CC} = 15V$	12	12.8		V
Output Low Voltage	$I_{OUT} = 200mA$	1.6	2.2		V
Output Low (UVLO)	$I_{OUT} = 50mA$, $V_{CC} = 0V$		0.9	1.5	V

UC1891/2/3/4
 UC2891/2/3/4
 UC3891/2/3/4

**ELECTRICAL
 CHARACTERISTICS (cont.):**

Unless specified V_{CC}=18V, R_T=15k, C_T=1.5nF, R_{IMAX}=15k, P_{KL}=1V, V_{RMS}=1.5V,
 I_{VAC}=100μA, V_{CA}=0V C_{AO}=3V, V_{AO}=5V, V_{SNS}=3.0V, -55°C < T_A < 125°C for the
 UC189X, -40°C < T_A < 85°C for the UC289X, and 0°C < T_A < 70°C for the UC389X,
 T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drivers A, B, C (cont.)					
Output RISE/FALL Time	C _{LOAD} = 1nF		35		ns
Output Peak Current	C _{LOAD} = 10nF		1		A
Deadtime (B & C only)	C _T = 1nF		600		ns

Note 1. Gain Constant (k) = $\frac{I_{AC}(V_{AC} - 1V)}{V_{RMS}^2 \times I_{MO}}$

where: I_{MO} = Multiplier Output Current
 1.5V ≤ V_{RMS} ≤ 5.0V
 2.0V ≤ V_{AO} ≤ 5.0V