+1.8V, Low Power, Quad-Input, 16-Bit ∑ – Δ A/D Converter with Power Fault Monitor

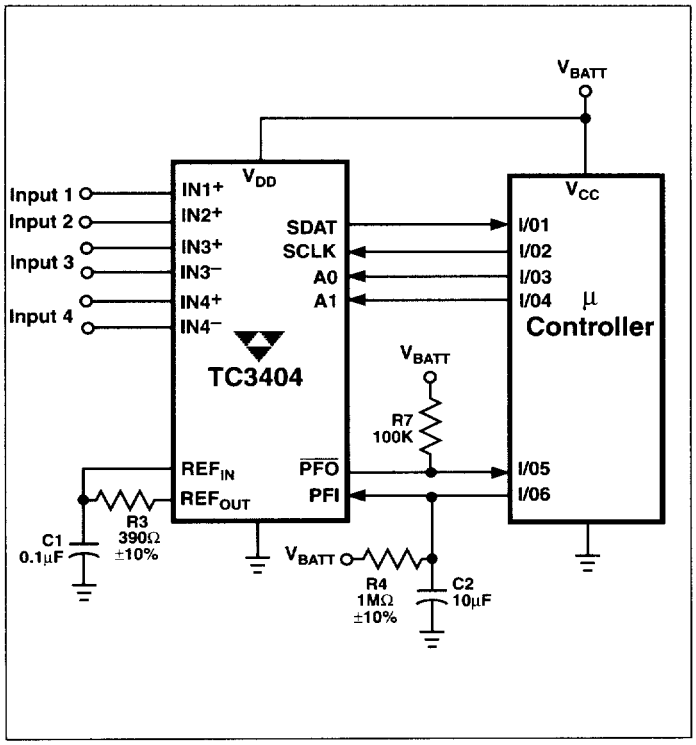
FEATURES

- 16-Bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-Bit Resolution at 512 Conversions Per Second
- 1.8V – 5.5V Operation, Low Power Operating .... 280µA ..... Sleep: 37µA
- Two Differential and Two Single Ended Inputs with Built-In Multiplexer
- MicroPort™ Serial Bus Requires Only Two Interface Lines
- Uses Internal or External Reference
- Early Warning Power Fail Detector, Also Suitable as Wake-Up Timer Operational in Shutdown Mode
- Automatically Enters Sleep Mode When Not In Use
- 16-Pin QSOP and PDIP Packages

TYPICAL APPLICATIONS

- Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
- Embedded Systems, Data Loggers, Portable Equipment
- Medical Instruments

TYPICAL APPLICATION



GENERAL DESCRIPTION

The TC3404 is a low cost, low power analog-to-digital converter based on TelCom's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3404 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. Threshold detector is provided for use as an early warning power fail detector, or as a wake-up timer.

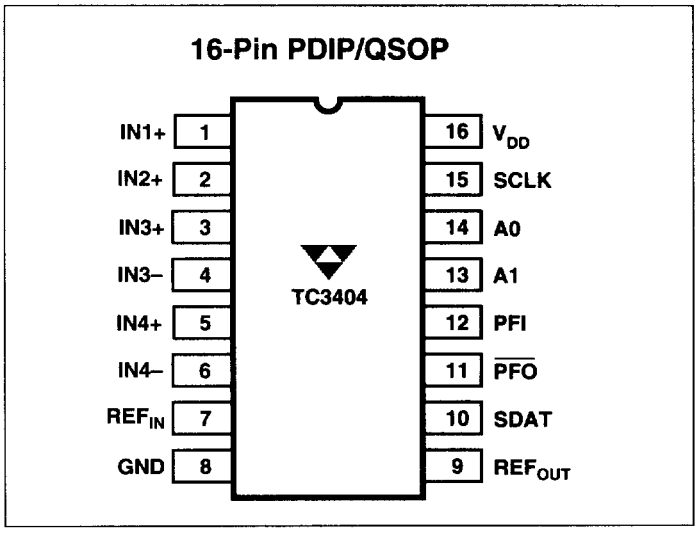
The TC3404's 2-wire MicroPort™digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

The TC3404 is available in 16-Pin PDIP and 16-Pin QSOP packages.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC3404VPE	16-Pin PDIP (Narrow)	0°C to +85°C
TC3404VQR	16-Pin QSOP (Narrow)	0°C to +85°C

PIN CONFIGURATIONS



TC3404

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 6.0V
Voltage on Pins:
$\overline{PFO}$ ..... (GND – 0.3V) to 5.5V
Input Voltage (All Other Pins) .....
..... (GND – 0.3V) to (V_{DD} + 0.3V)
Operating Temperature ..... 0°C to 85°C
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C. V_{REF} =1.25V, Internal Clock Freq = 520kHz

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
V_{DD}	Supply Voltage		1.8	—	5.5	V
I_{DD}	Supply Current, During Data Conversion		—	280	—	µA
$I_{DD(SLEEP)}$	Supply Current, Sleep Mode	T_A = +25°C	—	37	50	µA
$I_{DD(SLEEP)}$			—	**46**	**60**	µA
ACCURACY						
RES	Resolution		—	16	—	Bits
INL	Integral Non-Linearity	V_{DD} = 2.7V	—	.0038	—	%FSR
V_{OS}	Offset Error	$IN^+ = IN^- = 0V$	—	—	**±1.0**	%FSR
V_{NOISE}	Refered to input		—	60	—	µVrms
CMR	Common Mode Rejection	at DC	—	75	—	dB
FSE	Full Scale Error		—	0.4%	—	%FS
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.5V to 3.5V	—	75	—	dB
INn+						
V_{IN}	Input Voltage	(Note 1)	—	—	V_{DD}	V
	Absolute Voltage Range INn		GND	—	V_{DD}	V
	Input Bias Current		—	1	100	nA
C_{IN}	Input Sampling Capacitance		—	2	—	pF
R_{IN}	Input Resistance	(Note 2)	—	2.0	—	M
REF_{IN}, REF_{OUT}						
V_{REF}	REF_{IN} Voltage Range		0	—	1.25	V
I_{REF}	REF_{IN} Input Current		—	1	—	µA
V_{REFOUT}	REF_{OUT} Voltage		1.175	1.193	1,210	V
REF_{SINK}	REF_{OUT} Current Sink Capability		—	10	—	µA
REF_{SRC}	REF_{OUT} Current Source Capability		300	—	—	µA
SCLK, ADDR						
V_{IL}	Input Low Voltage		—	—	**0.3 x V_{DD}**	V
V_{IH}	Input High Voltage		**0.7 x V_{DD}**	—	—	V
I_{LEAK}	Leakage Current		—	1	—	µA

Notes: 1. Input voltage defined as (V_{IN}+ – GND or V_{IN}+ – V_{IN}–)
2. Resistance from INn+ to GND.

DC ELECTRICAL CHARACTERISTICS : T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified.

Specifications in Bold type apply over a temperature range of 0°C to 85°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SDAT						
V_{OL}	Output Low Voltage	I_{OL} = 1.5mA	—	—	0.4	V
V_{OH}	Output High Voltage (SDAT)	I_{SOURCE} = 400µa (Note 2)	0.9 x V_{DD}	—	—	V
$V_{DD(MIN)}$	Minimum V_{DD} for $\overline{PFO}$, $\overline{RESET}$ Valid		—	1.1	1.3	V
V_{TH}						
V_{CCPFI}	PFI Input Voltage Range		0	—	V_{DD}	V
	V_{TH}, PFI Input Current		–0.1	.01	0.1	µA
V_{THR}	Threshold		—	1.23	—	V
	Threshold Hysteresis		—	30	—	mV

AC ELECTRICAL CHARACTERISTICS: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C. V_{REF} =1.25V, Internal Clock Freq = 520kHz

Symbol	Parameter	Description	Min	Typ	Max	Unit
t_1		Width of SCLK (Negative)	1	—	—	µsec
t_2	Resolution Reduction Clock Width	Width of SCLK (Positive)	1	—	—	µsec
t_3	Conversion Time (15-Bit Plus Sign)	16-bit conversion, T_A = 25° (Note 1)	—	125	—	msec
	Conversion Time (14-Bit Plus Sign)	15-bit conversion	—	t3/2.0	—	msec
	Conversion Time (13-Bit Plus Sign)	14-bit conversion	—	t3/4.0	—	msec
	Conversion Time (12-Bit Plus Sign)	13-bit conversion	—	t3/7.8	—	msec
	Conversion Time (11-Bit Plus Sign)	12-bit conversion	—	t3/15.1	—	msec
	Conversion Time (10-Bit Plus Sign)	11-bit conversion	—	t3/28.6	—	msec
	Conversion Time (9-Bit Plus Sign)	10-Bit conversion	—	t3/51.4	—	msec
t_4	Resolution Reduction Window	Width of SCLK	—	t3/85.7	—	msec
t_5	SCLK to Data Valid	SCLK falling edge to SDAT valid	**1000**	—	—	nsec
t_6	Address Setup	Address valid to SCLK	**0**	—	—	nsec
t_7	Address Hold	SCLK to address valid hold	**1000**	—	—	nsec
t_8	Acknowledge Delay	SCLK to SDAT delay	—	—	**1000**	nsec
t_{10}	$\overline{PFO}$ Delay	PFI to $\overline{PFO}$ delay	—	25	—	µsec

Notes: 1. Nominal temperature drift is -2830 ppm/°C for temperature less than 25°C and -1340 ppm/°C for temperatures greater than 25°C.
2. @V_{DD} =1.8V, $I_{SOURCE} \leq$ 200µa

TC3404

PIN DESCRIPTION

TC3404 Pin No.	Name	Description
1,2	INn^+	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. (See *Electrical Characteristics.*)
3,5	INn^+	Analog Input. This is the positive terminal of a true differential input consisting of INn^+ and INn^-. $V_{IN(n)} = (INn^+ - INn^-)$.(See *Electrical Characteristics.*)
4,6	INn^-	Analog Input. This is the negative terminal of a true differential input consisting of INn^+ and INn^-. $V_{IN(n)} = (INn^+ - INn^-)$ INn^- can swing to, but not below, ground. (See *Electrical Characteristics.*)
7	REF_{IN}	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be connected to REF_{OUT} as shown on page 1 or scaled using a resistor divider. Any user supplied reference voltage or the power supply rail may be used in place of REF_{OUT}.
8	GND	Ground Terminal.
9	REF_{OUT}	Analog Output. The internal reference connects to this pin. It may be scaled externally, if desired, and tied to the REF_{IN} input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin. (See *Electrical Characteristics.*)
10	SDAT	Digital Output (push-pull). This is the MicroPort™ serial data output. SDAT is driven low while the TC3404 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high-to-low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).
11	$\overline{PFO}$	Digital Output (open drain). This is the output of the internal threshold detector. When PFI is less than the internal reference, $\overline{PFO}$ is driven low.
12	PFI	Analog Input. This is the positive input to an internal comparator used as a threshold detector. The negative input is tied to an internal reference.
13	A1	Digital Input. Controls analog multiplexer in conjunction with A0 to select one of the four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
14	A0	Digital Input. Controls analog multiplexer in conjunction with A1 to select one of four Input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1,A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
15	SCLK	Digital Input. This is the MicroPort™ serial clock input. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t4 seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
16	V_{DD}	Power Supply Input. (See *Electrical Characteristics.*)