HM534251B Series

262,144-word × 4-bit Multiport CMOS Video RAM

Rev. 1
Mar. 18, 1994

HITACHI

The HM534251B is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

Features

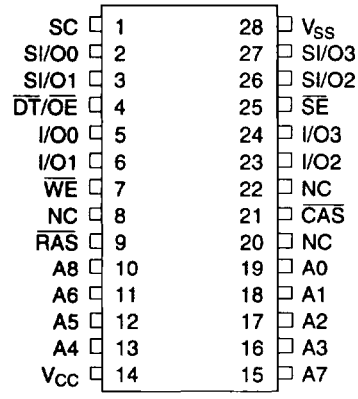
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
    - RAM: 256 kword x 4 bit
    - SAM: 512 word x 4 bit
- Access time
  - RAM: 60 ns/70 ns/80 ns/100 ns max
  - SAM: 20 ns/22 ns/25 ns/25 ns max
- Cycle time
  - RAM: 125 ns/135 ns/150 ns/180 ns min
  - SAM: 25 ns/25 ns/30 ns/30 ns min
- Low power
  - Active RAM: 413 mW max
  - SAM: 275 mW max
  - Standby 38.5 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer cycle capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HM534251BJ-6	60 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM534251BJ-7	70 ns	
HM534251BJ-8	80 ns	
HM534251BJ-10	100 ns	
HM534251BZ-6	60 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM534251BZ-7	70 ns	
HM534251BZ-8	80 ns	
HM534251BZ-10	100 ns	
HM534251BT-6	60 ns	8 mm x 14 mm 32-pin TSOP type I (TFP-32DA)
HM534251BT-7	70 ns	
HM534251BT-8	80 ns	
HM534251BT-10	100 ns	
HM534251BR-6	60 ns	8 mm x 14 mm 32-pin TSOP type I reverse (TFP-32DAR)
HM534251BR-7	70 ns	
HM534251BR-8	80 ns	
HM534251BR-10	100 ns	

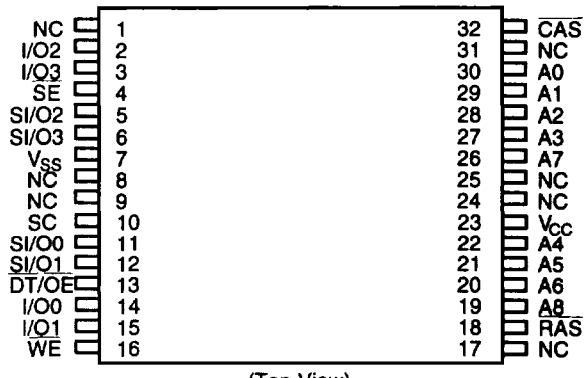
Pin Arrangement

HM534251BJ Series



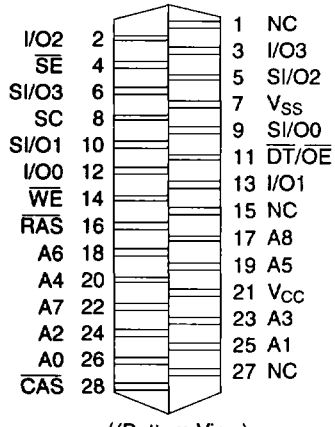
(Top View)

HM534251BT Series



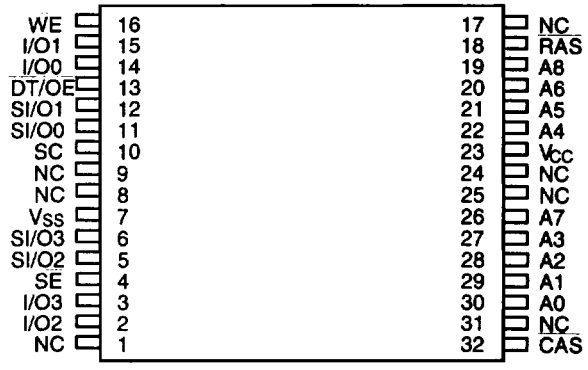
(Top View)

HM534251BZ Series



((Bottom View)

HM534251BR Series



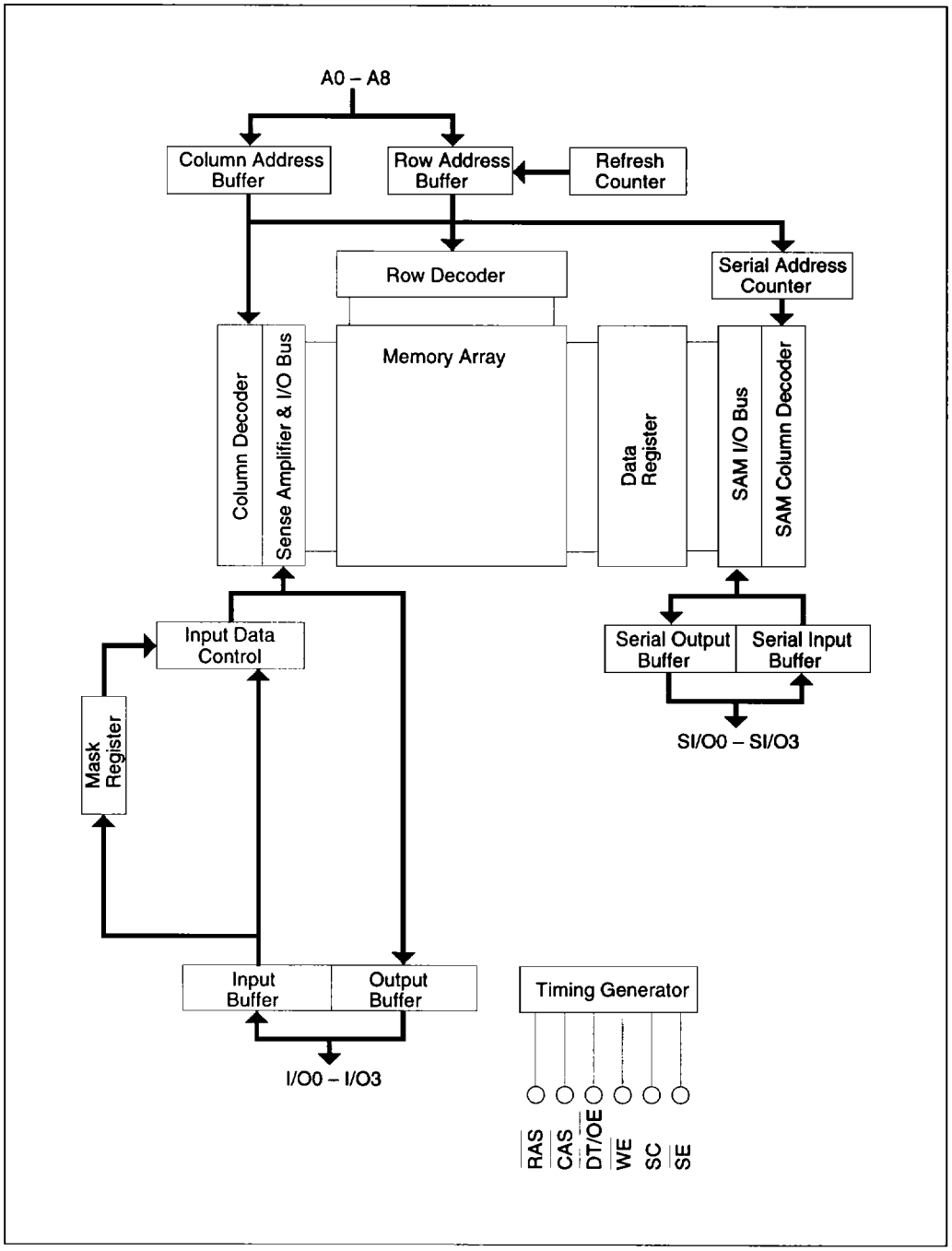
(Top View)

Pin Description

Pin name	Function
A0 – A8	Address inputs
I/O0 – I/O3	RAM port data inputs/outputs
SI/O0 – SI/O3	SAM port data inputs/outputs
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable

Pin name	Function
DT/OE	Data transfer/Output enable
SC	Serial clock
SE	SAM port enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Pin Functions

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534251B.

Table 1. Operation Cycles of the HM534251B

Input level at the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	Operation mode
L	X	X	X	CBR refresh
H	L	L	L	Write transfer
H	L	L	H	Pseudo transfer
H	L	H	X	Read transfer
H	H	L	X	Read/mask write
H	H	H	X	Read/write

Note: X : Don't care.

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0-A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251B turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0 – I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT/OE}$ (input pin): $\overline{DT/OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0-SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251B

RAM Read Cycle ($\overline{DT/OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT/OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT/OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)
($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.
If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.
If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.
If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

Transfer Operation

The HM534251B provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)
Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM
(2) Determine SI/O state
Read transfer cycle: SI/O output
Pseudo transfer cycle
and write transfer cycle: SI/O input
(3) Determine first SAM address to access after transferring at column address (SAM start address).
SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.
This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.).

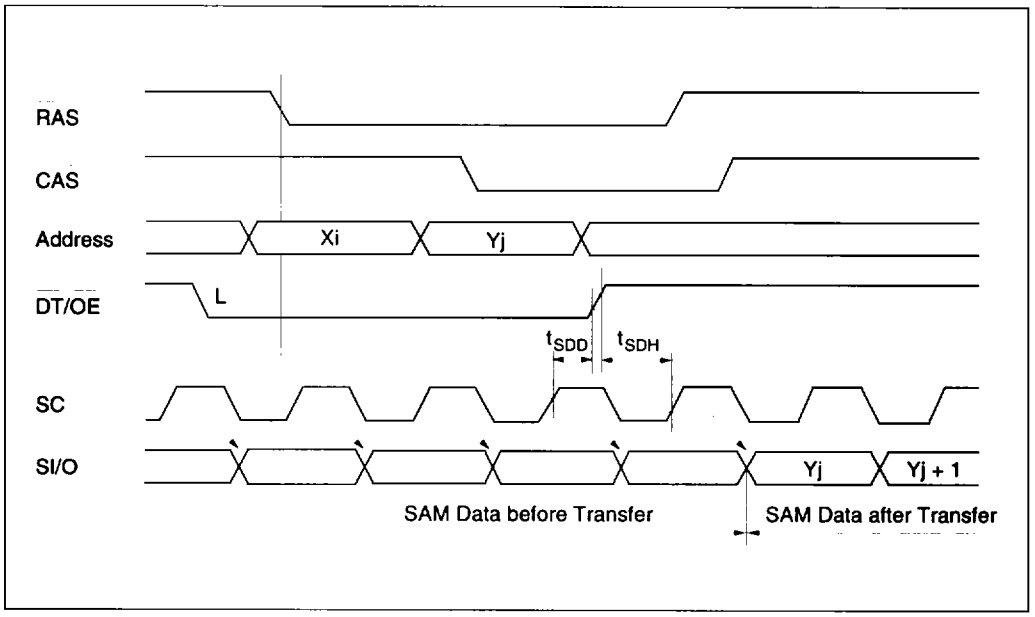


Figure 1. Real Time Read Transfer

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.
This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.
Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage*1	V_T	−1.0 to +7.0	V
Power supply voltage*1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: 1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage*1	V_{CC}	4.5	5.0	5.5	V
Input high voltage*1	V_{IH}	2.4	—	6.5	V
Input low voltage*1	V_{IL}	–0.5*2	—	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. –3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM534251B										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Operating current	I_{CC1}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	—	40	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{RAS}$-only refresh current	I_{CC3}	—	75	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	125	—	120	—	100	—	95	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Page mode current	I_{CC4}	—	80	—	80	—	70	—	65	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL} t_{PC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	130	—	130	—	110	—	105	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	50	—	45	—	40	—	35	mA	$\overline{RAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	100	—	95	—	80	—	75	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min
Data transfer current	I_{CC6}	—	80	—	75	—	65	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	130	—	125	—	105	—	100	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = min

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM534251B										
		-6		-7		-8		-10			Test conditions	
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	RAM port	SAM port
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA		
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA		
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once while $\overline{RAS}$ is low and $\overline{CAS}$ is high.

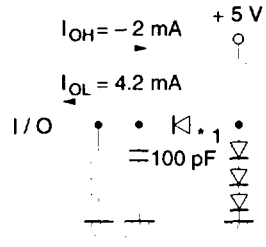
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

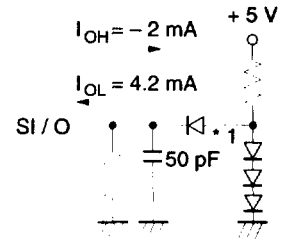
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V) *1, *16

Test Conditions

- Input rise and fall time: 5 ns
- Output load: See figures
- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V



Output Load (A)



Output Load (B)

Note: 1. Including scope & jig.

Common Parameter

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	135	—	150	—	180	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	55	—	60	—	70	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	—	20	—	20	—	25	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	20	60	20	75	ns	2
$\overline{RAS}$ hold time referenced to $\overline{CAS}$	t_{RSH}	20	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	10	—	10	—	10	—	10	—	ns	
Data-in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	4
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	20	—	20	—	20	ns	5
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	20	ns	5

Read Cycle (RAM), Page Mode Read Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	10
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	2
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	35	—	35	—	40	—	45	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	40	—	45	—	50	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	11
Write command hold time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	10	—	10	—	10	—	10	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	
Page mode cycle time	t_{PC}	45	—	45	—	50	—	55	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ to data-in delay time	t_{CDD}	20	—	20	—	20	—	20	—	ns	13
Page mode $\overline{RAS}$ pulse width	t_{RASP}	60	100000	70	100000	80	100000	100	100000	ns	

Read-Modify-Write Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	175	—	185	—	200	—	230	—	ns	
$\overline{RAS}$ pulse width (read-modify-write cycle)	t_{RWS}	110	10000	120	10000	130	10000	150	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	45	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	60	—	65	—	70	—	ns	14
$\overline{OE}$ to data-in delay time	t_{ODD}	20	—	20	—	20	—	20	—	ns	12
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7
Access time form $\overline{CAS}$	t_{CAC}	—	20	—	20	—	20	—	25	ns	7, 8
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	20	—	25	ns	7
Address access time	t_{AA}	—	35	—	35	—	40	—	45	ns	7, 9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	12
Data-in hold time	t_{DH}	15	—	15	—	15	—	15	—	ns	12
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	20	—	20	—	20	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle

Item	Symbol	HM534251B -6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	-10 Min	-10 Max	Unit	Notes
$\overline{DT}$ hold time referenced to $\overline{RAS}$	t_{RDH}	50	10000	60	10000	65	10000	80	10000	ns	
$\overline{DT}$ hold time referenced to $\overline{CAS}$	t_{CDH}	20	—	20	—	20	—	25	—	ns	
$\overline{DT}$ hold time referenced to column address	t_{ADH}	25	—	25	—	30	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	20	—	20	—	20	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ delay time	t_{DRD}	65	—	65	—	70	—	80	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	25	—	25	—	30	—	30	—	ns	
1st SC to $\overline{RAS}$ hold time	t_{SRH}	60	—	70	—	80	—	100	—	ns	
1st SC to $\overline{CAS}$ hold time	t_{SCH}	25	—	25	—	25	—	25	—	ns	
1st SC to column address hold time	t_{SAH}	40	—	40	—	45	—	50	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	5	—	ns	
1st SC to $\overline{DT}$ hold time	t_{SDH}	10	—	10	—	15	—	15	—	ns	
Serial data-in to 1st SC delay time	t_{SZS}	0	—	0	—	0	—	0	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	

Read Transfer Cycle (cont)

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	35	15	40	15	55	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	35	—	40	—	45	—	ns	
$\overline{DT}$ high hold time from $\overline{RAS}$ precharge	t_{DTHH}	10	—	10	—	10	—	10	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{SE}$ setup time referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{EH}	10	—	10	—	10	—	10	—	ns	
SC setup time referenced to $\overline{RAS}$	t_{SRS}	25	—	25	—	30	—	30	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	20	—	20	—	25	—	25	—	ns	
Serial output buffer turn-off time referenced to $\overline{RAS}$	t_{SRZ}	10	40	10	40	10	45	10	50	ns	
$\overline{RAS}$ to serial data-in delay time	t_{SID}	40	—	40	—	45	—	50	—	ns	
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge time	t_{SCP}	10	—	10	—	10	—	10	—	ns	
SC access time	t_{SCA}	—	20	—	22	—	25	—	25	ns	15

Pseudo Transfer Cycle, Write Transfer Cycle (cont)

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{SE}$ access time	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	

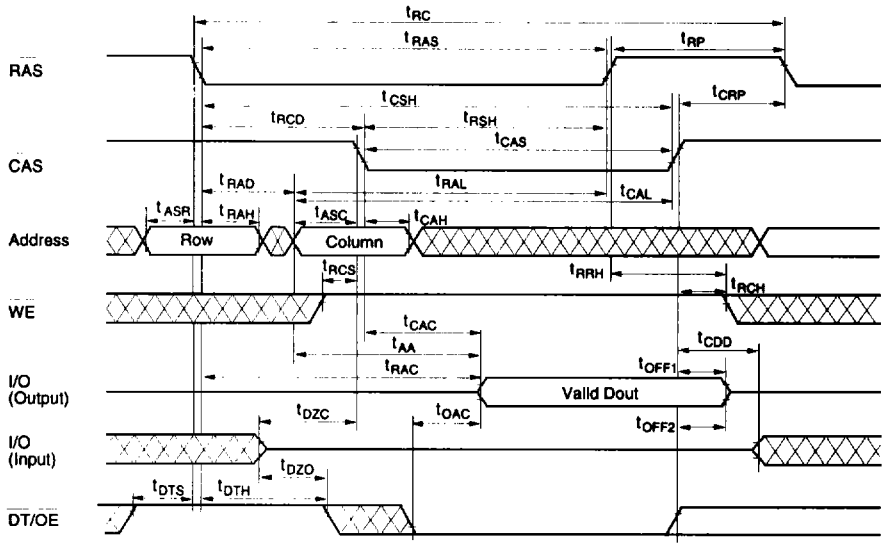
Serial Read Cycle, Serial Write Cycle

		HM534251B									
		-6		-7		-8		-10			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Serial clock cycle time	t_{SCC}	25	—	25	—	30	—	30	—	ns	
SC pulse width	t_{SC}	5	—	5	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Access time from SC	t_{SCA}	—	20	—	22	—	25	—	25	ns	15
Access time from $\overline{SE}$	t_{SEA}	—	20	—	22	—	25	—	25	ns	15
Serial data-out hold time	t_{SOH}	5	—	5	—	5	—	5	—	ns	
Serial output buffer turn-off time referenced to $\overline{SE}$	t_{SEZ}	—	20	—	20	—	20	—	20	ns	5
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	15	—	15	—	15	—	ns	
Serial write enable setup time	t_{SWS}	5	—	5	—	5	—	5	—	ns	
Serial write enable hold time	t_{SWH}	15	—	15	—	15	—	15	—	ns	
Serial write disable setup time	t_{SWIS}	5	—	5	—	5	—	5	—	ns	
Serial write disable hold time	t_{SWIH}	15	—	15	—	15	—	15	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output acheives the open circuit condition (V_{OH} −100 mV, V_{OL} +100 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 µs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

Timing Waveforms *17

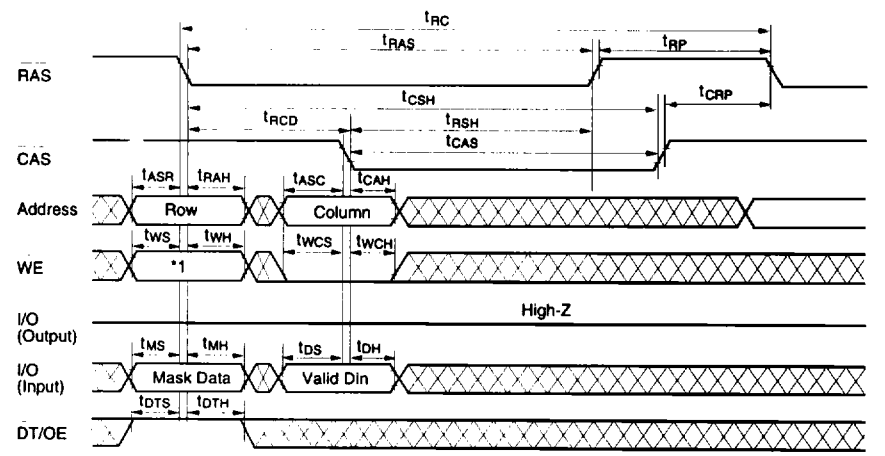
Read Cycle



Note17: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

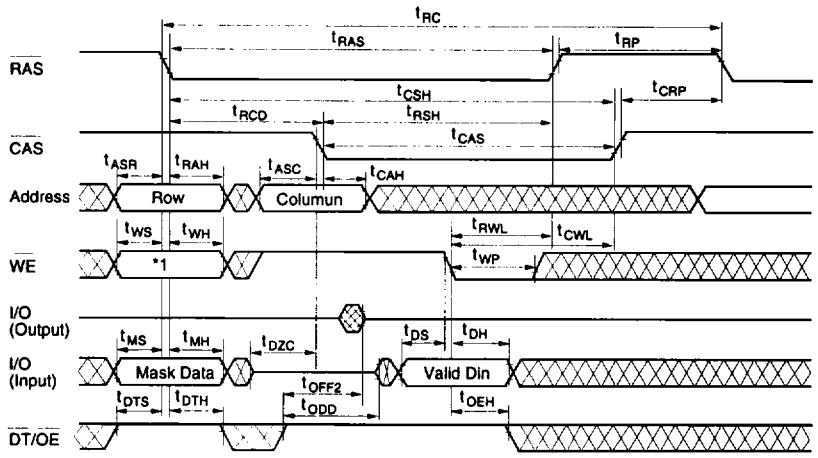
Invalid Dout

Early Write Cycle



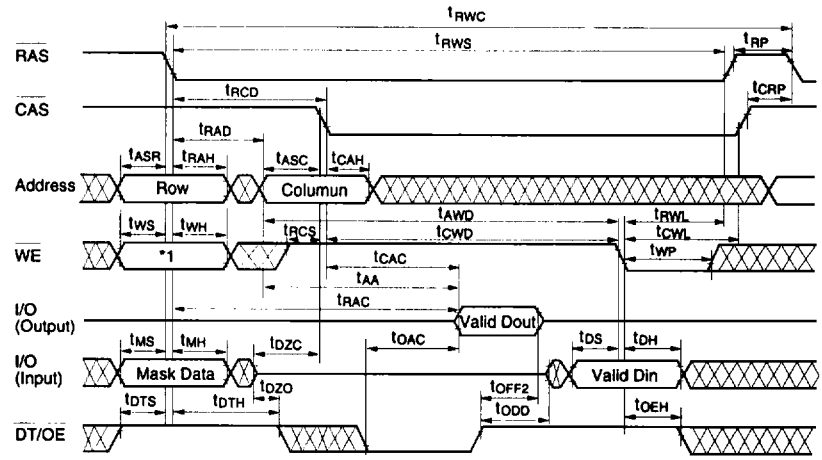
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Delayed Write Cycle



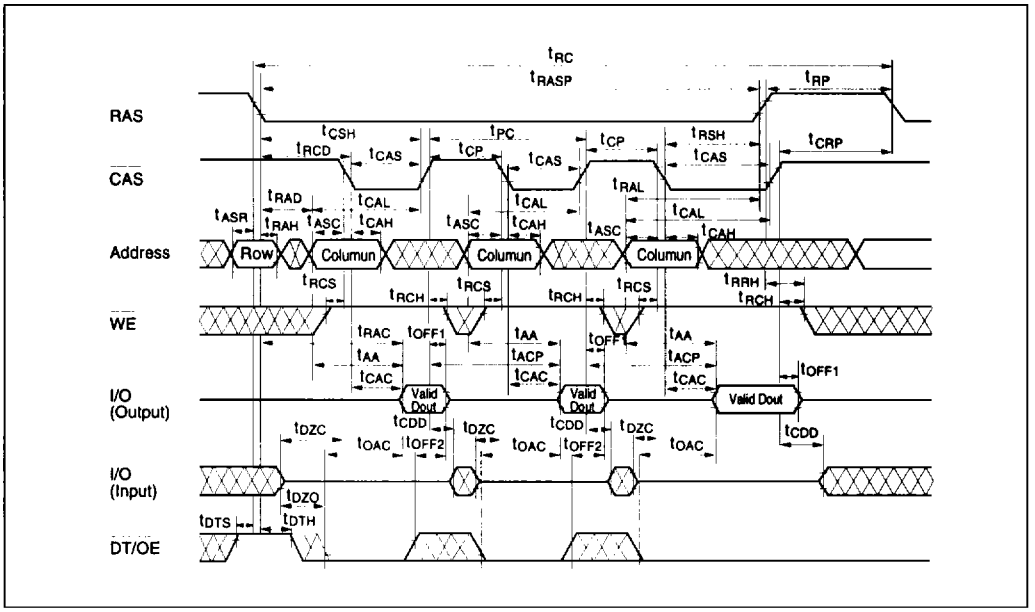
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Read-Modify-Write Cycle

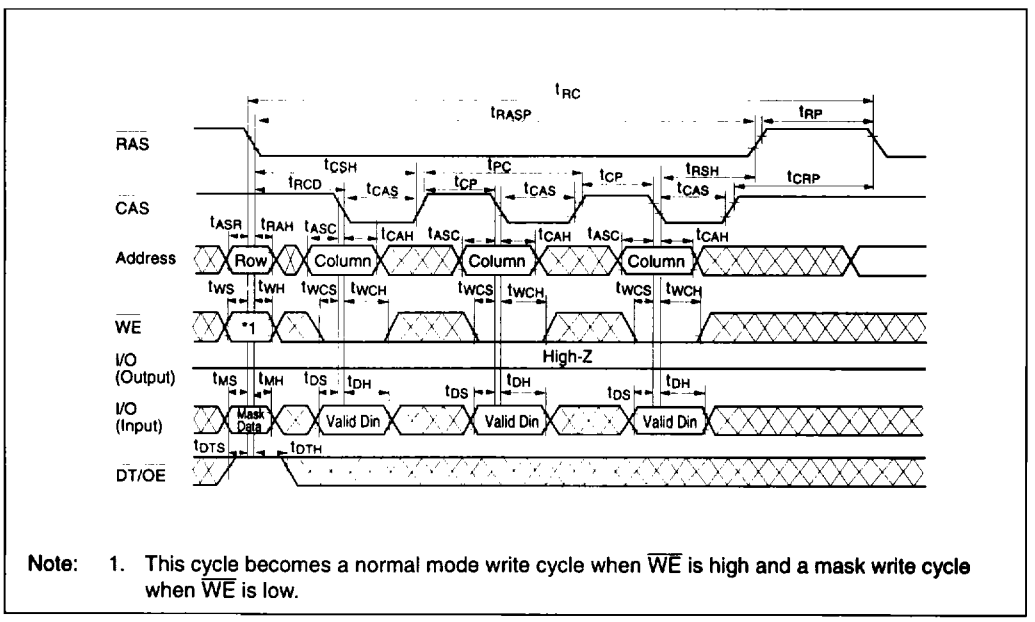


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Read Cycle

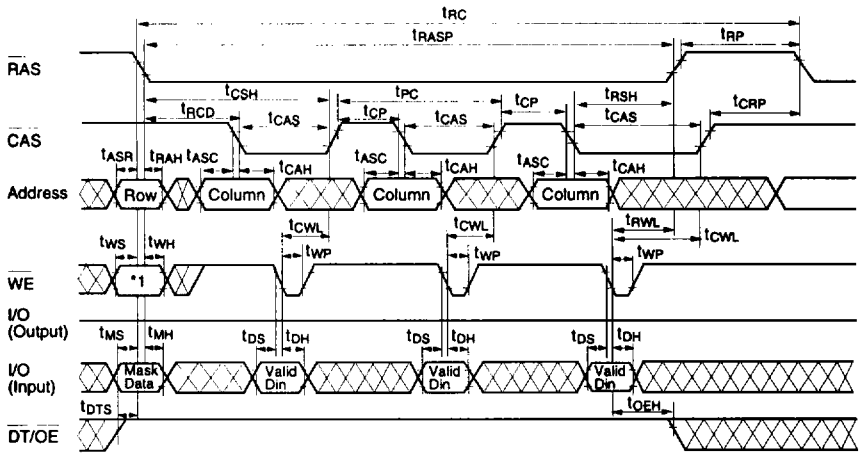


Page Mode Write Cycle (Early Write)



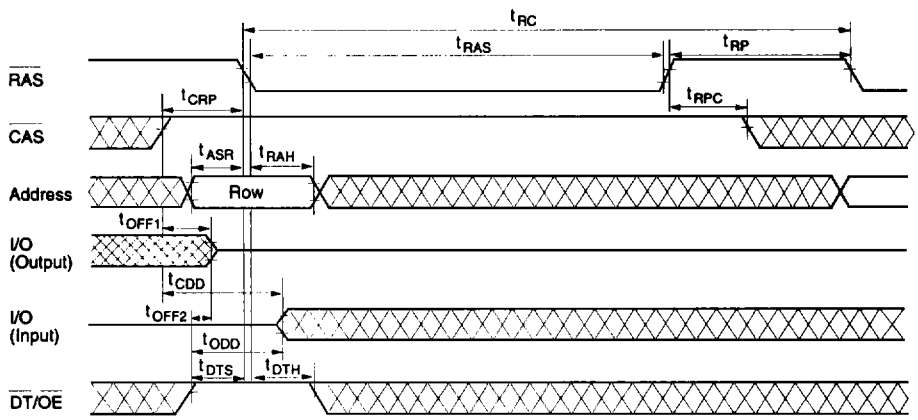
Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

Page Mode Write Cycle (Delayed Write)

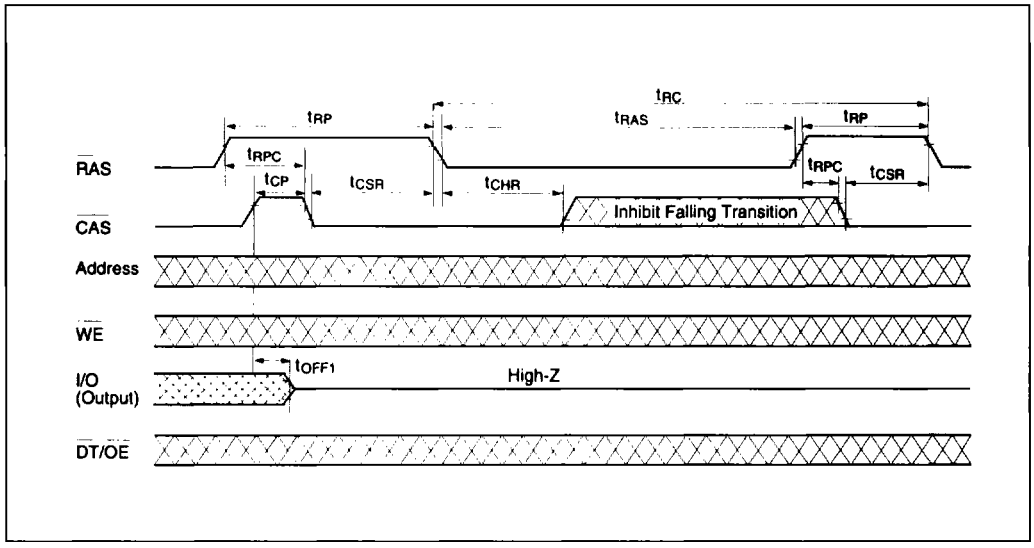


Note: 1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

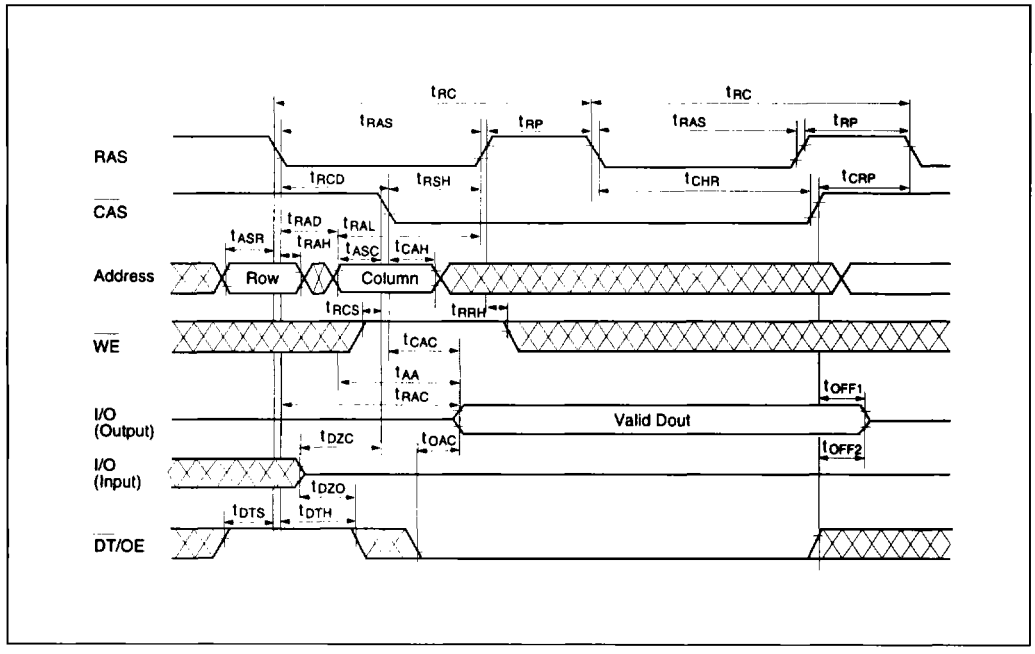
$\overline{RAS}$-Only Refresh Cycle



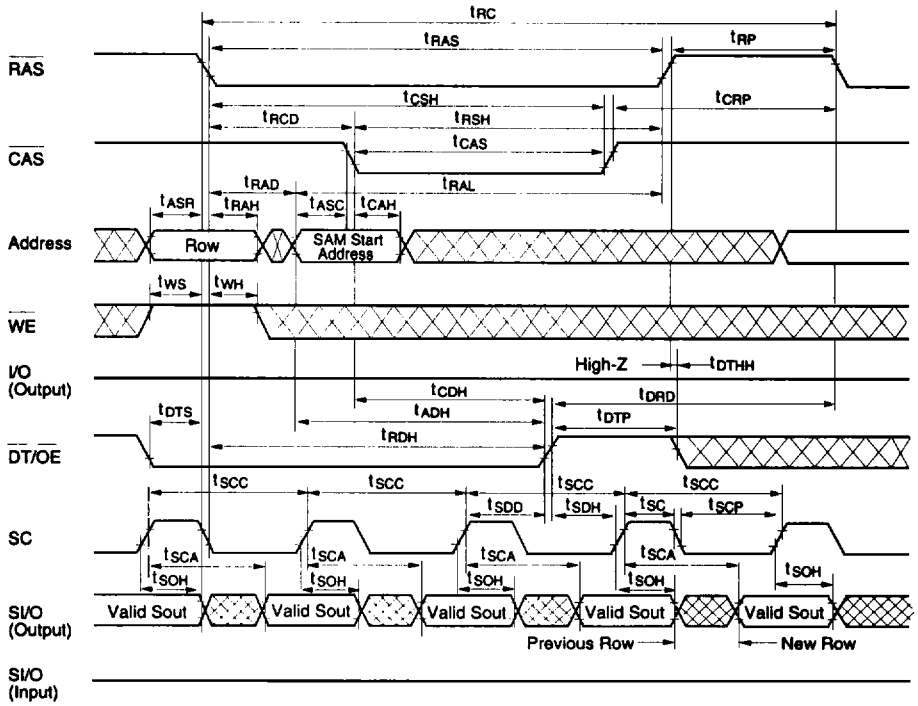
CAS-Before-RAS Refresh Cycle



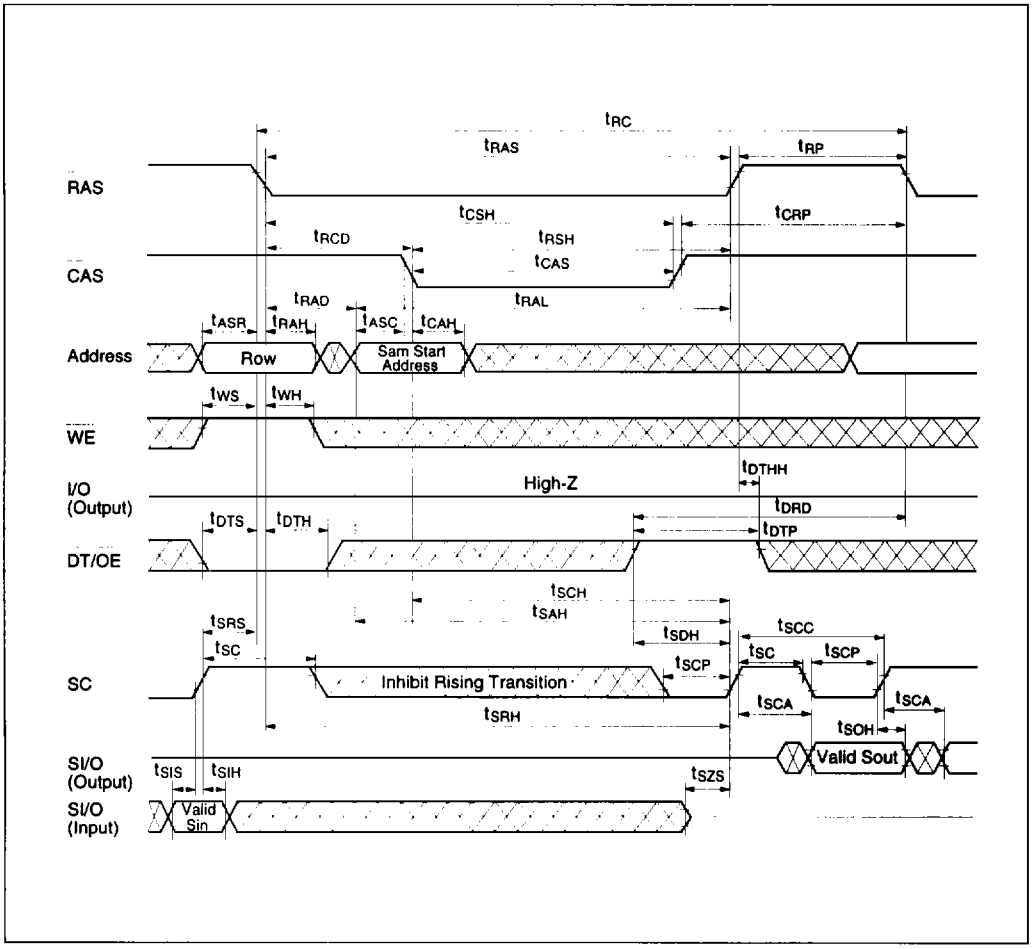
Hidden Refresh Cycle



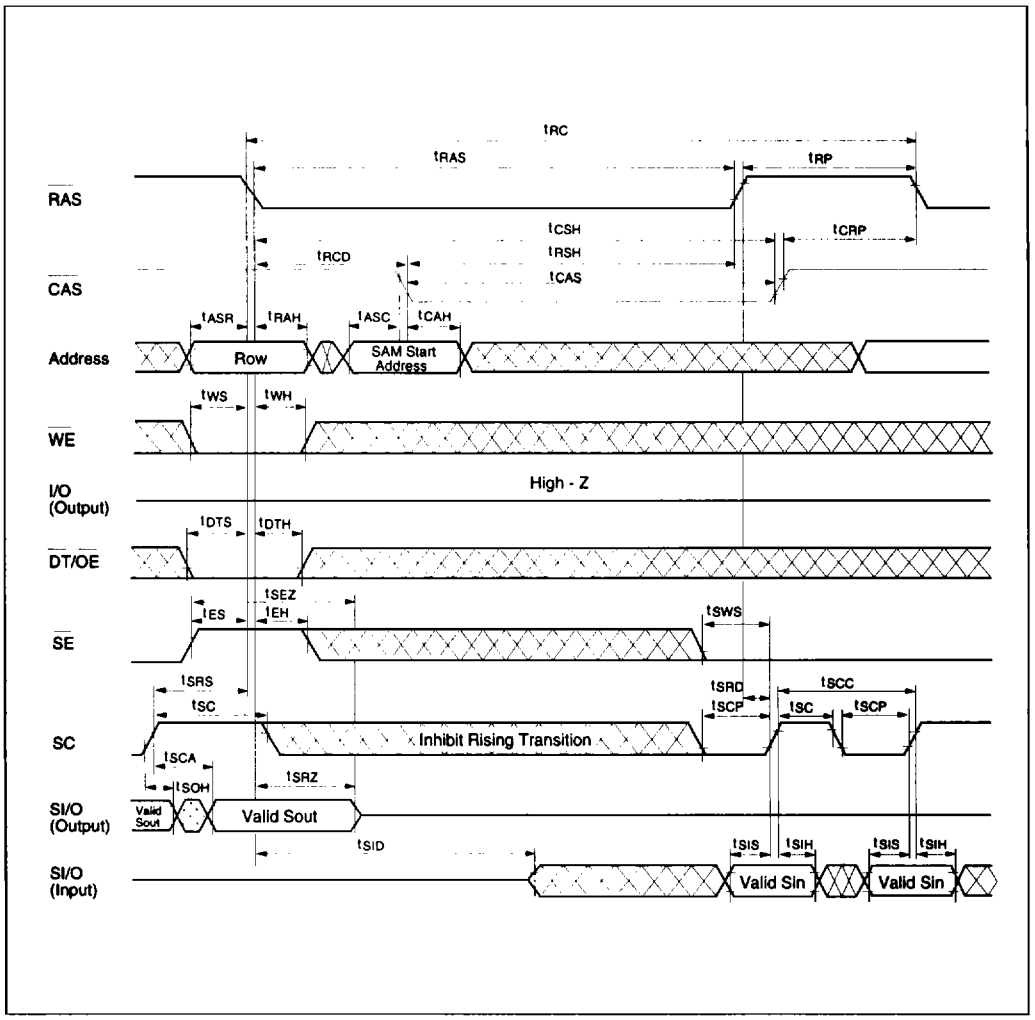
Read Transfer Cycle (1)



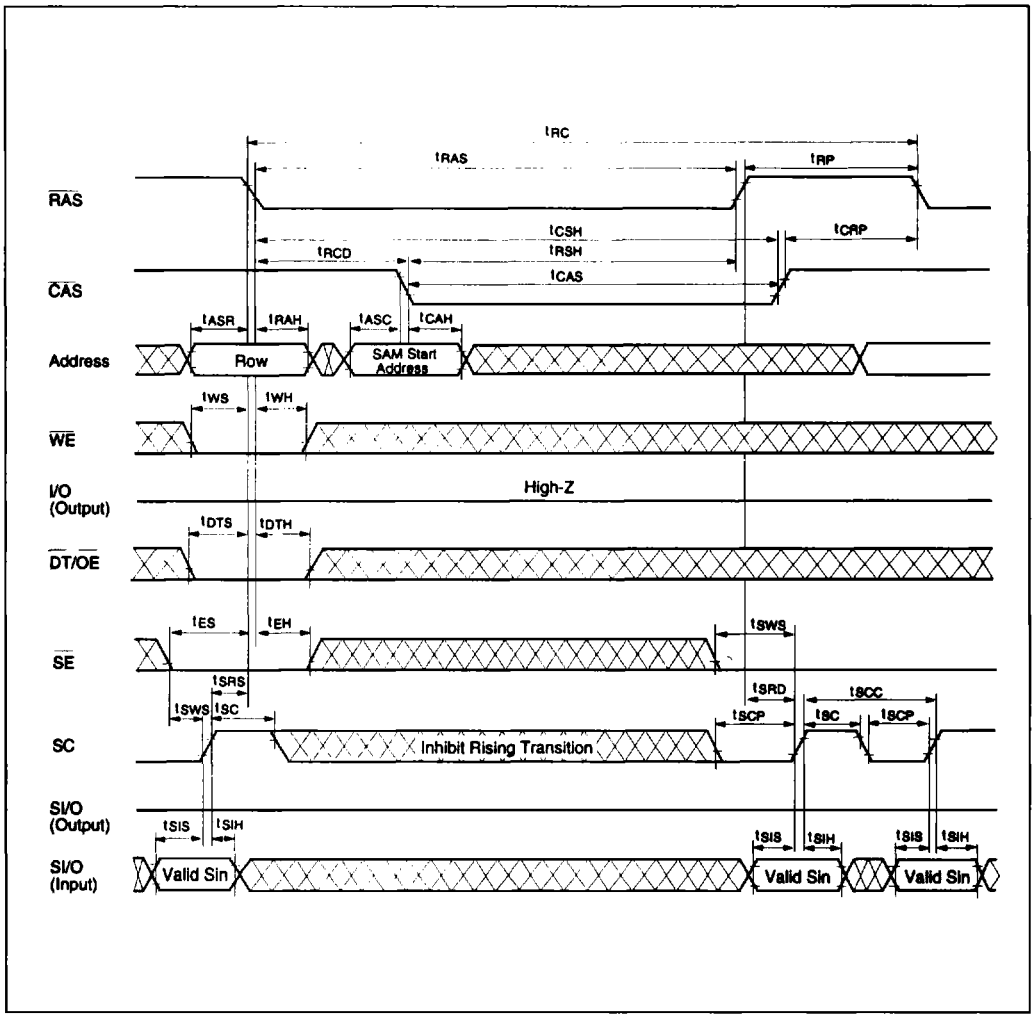
Read Transfer Cycle (2)



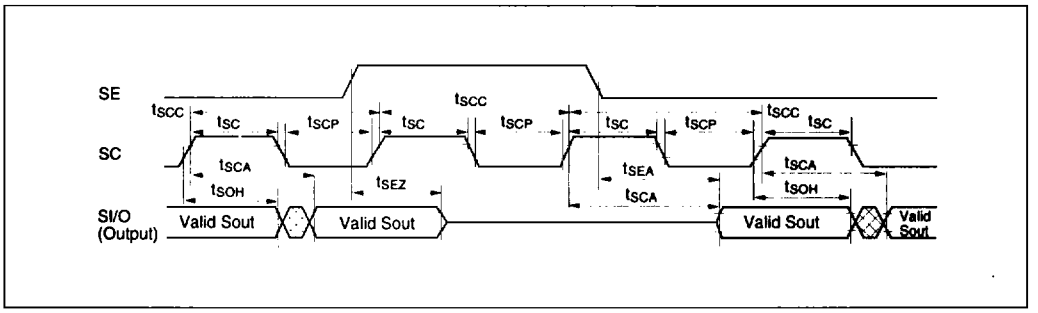
Pseudo Transfer Cycle



Write Transfer Cycle



Serial Read Cycle



Serial Write Cycle