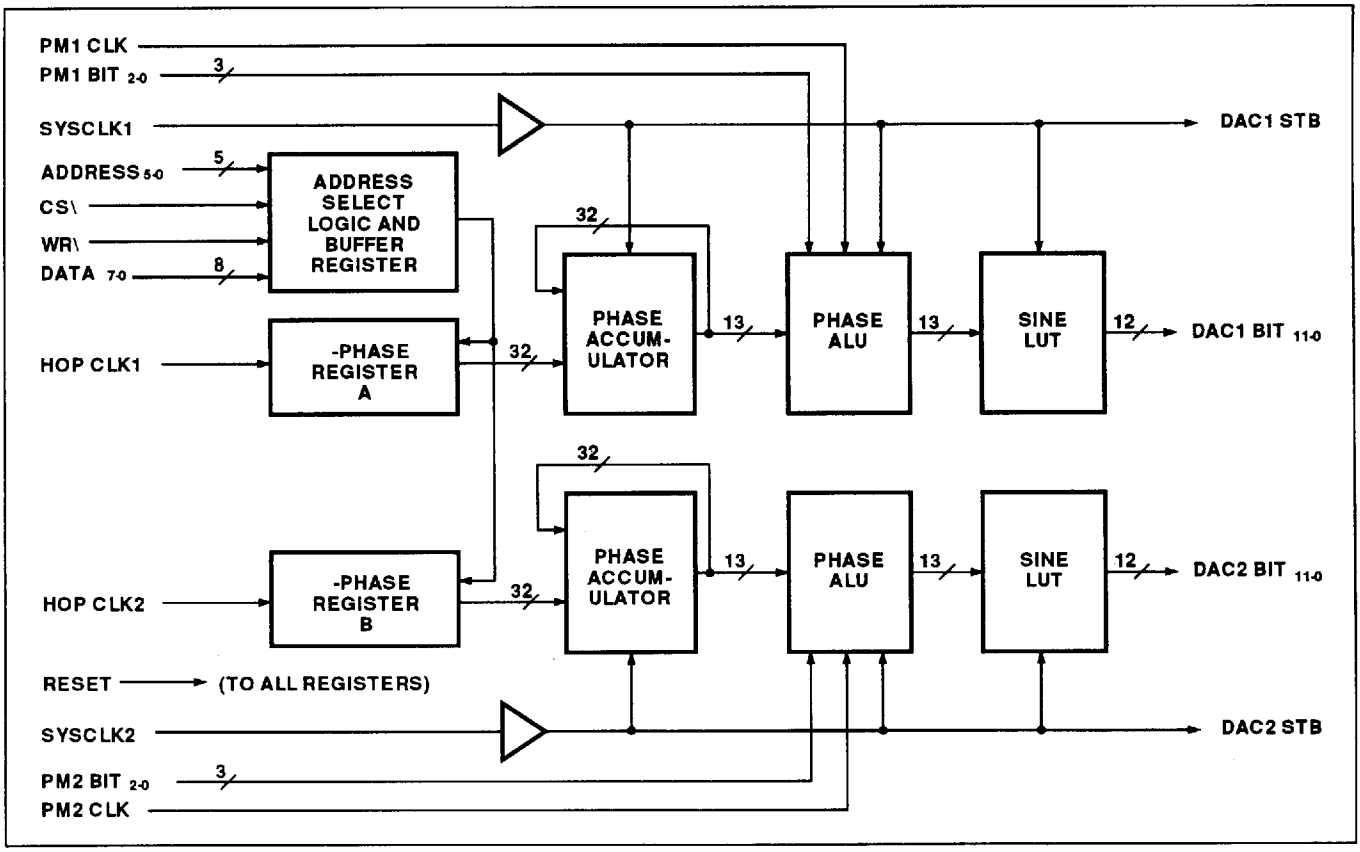
FEATURES

- **TWO COMPLETELY INDEPENDENT NCOs IN A SINGLE PACKAGE**
- **80 MHz MAXIMUM CLOCK FREQUENCY**
- **LOWER COST 50 MHz VERSION AVAILABLE**
- **32-BIT FREQUENCY RESOLUTION**
  - **12 milli-Hz @ 50 MHz**
  - **19 milli-Hz @ 80 MHz**
- **WIDE OUTPUT BANDWIDTH**
  - **0 TO 32 MHz @ 80 MHz CLOCK**
- **3-BIT PHASE MODULATION**
- **SINE OR COSINE SIGNAL GENERATION**
  - **12-BIT OUTPUTS**
- **HIGH SPECTRAL PURITY**
  - **ALL SPURS < -75 dBc**
- **MICROPROCESSOR COMPATIBLE INPUTS**
- **PROPRIETARY NOISE-REDUCTION TECHNIQUES UTILIZED**
- **68 PIN PLCC AND CLDCC PACKAGES**

FUNCTIONAL DESCRIPTION

The STEL-1178A features two completely independent 32-bit Numerically Controlled Oscillators in a single package operating at up to 80 MHz. A lower cost 50 MHz version is also available. It provides a compact, low-cost solution to applications requiring two independently controlled precision frequency sources. Separate registers control the functions of the two NCOs, making the device very easy to program. In the STEL-1178A the two NCOs also have independent 3-bit phase modulation, making the device suitable for phase modulation applications as well as making it possible to use an STEL-1178A as a quadrature synthesizer. The two NCOs also have independent clocks. The 12-bit outputs provide –75 dBc purity with suitable DACs, and DAC strobe outputs are also provided to simplify DAC timing. The STEL-1178A uses digital techniques to provide a cost-effective solution for low noise signal sources. The dual NCO features high frequency resolution with exceptional spectral purity of outputs up to 32 MHz. The device combines low power 1.5µ CMOS technology with a unique architectural design resulting in a power efficient, high-speed dual sinusoidal waveform generator able to achieve fine tuning resolution and exceptional spectral purity at clock frequencies up to 80 MHz. The dual NCO is designed to provide a simple interface to an 8-bit microprocessor bus.

BLOCK DIAGRAM



Each NCO maintains a record of phase which is accurate to 32 bits. At each clock cycle the number stored in the 32-bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine function. The number in the Δ-Phase register represents the phase change for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

where: f_o is the frequency of the output signal

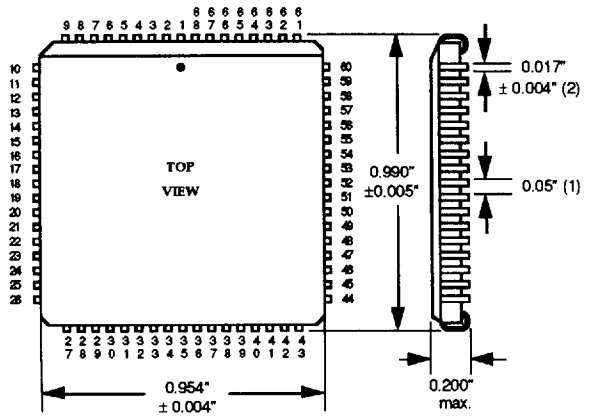
and: f_c is the clock frequency.

The sine functions are generated from the 13 most significant bits of the phase accumulators. The frequency of each NCO is determined by the number stored in the Δ-Phase Register, which may be programmed by an 8-bit microprocessor.

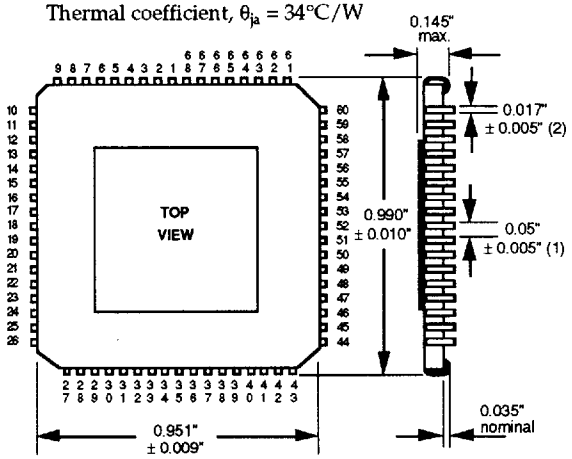
Each NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at frequencies greater than half the clock frequency, and become more difficult to remove by filtering.

PIN CONFIGURATION

Package: 68 pin PLCC
Thermal coefficient, θ_{ja} = 36°C/W



Package: 68 pin CLDCC
Thermal coefficient, θ_{ja} = 34°C/W



Notes: (1) Tolerances on pin spacing are not cumulative.
(2) Dimensions apply at seating plane.
(3) PLCC and CLDCC packages have different corners and may not fit into sockets designed for the other type. Universal sockets are available without alignment locators.

PIN CONNECTIONS

1	SYS CLK2	15	DAC1 BIT_7	29	PM1 BIT_0		
2	V_{SS}	16	DAC1 BIT_6	30	PM1 CLK	43	$DATA_4$
3	$ADDRESS_0$	17	V_{SS}	31	N.C	44	V_{SS}
4	$ADDRESS_3$	18	V_{DD}	32	N.C	45	DAC2 BIT11
5	$ADDRESS_2$	19	DAC1 BIT_5	33	V_{DD}		(MSB)
6	$DATA_0$	20	DAC1 BIT_4	34	HOP CLK1	46	DAC2 BIT_{10}
7	$DATA_1$	21	DAC1 BIT_3	35	SYS CLK1	47	DAC2 BIT_9
8	$DATA_2$	22	DAC1 BIT_2	36	CS\	48	DAC2 BIT_8
9	$DATA_3$	23	DAC1 BIT_1	37	WR\	49	DAC2 BIT_7
10	V_{SS}	24	DAC1 BIT0 (LSB)	38	$ADDRESS_4$	50	DAC2 BIT_6
11	DAC1 BIT11 (MSB)	25	V_{SS}	39	$ADDRESS_1$	51	V_{SS}
12	DAC1 BIT_{10}	26	DAC1 STB	40	$DATA_7$	52	V_{DD}
13	DAC1 BIT_9	27	PM1 BIT_2	41	$DATA_6$	53	DAC2 BIT_5
14	DAC1 BIT_8	28	PM1 BIT_1	42	$DATA_5$	54	DAC2 BIT_4

55	DAC2 BIT_3	67	V_{DD}
56	DAC2 BIT_2	68	HOP CLK2
57	DAC2 BIT_1		
58	DAC2 BIT_0		
59	RESET		
60	DAC2 STB		
61	PM2 BIT_2		
62	PM2 BIT_1		
63	PM2 BIT_0		
64	PM2 CLK		
65	N.C.		
66	N.C.		

Notes: I.C. denotes Internal Connection. Do not use for vias.
N.C. denotes No Connection. May be used for vias.

The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

Each NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCOs represent 16 clock edges. Note that when frequency changes occur at the outputs the changes are instantaneous, i.e., they occur in one clock cycle, with complete phase continuity.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the **$DATA_{7-0}$** inputs. The data is written into the device on the rising edge of the **WR** input, and the register into which the data is written is selected by the **$ADDRESS_{4-0}$** inputs. The **CS** input can be used to selectively enable the writing of data from the bus.

Δ-PHASE BUFFER REGISTER BLOCK

The Δ-Phase Buffer Register is used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as four bytes per 32-bit Δ-Phase word. The data is transferred from these registers into the Δ-Phase Registers after a falling edge on the **HOP CLK1** or **HOP CLK2** inputs.

Δ-PHASE REGISTER BLOCKS 1 AND 2

These blocks control the updating of the Δ-Phase words used in the Accumulators. The frequency data from the Buffer Register Block is loaded into these blocks after a falling edge on the **HOP CLK1** or **HOP CLK2** inputs.

PHASE ACCUMULATOR BLOCKS 1 AND 2

These blocks form the core of the dual NCO function. They are high-speed, pipelined, 32-bit parallel accumulators, generating a new sum in every clock cycle. The overflow signal is discarded, since the required output is the modulo (2^{32}) sum only. This represents the modulo(2π) phase angle.

PHASE ALU BLOCKS 1 AND 2

These blocks perform the modulation of the outputs of the Phase Accumulators with the modulation signals **PM1 BIT_{2-0}** and **PM2 BIT_{2-0}**. These 3-bit signals allow the outputs of the NCOs to be modulated independently to generate a variety of signal types.

SINE LOOKUP TABLE BLOCKS 1 AND 2

These blocks are the sine memories. The 13 most significant bits from the Phase Accumulator Blocks are used to address these memories to generate the 12-bit **DAC1 BIT_{11-0}** and **DAC2 BIT_{11-0}** outputs.

INPUT SIGNALS

RESET

The **RESET** input is asynchronous and active high, and clears all the registers in the device. When **RESET** goes high all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns low. The data on the outputs will then be invalid for 4 clock cycles, and thereafter will remain at the value corresponding to zero phase until new frequencies are loaded with the **HOP CLK1/2** inputs after the **RESET** returns low. The individual accumulators can be reset (to set them to zero phase) without resetting the other circuits by means of the Accumulator Reset software command (ARST1 or 2), by writing dummy data into addresses $0C_H$ (NCO1) or $1C_H$ (NCO2) as shown in the address table. This will arm the corresponding ARST function so that at the next HOP CLK command (hardware or software) the accumulator will reset to zero phase when the frequency change occurs.

SYS CLK1, SYS CLK2

All synchronous functions performed within the NCOs are referenced to the falling edges of the corresponding **SYS CLK** input. The **SYS CLK1** and **SYS CLK2** signals should be nominally a square wave at a maximum frequency of 80 MHz. Non-repetitive **SYS CLK1/2** waveforms are permissible as long as the minimum duration positive or negative pulse on the waveforms are always greater than 4 nanoseconds (commercial).

CS\

The Chip Select input is used to control the writing of data into the chip. It is active low. When this input is high all data writing via the **$DATA_{7-0}$** bus is inhibited.

WR\

The Write Strobe input is used to latch the data on the **$DATA_{7-0}$** bus into the device. On the rising edge of the **WR** input, the information on the 8-bit data bus is transferred to the buffer register selected by the **$ADDR_{3-0}$** bus.

$DATA_7$ through $DATA_0$

The 8-bit **$DATA_{7-0}$** bus is used to program the two 32-bit Δ-Phase Registers. **$DATA_0$** is the least significant bit of the bus. The data programmed into the Δ-Phase Registers in this way determines the output frequencies of the NCOs.

$ADDR_4$ through $ADDR_0$

The five address lines $ADDR_{4-0}$ control the use of the $DATA_{7-0}$ bus for writing frequency data to the Δ-Phase Buffer Registers, as shown in the tables. When $ADDR_4$ is set low all input data will program NCO1, and when it is set high the data will program NCO2:

$ADDR_3$ - $ADDR_0$				Register Field
0	0	0	0	Δ-Phase Bits 7 –0(LSB)
0	0	0	1	Δ-Phase Bits15 – 8
0	0	1	0	Δ-Phase Bits 23 – 16
0	0	1	1	Δ-Phase Bits 31 – 24
1	1	0	0	ARST1 or ARST2
1	1	1	0	HOP CLK1 or HOP CLK2

Addresses $0C_H$, $0E_H$, $1C_H$ and $1E_H$ do not contain physical registers. The functions will be performed whenever any data values are written into these addresses. The remaining unspecified addresses do not contain any physical registers and do not perform any functions. When changing frequency data it is not necessary to reload unchanged bytes, and the byte loading sequence may be random.

HOP CLK1 and HOP CLK2

The HOP CLK inputs are used to control the transfer of the data from the Δ-Phase Buffer Registers to the Δ-Phase Registers. The frequency of the NCO output will change 16 falling clock edges after the corresponding HOP CLK command due to pipelining delays. The maximum frequency update rate is once every 8 SYS CLK1/2 cycles. The HOP CLK function can also be controlled by means of the FRLD software command by writing dummy data to address $0E_H$ (NCO1) or $1E_H$ (NCO2), as shown in the address table.

PM1 BIT_{2-0} and PM2 BIT_{2-0}

The two 3-bit inputs PM1 BIT_{2-0} and PM2 BIT_{2-0} are used to phase modulate NCO1 and NCO2 respectively. The MSB of each input (PM1/2 BIT_2) corresponds to a 180° phase shift at each output.

PM1 CLK and PM2 CLK

The PM1/2 CLK inputs are used to load the signals into the Phase ALUs. The phase of the NCO output will change 4 falling clock edges after the corresponding PM1/2 CLK command due to pipelining delays. The maximum phase update rate is once every 2 SYS CLK cycles.

OUTPUT SIGNALS

DAC1 BIT_{11-0} and DAC2 BIT_{11-0}

The signals appearing on the DAC1 BIT_{11-0} and DAC2 BIT_{11-0} output busses are derived from the 13 most significant bits of the corresponding Phase Accumulator. The 12-bit sine functions are presented in offset binary format. The value of the output for a given phase value follows the relationship:

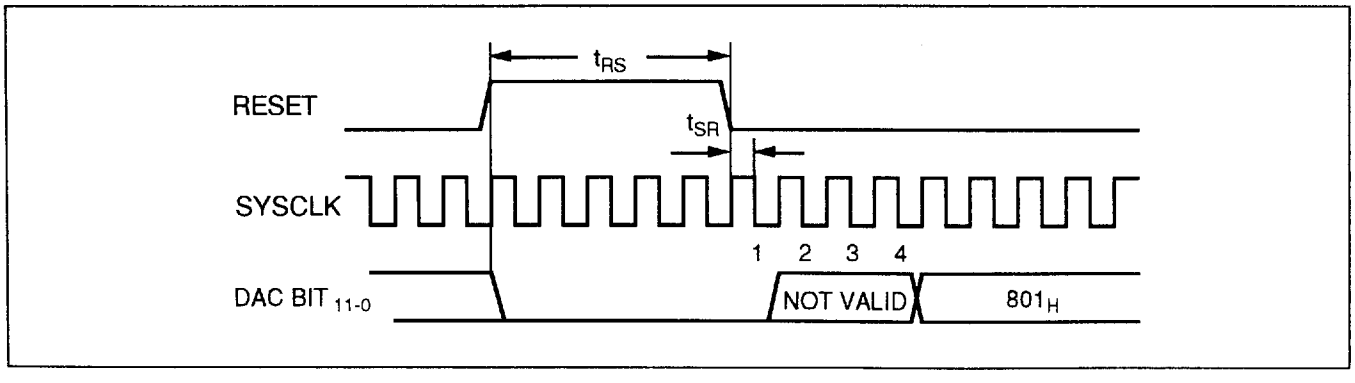
DAC BIT_{11-0}=2047 x sin (360 x (phase + 0.5)/8192)° + 2048

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 (801_H).

DAC1 STB and DAC2 STB

The DAC Strobe outputs are used to clock the digital to analog converters (DACs) used with the STEL-1178A for optimum timing. The DAC1 BIT_{11-0} and DAC2 BIT_{11-0} signals change on the falling edges of the corresponding DAC1/2 STB.

NCO RESET SEQUENCE



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125	°C (Plastic package)
		–65 to +150	°C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD}+0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial Conditions)
		+5 ± 10%	Volts (Military Conditions)
T_a	Operating Temperature (Ambient)	0 to +70	°C (Commercial Conditions)
		–55 to +125	°C (Military Conditions)

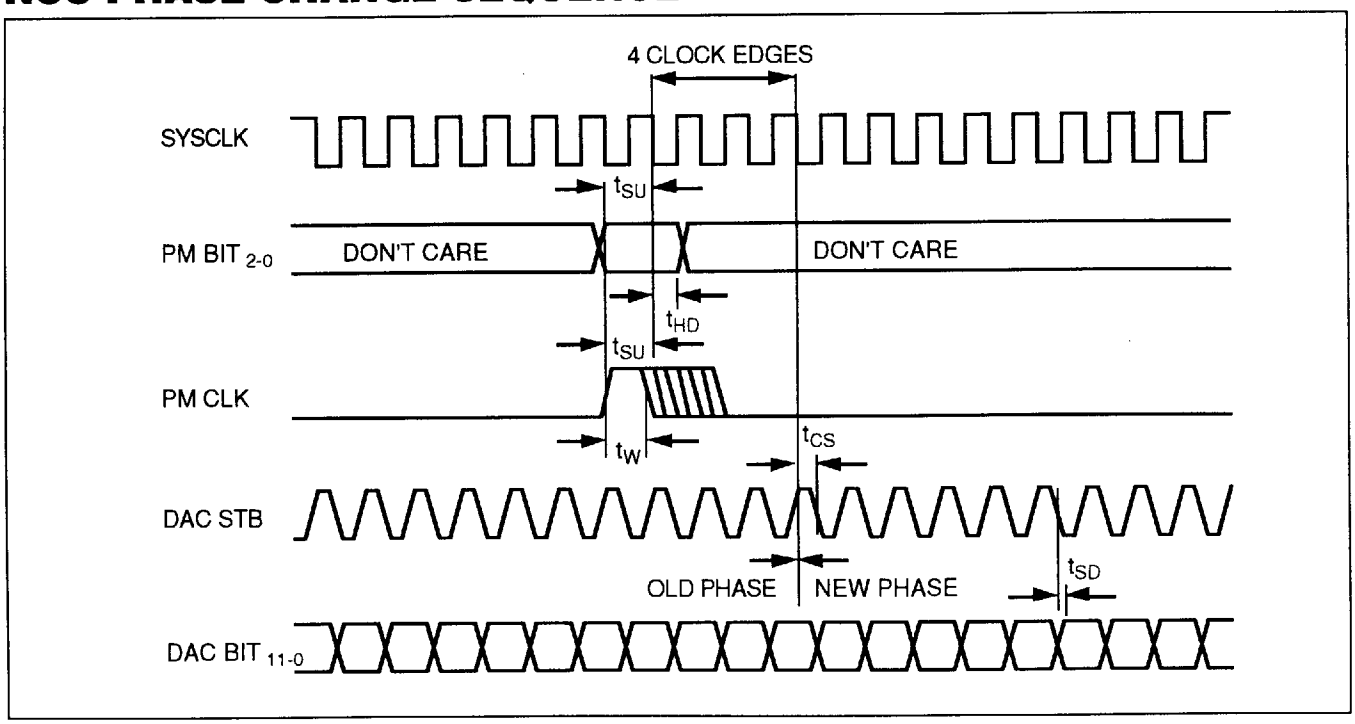
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	f_{CLK} = 80 MHz, each NCO
$V_{IH(min)}$	High Level Input Voltage					
	Commercial Operating Conditions	2.0			volts	Logic '1'
	Military Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	30	70	130	µA	**CS**, **WR**, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–60	–150	–300	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

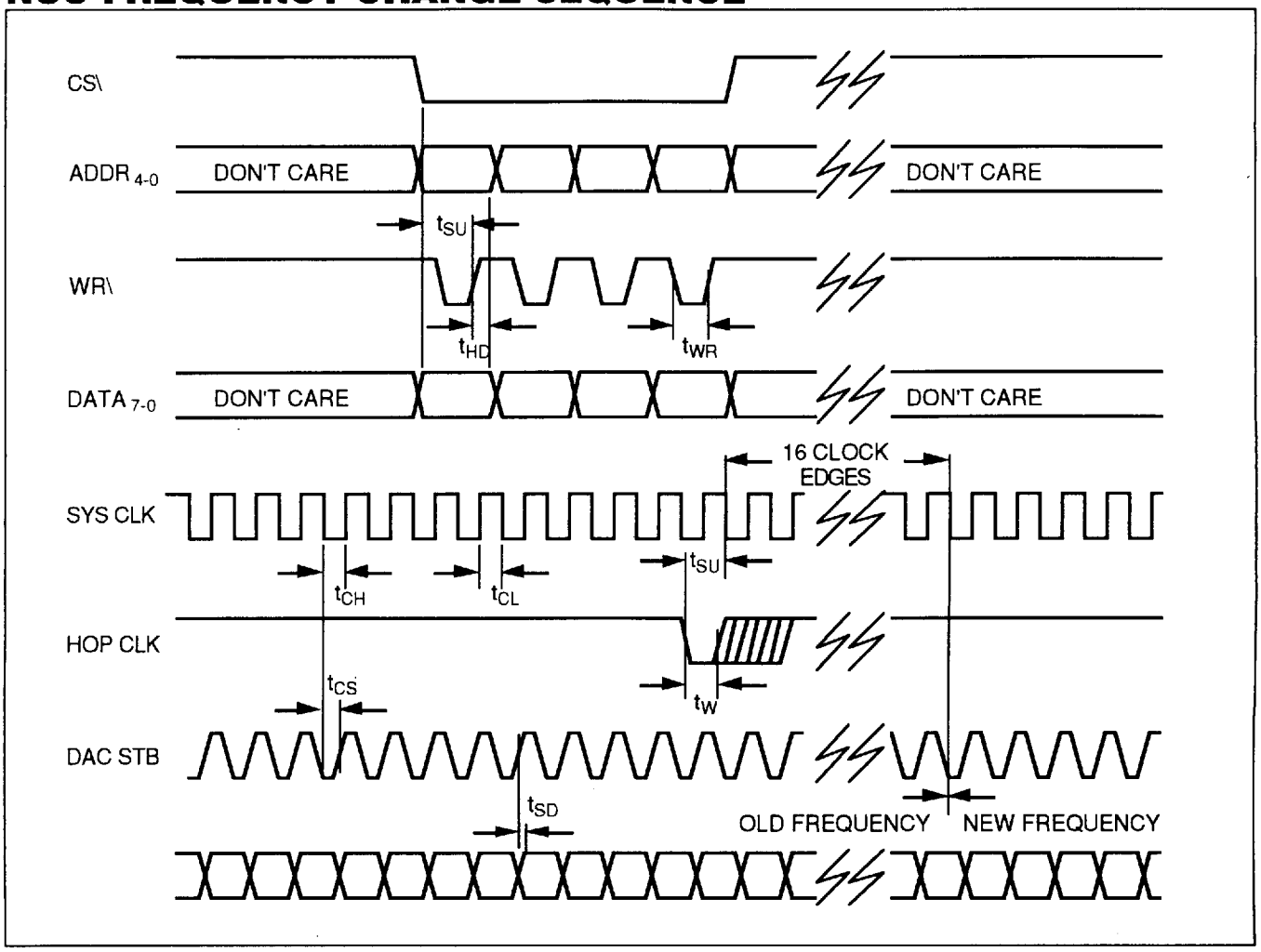
A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ± 10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

		STEL-1178A +50		STEL-1178A+80					
				Commercial		Military			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Conditions
t_{RS}	**RESET** pulse width	20		20		25		nsec.	
t_{SR}	**RESET** to **SYSCLK** Setup	10		10		12		nsec.	
t_{SU}	**DATA, ADDR** or **CS** to **WR** Setup, and **HOP CLK** or **PM CLK** to **SYS CLK** Setup	5		5		6		nsec.	
t_{HD}	**DATA, ADDR** or **CS** to **WR** Hold, and **HOP CLK** or **PM CLK** to **SYS CLK** Hold	5		5		6		nsec.	
t_{CH}	**SYS CLK** high	8		4		5		nsec.	f_{CLK} = max.
t_{CL}	**SYS CLK** low	8		4		5		nsec.	f_{CLK} = max.
t_W	**WR\, HOP CLK, PM CLK** pulse width	10		10		12		nsec.	
t_{CS}	**SYS CLK** to **DAC STB** delay	4	17	4	17	3	20	nsec.	Load = 15 pF (All outputs)
t_{SD}	**DACSTB** to **DAC BIT** delay	1	3	1	3	1	5	nsec.	Load = 15 pF (All outputs)

NCO PHASE CHANGE SEQUENCE



NCO FREQUENCY CHANGE SEQUENCE



APPLICATIONS INFORMATION

Requirements for using an STEL-1178A NCO in an application designed for the STEL-1178

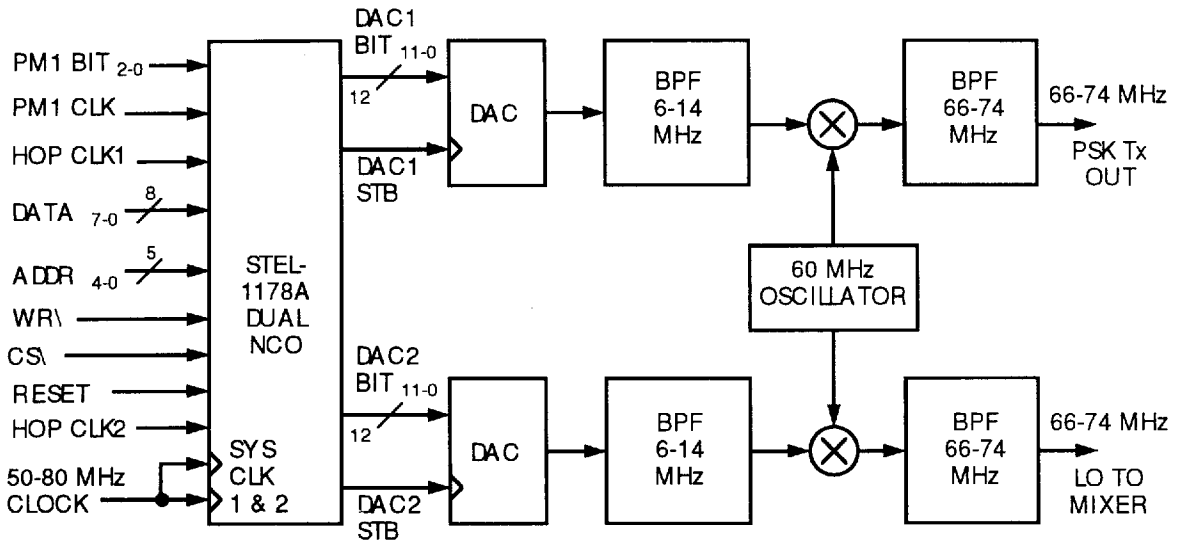
The STEL-1178A is an enhanced version of the STEL-1178 Dual NCO; the enhancement is the addition of 3-bit phase modulation to the two NCOs. As long as the phase modulation function is not inadvertently operated it is possible to use an STEL-1178A in an application that was designed around the STEL-1178. This is easily achieved by meeting the following criteria:

1. **Absolute minimum requirements for correct operation:**
   The phase modulation is triggered by the **PM1 CLK** and **PM2 CLK** signals on pins 30 and 64 respectively. As long as there are no active signals connected to these edge triggered inputs an STEL-1178A will operate in an identical manner to an STEL-1178 in the system.

2. For improved reliability of the STEL-1178A and its operation in the system it is desirable that the pins used for the phase modulation function in this device should not be left floating. (This is true of all unused inputs on CMOS devices.) This condition will be met by connecting pins 27-30 and 61-64 to either GND (V_{SS}) or V_{DD}. Since these pins are N.C. (No Connection) on the STEL-1178 these connections will not affect the operation of this device in the system.

APPLICATIONS INFORMATION

TYPICAL APPLICATION OF A DUAL NCO - TRANSMITTER PSK MODULATOR/ SYNTHESIZER AND RECEIVER LOCAL OSCILLATOR FOR A MODEM



The STEL-1178A is ideally suited for modem applications since it can be used to synthesize signals for both the transmitter and receiver sections simultaneously. In addition, the ability to modulate the signals allows the NCO used in the transmitter synthesizer to be used as the PSK modulator as well as the synthesizer. The NCO used in the receiver local oscillator synthesizer can be controlled by the host processor to act as a tracking oscillator and to be phase locked to the incoming signal.

SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

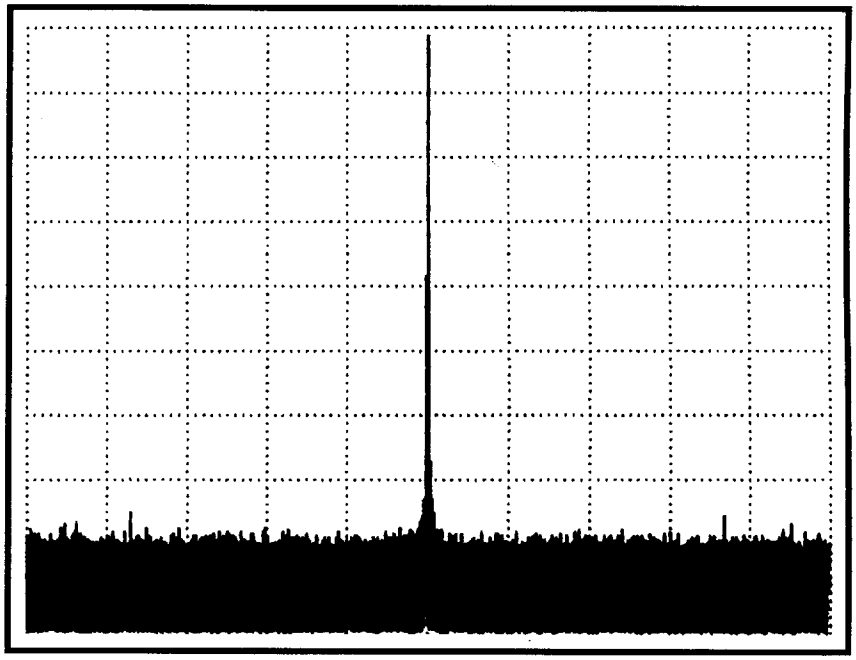
The sine or cosine signals generated by the STEL-1178A have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically at least 75 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the

NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 60 MHz and the output frequency is programmed to 6.789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 10 or 20 MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –74 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	6.7 MHz
Frequency Span:	10.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	60 MHz



FOR FURTHER INFORMATION

CALL OR WRITE

STANFORD TELECOMMUNICATIONS

ASIC & Custom Products Division

Tel: (408) 541-9031 Fax: (408) 541-9030

480 Java Drive • Sunnyvale, CA 94089-1125